

Document Title**256Kx8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Design target	January 30, 1997	Advance
0.1	Initial draft	April 7, 1997	Preliminary
1.0	Finalize - Improved $V_{IL}(\text{Min.})$: 0.4V → 0.6V - Erase reverse type package - Change speed bin KM68V2000 : 70/85ns KM68V2000I, KM68U2000, KM68U2000I : 85/100ns - Improved standby current Commercial product : 15 μ A → 10 μ A Industrial product : 30 μ A → 15 μ A - Increased Power dissipation : 0.7W → 1.0W	November 27, 1997	Final

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256Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology : TFT
- Organization : 256Kx8
- Power Supply Voltage
 - KM68V2000 Family : 3.0V ~ 3.6V
 - KM68U2000 Family : 2.7V ~ 3.3V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type :32-TSOP1-0820F, 32-TSOP1-0813.4F

GENERAL DESCRIPTION

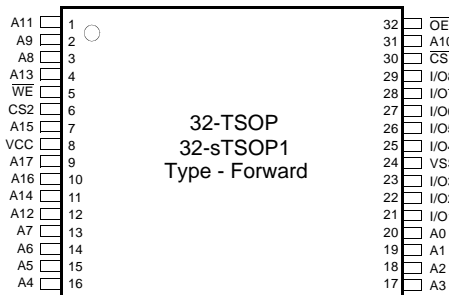
The KM68V2000 and KM68U2000 families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temp.	Vcc Range	Speed(ns)	Power Dissipation		PKG Type
				Standby (I _{SB1} , Max)	Operating (I _{CC2} , Max)	
KM68V2000L-L	Commercial (0~70°C)	3.0~3.6V	70/85	10µA	40mA ¹⁾	32-TSOP1-F 32-sTSOP1-F
KM68U2000L-L		2.7~3.3V	85/100			
KM68V2000LI-L	Industrial (-40~85°C)	3.0~3.6V	85/100	15µA		
KM68U2000LI-L		2.7~3.3V	85/100			

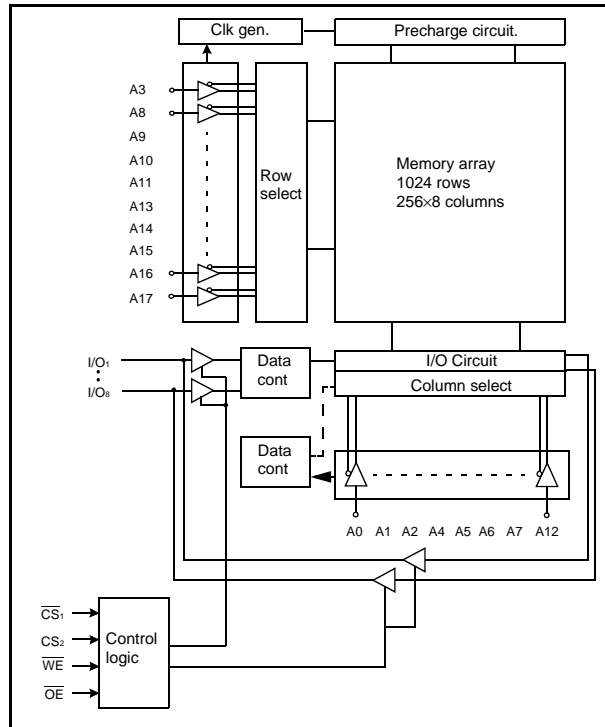
1. KM68V2000 family = 50mA

PIN DESCRIPTION



Name	Function
$\overline{CS}_1, \overline{CS}_2$	Chip Select Input
\overline{OE}	Output Enable Input
\overline{WE}	Write Enable Input
A0~A17	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM68V2000LT-7L KM68V2000LT-8L	32-TSOP1 F, 70ns, 3.3V, LL 32-TSOP1 F, 85ns, 3.3V, LL	KM68V2000LTI-8L KM68V2000LTI-10L	32-TSOP1 F, 85ns, 3.3V, LL 32-TSOP1 F, 100ns, 3.3V, LL
KM68U2000LT-8L KM68U2000LT-10L	32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL	KM68U2000LTI-8L KM68U2000LTI-10L	32-TSOP1 F, 85ns, 3.0V, LL 32-TSOP1 F, 100ns, 3.0V, LL
KM68V2000LTG-7L KM68V2000LTG-8L	32-sTSOP1 F, 70ns, 3.3V,LL 32-sTSOP1 F, 85ns, 3.3V,LL	KM68V2000LTGI-8L KM68V2000LTGI-10L	32-sTSOP1 F, 85ns, 3.3V,LL 32-sTSOP1 F, 100ns, 3.3V,LL
KM68U2000LTG-8L KM68U2000LTG-10L	32-sTSOP1 F, 85ns, 3.0V, LL 32-sTSOP1 F, 100ns, 3.0V, LL	KM68U2000LTGI-8L KM68U2000LTGI-10L	32-sTSOP1 F, 85ns, 3.0V, LL 32-sTSOP1 F, 100ns, 3.0V, LL

FUNCTIONAL DESCRIPTION

CS ₁	CS ₂	OE	WE	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	-
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.3 to 4.6	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM68V2000L, KM68U2000L
		-40 to 85	°C	KM68V2000LI, KM68U2000LI
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V _{CC}	KM68V2000 Family KM68U2000 Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	V _{SS}	All Family	0	0	0	V
Input high voltage	V _{IH}	KM68V2000, KM68U2000 Family	2.2	-	V _{CC} +0.3 ²⁾	V
Input low voltage	V _{IL}	KM68V2000, KM68U2000 Family	-0.3 ³⁾	-	0.6	V

Note:

- Commercial Product : T_A=0 to 70°C, otherwise specified
Industrial Product : T_A=-40 to 85°C, otherwise specified
- Overshoot : V_{CC}+3.0V in case of pulse width≤30ns
- Undershoot : -3.0V in case of pulse width≤30ns
- Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

- Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

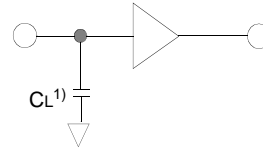
Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or CS ₂ =V _{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL} , Read	-	2	5	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, CS ₂ ≥V _{CC} -0.2V, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	2	5	mA
			Write	-	10	15	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, CS ₂ =V _{IH} , V _{IN} =V _{IH} or V _{IL}	-	30	40 ¹⁾	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, CS ₂ =V _{IL} , Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, CS ₂ ≥V _{CC} -0.2V or CS ₂ ≤0.2V, Other inputs=0-V _{CC}	-	0.2	10 ²⁾	μA	

- KM68V2000 Family = 50mA
- Industrial product = 15μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level : 0.4 to 2.2V
 Input rising and falling time : 5ns
 Input and output reference voltage : 1.5V
 Output load (see right) : $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (KM68V2000 Family : $V_{CC} = 3.0 \sim 3.6\text{V}$, KM68U2000 Family : $V_{CC} = 2.7 \sim 3.3\text{V}$ Commercial Product : $T_A = 0$ to 70°C , Industrial Product : $T_A = -40$ to 85°C)

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	70	-	85	-	100	-	ns
	Address access time	t _{AA}	-	70	-	85	-	100	ns
	Chip select to output	t _{CO1} , t _{CO2}	-	70	-	85	-	100	ns
	Output enable to valid output	t _{OE}	-	35	-	40	-	50	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	25	0	25	0	30	ns
	Output disable to high-Z output	t _{OHZ}	0	25	0	25	0	30	ns
	Output hold from address change	t _{OH}	10	-	15	-	15	-	ns
Write	Write cycle time	t _{WC}	70	-	85	-	100	-	ns
	Chip select to end of write	t _{CW}	60	-	70	-	80	-	ns
	Address set-up time	t _{AS}	0	-	0	-	0	-	ns
	Address valid to end of write	t _{AW}	60	-	70	-	80	-	ns
	Write pulse width	t _{WP}	55	-	60	-	70	-	ns
	Write recovery time	t _{WR}	0	-	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	25	0	30	0	30	ns
	Data to write time overlap	t _{DW}	30	-	35	-	40	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	5	-	ns

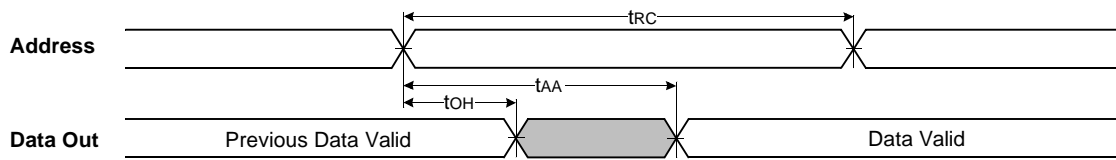
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS}_1^{(1)} \geq V_{CC} - 0.2\text{V}$	2.0	-	3.6	V
Data retention current	I _{DR}	$V_{CC} = 3.0\text{V}$ $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ $CS_2 \geq V_{CC} - 0.2\text{V}$ or $CS_2 \leq 0.2\text{V}$	-	0.2	10	μA
			-	0.2	10	
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

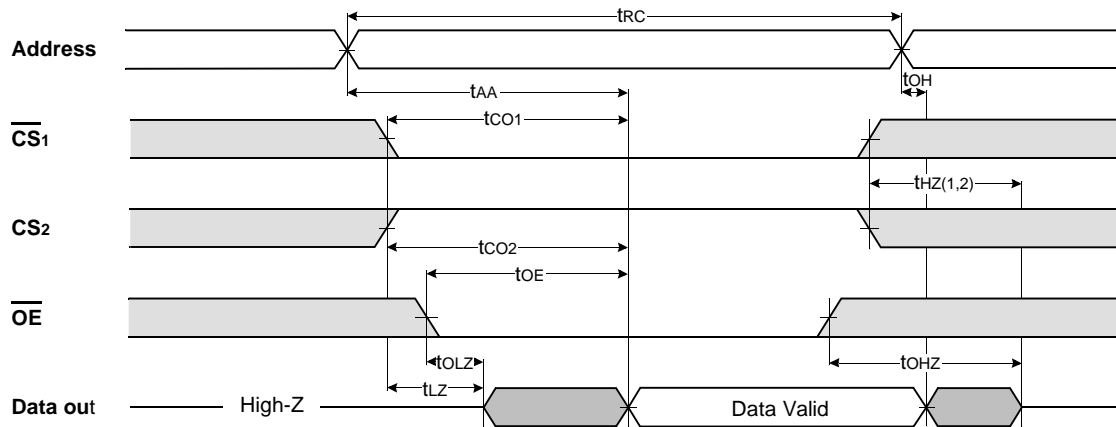
1. $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$, $CS_2 \geq V_{CC} - 0.2\text{V}$ (\overline{CS}_1 controlled) or $CS_2 \leq 0.2\text{V}$ (CS_2 controlled)

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$)



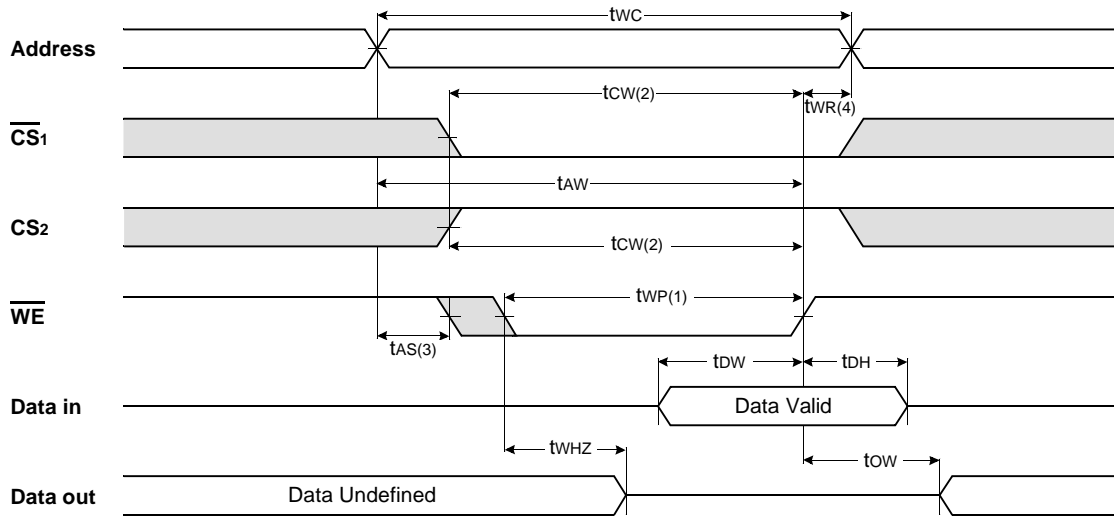
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE} = V_{IH}$)



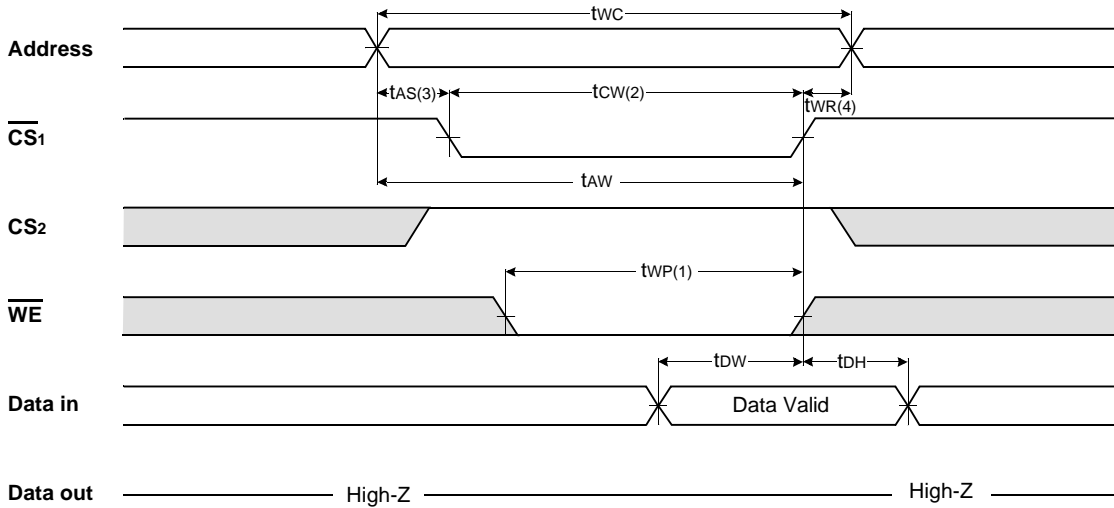
NOTES (READ CYCLE)

1. t_{HZ} and t_{OH} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

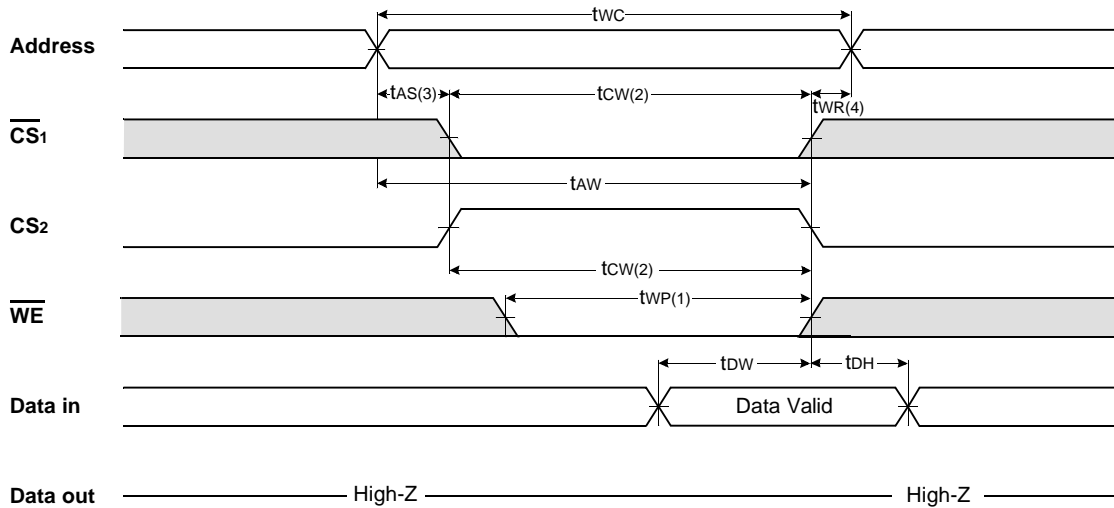
TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

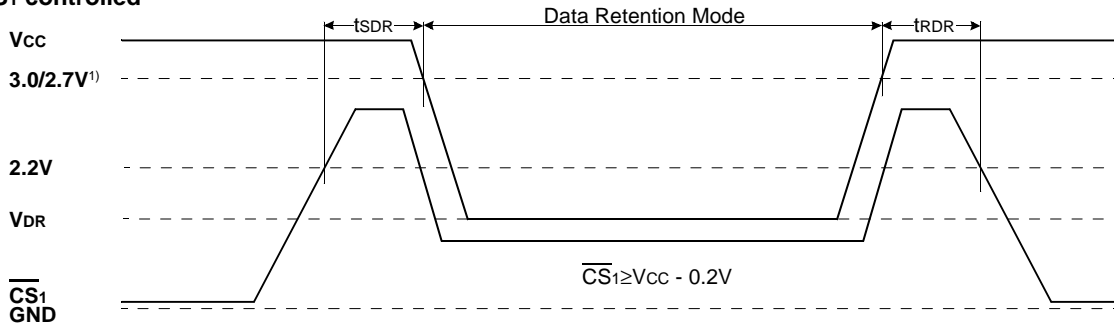


NOTES (WRITE CYCLE)

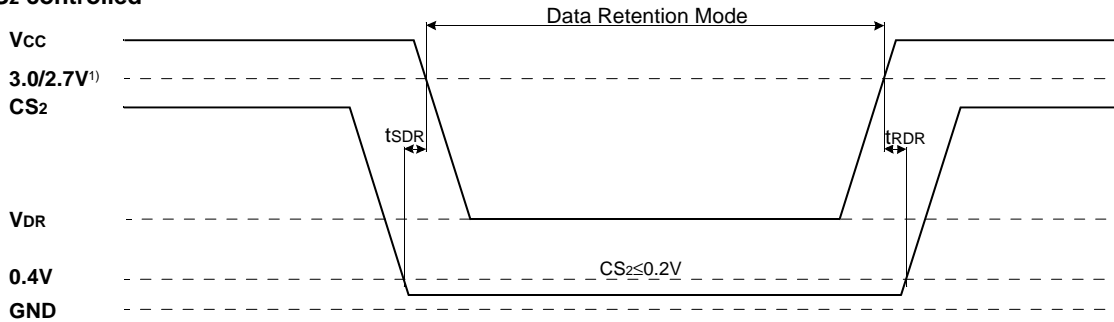
1. A write occurs during the overlap of a low \overline{CS}_1 , a high CS_2 and a low \overline{WE} . A write begins at the latest transition among \overline{CS}_1 goes low, CS_2 going high and \overline{WE} going low : A write ends at the earliest transition among \overline{CS}_1 going high, CS_2 going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the \overline{CS}_1 going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applied in case a write ends as \overline{CS}_1 or \overline{WE} going high t_{WR2} applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

\overline{CS}_1 controlled



CS_2 controlled

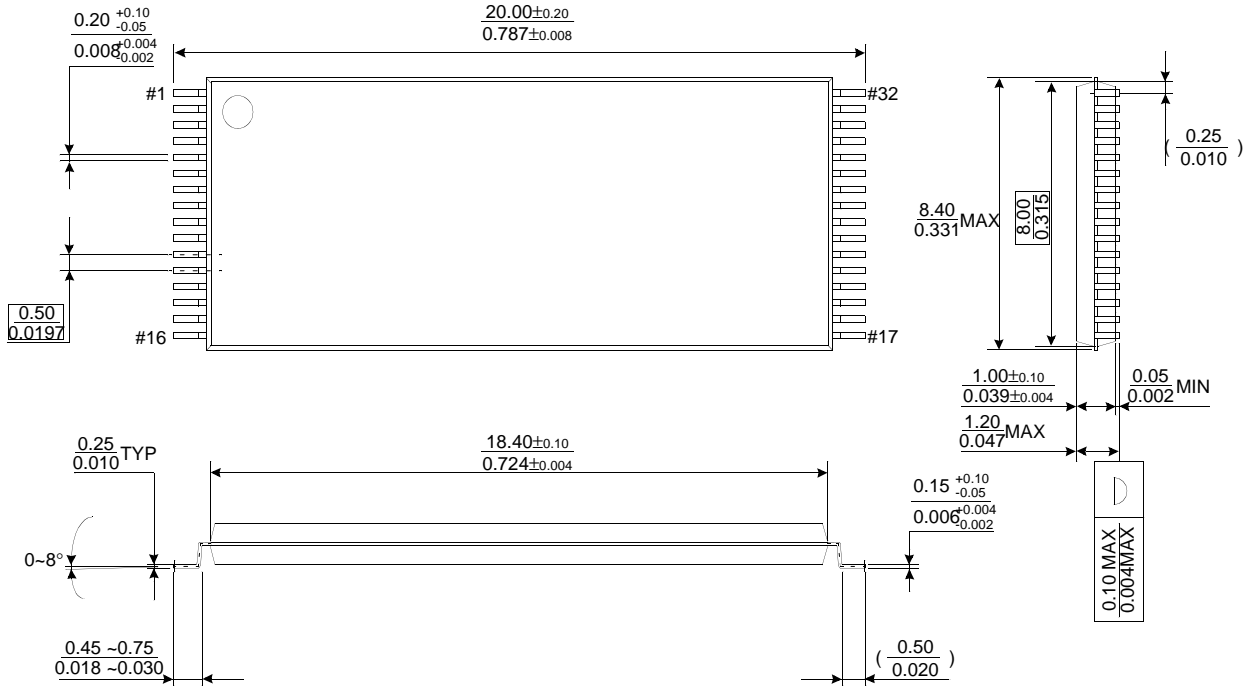


1. 3.0V for KM68V2000 Family, 2.7V for KM68U2000Family.

PACKAGE DIMENSIONS

Units : millimeter(inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

