REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated document. Added three device types 04, 05, and 06. Added S package. Added two vendors. Editorial changes throughout.	91-08-23	

REV																			
SHEET																			
REV	A	A																	
SHEET	15	16																	

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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CHECKED BY
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DRAWING APPROVAL DATE
18 DECEMBER 1989

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS EE PROGRAMMABLE ARRAY LOGIC, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89839
A	67268	

SHEET 1 OF 16

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Use previous edition until exhausted.

5962-E245

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-89839	01	R	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Supply current
01	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	30	130
02	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	20	130
03	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	15	130
04	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	10	130
05	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	25	65
06	16V8	16-input, 8-output, EECMOS, architecturally generic, programmable AND-OR array	20	65

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package
S	F-9 (20-lead, .540" x .300" x .100"), flat package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Off-state output voltage applied	-2.5 V dc to V_{CC} + 1.0 V dc 1/
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (TJ)	+175°C
Data retention	10 years (minimum)
Endurance	100 erase/write cycles (minimum)

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc
Low level input voltage (V_{IL})	V_{SS} -0.5 V dc to +0.8 V dc
High level output current (I_{OH})	-2.0 mA maximum
Low level output current (I_{OL})	12 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C

1/ Minimum input voltage is -0.5 V dc which may undershoot to -2.5 V dc for pulses less than 20 ns.
2/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The requirements for supplying programmed devices are not a part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Input leakage current	I_{LX}	$0.0 V \le V_{IN} \le V_{CC}$	01,02, 03,05, 06	1,2,3	-10	10	µA
			04		-100	10	
Bidirectional pin leakage current	$I_{I/O/Q}$	$0.0 V \le V_{I/O/Q} \le V_{CC}$	01,02, 03,05, 06	1,2,3	-10	10	µA
			04		-100	10	
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3		0.5	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2.0$ mA, $V_{IN} = V_{IH}$ or V_{IL}	All	1,2,3	2.4		V
Input low voltage 1/	V_{IL}		All	1,2,3	$V_{SS}-0.5$	0.8	V
Input high voltage 1/	V_{IH}		All	1,2,3	2.0	$V_{CC}+1.0$	V
Operating power supply current	I_{CC}	$V_{IL} = 0.5$ V, $V_{IH} = 3.0$ V, $f_{tog} = 25$ MHz	01,02, 03,04	1,2,3		130	mA
			05,06			65	
Output short circuit current 2/	I_{OS}	$V_{CC} = 5.0$ V, $V_{OUT} = 0.5$ V, $T_A = +25°C$, see 4.3.1d	All	1	-30	-150	mA
Input capacitance	C_{IN}	$V_{CC} = 5.0$ V, $V_I = 2.0$ V, $f = 1.0$ MHz, $T_A = +25°C$, see 4.3.1c	All	4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V $\le V_{CC} \le$ 5.5 V unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Bidirectional pin capacitance	$C_{I/O/Q}$	V_{CC} = 5.0 V, $V_{I/O/Q}$ = 2.0 V, f = 1.0 MHz, $T_A = +25°C$, see 4.3.1c	All	4		10	pF
Input or feedback to nonregistered output	t_{PD}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11	3.0	30	ns
			02,06		3.0	20	
			03		3.0	15	
			04		2.0	10	
			05		3.0	25	
Clock to output delay 4/	t_{CO}		01	9,10,11	2.0	20	ns
			02,06		2.0	15	
			03		2.0	12	
			04		1.0	7.0	
			05		2.0	15	
Input to output enable	t_{EA1}		01	9,10,11		30	ns
			02,06			20	
			03			15	
			04			10	
			05			25	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Input to output register enable 4/	t_{EA2}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11		25	ns
			02,06			18	
			03			15	
			04			10	
			05			20	
Input to output disable 5/	t_{ER1}		01	9,10,11		30	ns
			02,06			20	
			03			15	
			04			10	
			05			25	
Input to output register disable 4/ 5/	t_{ER2}		01	9,10,11		25	ns
			02,06			18	
			03			15	
			04			10	
			05			20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{SS} = 0 V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Clock frequency without feedback 4/	f_{CLK1}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11	0.0	33.3	MHz
			02,06		0.0	41.6	
			03		0.0	50.0	
			04		0.0	62.5	
			05		0.0	33.3	
Clock frequency with feedback 4/	f_{CLK2}		01	9,10,11	0.0	22.2	MHz
			02,06		0.0	33.3	
			03		0.0	41.6	
			04		0.0	58.5	
			05		0.0	28.5	
Input or feedback setup time, before rising clock 4/	t_S		01	9,10,11	25		ns
			02,06		15		
			03		12		
			04		10		
			05		20		
Input or feedback hold time after rising clock 4/	t_H		All	9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Device type	Group A sub-groups	Limits Min	Limits Max	Unit
Clock pulse width, high 4/	t_{PWH}	V_{CC} = 4.5 V, see figures 3 and 4 3/	01	9,10,11	15		ns
			02,06		12		
			03		10		
			04		8.0		
			05		15		
Clock pulse width, low 4/	t_{PWL}		01	9,10,11	15		ns
			02,06		12		
			03		10		
			04		8.0		
			05		15		

1/ These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

2/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second (see 4.3.1d).

3/ AC tests are performed with input rise and fall times (10 percent to 90 percent) of 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and the output load of figure 3. Input pulse levels are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.

4/ Test applies only to registered outputs.

5/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

Device types	All
Case outlines	R, S, and 2
Terminal number	Terminal symbol
1	I/CLK
2	I
3	I
4	I
5	I
6	I
7	I
8	I
9	I
10	GND
11	I/$\overline{OE}$
12	I/O/Q
13	I/O/Q
14	I/O/Q
15	I/O/Q
16	I/O/Q
17	I/O/Q
18	I/O/Q
19	I/O/Q
20	V_{CC}

FIGURE 1. Terminal connections.

Inputs										Outputs							
I/CLK	I/$\overline{OE}$	I	I	I	I	I	I	I	I	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q
X	X	X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H

X = don't care state
H = logic high

FIGURE 2. Truth table (unprogrammed).

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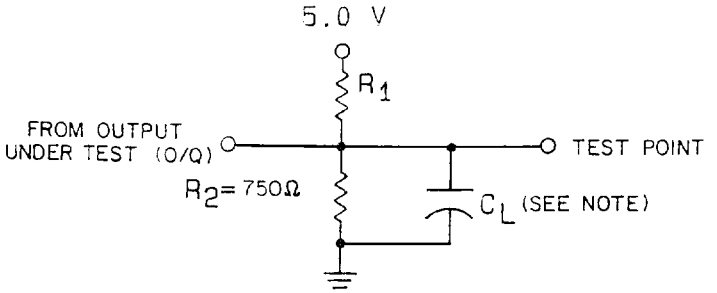

Test	R_1	C_L (minimum)
t_{PD}, t_{CO}, f_{CLK1}, f_{CLK2}	390Ω	50 pF
t_{EA1}, t_{EA2}	Active high = infinity Active low = 390Ω	50 pF
t_{ER1}, t_{ER2}	Active high = infinity Active low = 390Ω	5.0 pF

NOTE: C_L = load capacitance and includes jig and probe capacitance.

FIGURE 3. Output load circuit.

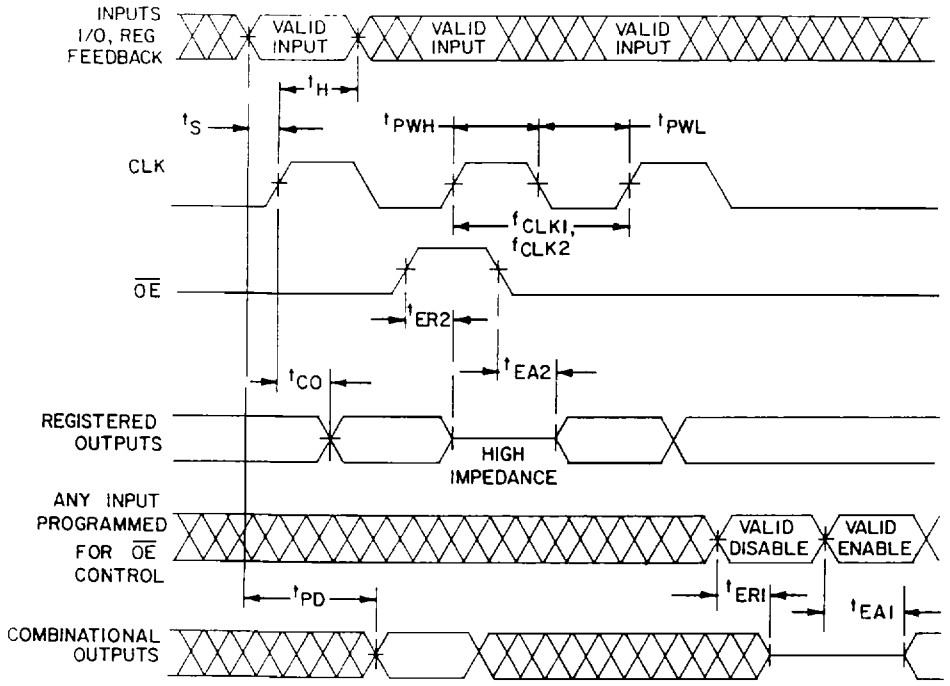

FIGURE 4. Switching waveforms.

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3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

(4) The burn-in pattern shall be read before and after burn-in. Devices having any logic array bits not in the proper state shall constitute a device failure and shall be added as failures for PDA calculation.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/retention test prior to burn-in, in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be at equipment room ambient temperature and shall cycle all bit locations for a minimum of 100 cycles. After cycling, devices containing bits which fail to verify shall be considered device failures.

(2) The retention pattern must have 100 percent of the logic array programmed.

(3) After cycling, perform a high temperature unbiased bake for a minimum 48 hours at +150°C. The bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T1} - \frac{1}{T2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K)
t_1 = time (hours) at temperature T_1
t_2 = time (hours) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8A, 8B,9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7,8A, 8B,9,10,11
Group C and D end-point electrical parameters (method 5005)	2,3,7,8A,8B

* PDA applies to subgroups 1 and 7.
** See 4.3.1c

(4) After cycling and bake and prior to burn-in read the data retention pattern. Test using subgroups 1 and 7 (at the manufacturer's option, high temperature equivalent subgroups 2 and 8A or low temperature equivalent subgroups 3 and 8B may be used in lieu of subgroups 1 and 7). Devices having any logic array bits not in the proper state after storage shall constitute device failure.

(5) At the manufacturer's option, the testing specified in 4.2c(4) may be deleted if the devices are put into burn-in with no reprogramming allowed between the start of data retention bake and the end of burn-in. Exercising this option will result in data retention bake failures being caught and included in post burn-in PDA calculations.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O/Q}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. I_{OS} measurements in subgroup 1 shall be measured only for the initial test and after process or design changes which may affect I_{OS}. Sample size is 15 devices with no failures, and all output terminals tested.

4.3.2 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

c. An extended data retention test shall be added, a new sample shall be selected and the sample size, frequency of testing, and LTPD shall be the same as that required for subgroup 1 of group C inspection. Extended data retention shall also consist of as follows:

(1) All devices shall have 100 percent of the logic array programmed with a charge on all cells, such that the cell will not be in a neutral state.

(2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using a higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T1} - \frac{1}{T2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2.
T = temperature in Kelvin (i.e., °C + 273 = K)
t_1 = time (hours) at temperature T_1
t_2 = time (hours) at temperature T_2
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

(3) Read the pattern after bake and perform end-point electrical tests in accordance with table II herein for group C.

4.3.3 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and end-point electrical parameters shall be as specified in table II herein.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.

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STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 91-08-23

Approved sources of supply for SMD 5962-89839 revision A are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8983901RX	66675 34335	GAL16V8A-30LD/883C PALCE16V8H-25E4/BRA
5962-89839012X	66675 34335	GAL16V8A-30LR/883C PALCE16V8H-25E4/B2A
5962-8983902RX	66675 34335 27014	GAL16V8A-20LD/883C PALCE16V8H-20E4/BRA GAL16V8L20J/883
5962-89839022X	66675 34335	GAL16V8A-20LR/883C PALCE16V8H-20E4/B2A
5962-8983902SX	27014	GAL16V8L20W/883
5962-8983903RX	66675 34335 27014	GAL16V8A-15LD/883C PALCE16V8H-15E4/BRA GAL16V8L15J/883
5962-89839032X	66675 34335	GAL16V8A-15LR/883C PALCE16V8H-15E4/B2A
5962-8983903SX	27014	GAL16V8L15W/883
5962-8983904RX	66675	GAL16V8B-10LD/883C
5962-89839042X	66675	GAL16V8B-10LR/883C
5962-8983905RX	66675	GAL16V8A-25QD/883C
5962-89839052X	66675	GAL16V8A-25QR/883C

See footnote at end of list.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8983906RX	66675	GAL16V8A-20QD/883C
5962-89839062X	66675	GAL16V8A-20QR/883C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
66675	Lattice Semiconductor Corporation 5555 NE Moore Court Hillsboro, OR 97124-6421
34335	Advanced Micro Devices 901 Thompson Place P O Box 3453 Sunnyvale, CA 94088
27014	National Semiconductor Corporation 2900 Semiconductor Drive P. O. Box 58090 Santa Clara, CA 95052-8090