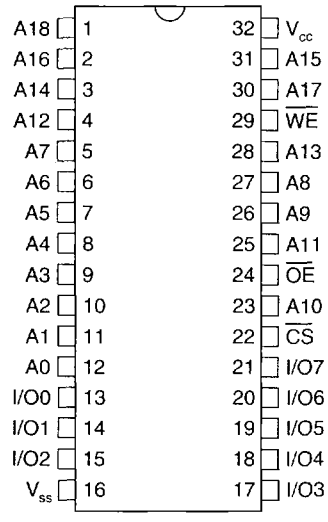


FIGURE 1 — Pin Configuration

A0 - A18	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

Pin Description

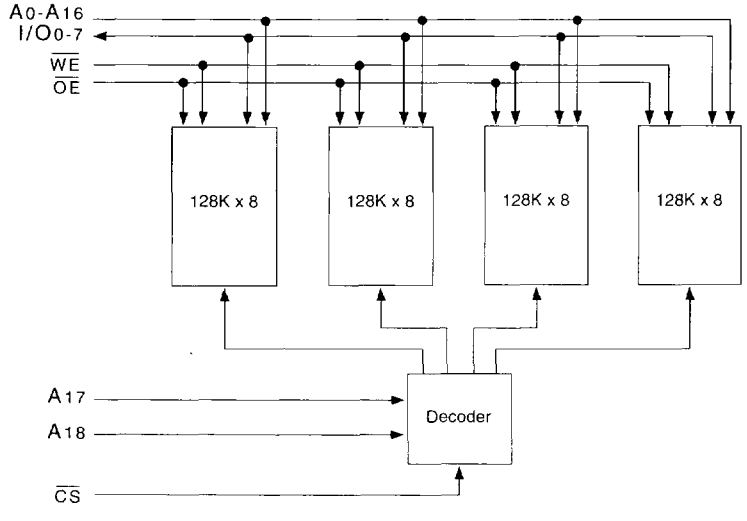


FIGURE 2 — Block Diagram

WS-512K8-XPX

512K x 8 CMOS SRAM Module High Speed

FEATURES

- **Access Times of 25 to 70nS**
- **Plastic/FR4 Substrate**
- **32 Pin DIP, JEDEC Approved Pinout**
- **Commercial and Industrial Temperature Ranges**
- **5 Volt Operation**
- **All CMOS Fully Static Design, No Clock**
- **Battery Back-Up Operation**
- **TTL Compatible Inputs and Outputs**
- **Onboard Decoupling Capacitors**

DESCRIPTION

The White Technology model WS-512K8-XPX is a 512K x 8 CMOS SRAM module, constructed of four 128K x 8 SOJ SRAMs mounted on a FR4 laminate. Featuring JEDEC standard pinouts, the device provides 512K bytes of read/write low power memory. The device is well suited for battery backed operation and will retain data at voltages as low as 2.0 volts.

Inputs and outputs are TTL compatible. The logic levels and drive capabilities permit the memory to interface with most digital logic systems. Since the device is all CMOS, low power operation for standby applications such as battery backed systems is straightforward.

The memory features low power consumption. In typical systems where multiple modules are operating using chip select to activate each device, the overall current requirement is only slightly above that for one unit. Those units not selected require only standby current.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Commercial	Industrial	Unit
Operating Temperature	T_A	0 to 70	-40 to +85	°C
Storage Temperature	T_{STG}	-40 to +85	-55 to +125	°C
Supply Voltage	V_{CC}	-0.5 to 7.0	-0.5 to 7.0	V
Signal Voltage Relative to GND	V_G	-0.6 to +6.25	-0.6 to +6.25	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Device Current
H	X	X	Standby	High Z	Standby (deselect/power down)
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Read	High Z	Active (deselect)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Com)	T_A	0	+70	°C

CAPACITANCE

(T_A = 25°C)

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	20	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Symbol	Conditions	-25		-35		-45		-55		-70		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		5		5		5		5		5	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		5		5		5		5		5	µA
Dynamic Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		65		65		65		65		65	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		4		4		4		4		4	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = Min		0.4		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = Min	2.4		2.4		2.4		2.4		2.4		V

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to 85°C)

Parameter	Symbol	Conditions	-25		-35		-45		-55		-70		Units
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		5		5		5		5		5	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		5		5		5		5		5	µA
Dynamic Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		75		75		75		75		75	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		5		5		5		5		5	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = Min		0.4		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = Min	2.4		2.4		2.4		2.4		2.4		V

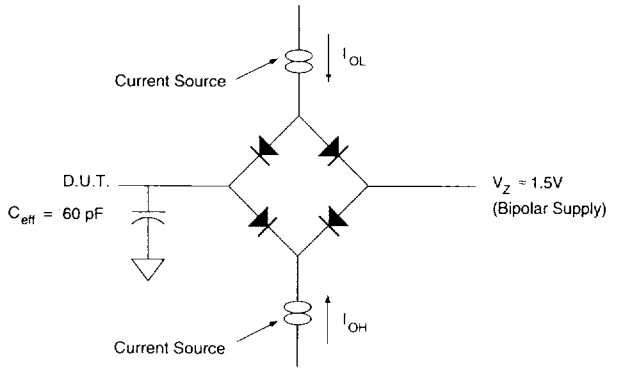


FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Typ.	Unit
Input Pulse Level	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Load Capacitance	100	pF

Notes:

V_Z is programmable from -2V to +7V

I_{OL} & I_{OH} programmable from 0 to 16mA

Tester Impedance Z_0 = 75 Ω

V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)

I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE Tester Includes Jig Capacitance

AC ELECTRICAL CHARACTERISTICS

(Vcc = 5.0V)

Parameter Read Cycle	Symbol	-25		-35		-45		-55		-70		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	25		35		45		55		70		nS
Address Access Time	t_{AA}		25		35		45		55		70	nS
Data Hold from Address Change	t_{OH}	4		4		4		4		5		nS
Chip Select Access	t_{ACS}		25		35		45		55		70	nS
Output Enable to Output Valid	t_{OE}		15		20		25		30		45	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		nS
Chip Deselect to Output in High Z	t_{CHZ}[1]		12		15		20		25		30	nS
Output Disable to Output in High Z	t_{OHZ}[1]		12		15		20		25		30	nS

1. This parameter is guaranteed by design but not tested.

Parameter Write Cycle	Symbol	-25		-35		-45		-55		-70		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	25		35		45		55		70		nS
Chip Select to End of Write	t_{CW}	20		30		40		45		50		nS
Address Valid to End of Write	t_{AW}	20		30		40		45		50		nS
Data to Write-Time Overlap	t_{DW}	15		18		20		25		30		nS
Data Hold from Write Time	t_{DH}	0		0		0		0		0		nS
Write Pulse Width	t_{WP}	20		25		35		40		50		nS
Address Setup Time	t_{AS}	0		0		0		0		0		nS
Write Recovery Time	t_{WR}	0		0		0		0		5		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		5		nS
Write to Output in High Z	t_{WHZ}[1]		10		15		15		20		25	nS

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORMS

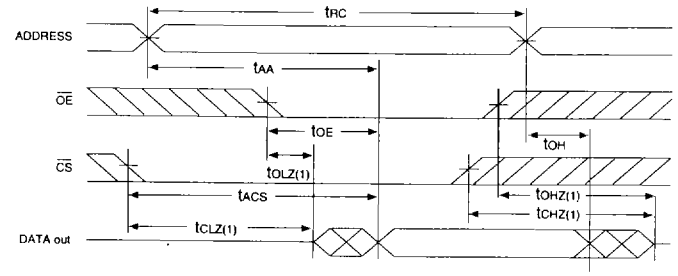


FIGURE 4 — Read Cycle Timing

1. Measured ± 200mV steady state; guaranteed by design but not tested.

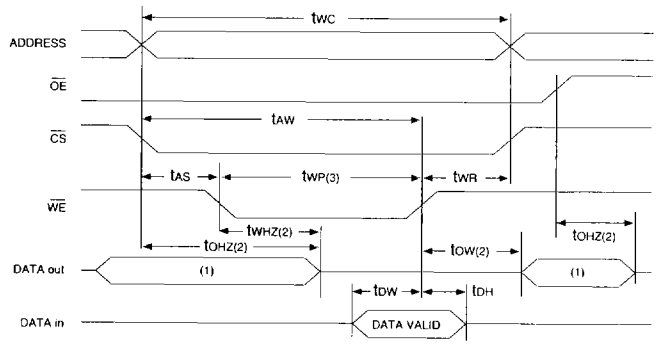


FIGURE 5 — Write Cycle Timing $\overline{WE}$ Controlled

1. I/O pins are in their output state, input signals must not be applied.
2. This parameter is guaranteed by design but not tested.
3. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

DATA RETENTION CHARACTERISTICS

(T_A = 0°C TO +70°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			-70			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		375	1000		375	1000		375	1000		375	1000		375	1000	µA
	I_{CCDR2}	V_{CC} = 2V		200	500		200	500		200	500		200	500		200	500	µA

(T_A = -40°C TO +85°C)

Parameter	Symbol	Conditions	-25			-35			-45			-55			-70			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Data Retention Supply Voltage	V_{DR}	$\overline{CS} \geq V_{CC}$ -.2V	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		375	1500		375	1500		375	1500		375	1500		375	1500	µA
	I_{CCDR2}	V_{CC} = 2V		200	800		200	800		200	800		200	800		200	800	µA

ORDERING INFORMATION

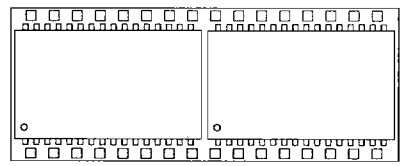
TEMPERATURE RANGE OPTIONS

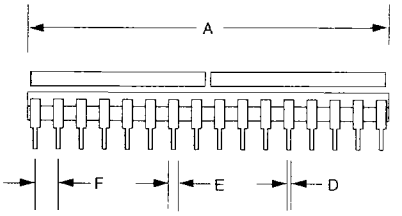
C	Commercial	0°C to +70°C
I	Industrial	-40°C to +85°C

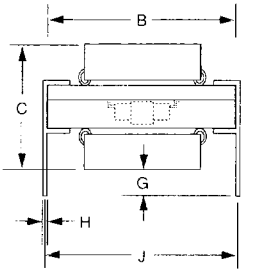
W S - 512K 8 - XX P XX

- PROCESSING: C = Commercial, I = Industrial
- PACKAGE: P = FR4 DIP/Plastic
- ACCESS TIME IN nS
- BITS PER WORD
- NUMBER OF WORDS
- STATIC RAM
- WHITE TECHNOLOGY

PACKAGE OUTLINE







DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.635	1.686	41.5	42.8
B	0.580	0.600	14.7	15.2
C	0.400	0.440	10.1	11.1
D	0.016	0.020	0.4	0.5
E	0.045	0.055	1.1	1.4
F	0.100 TYP.		2.5 TYP.	
G	0.125	0.170	3.17	4.3
H	0.008	0.012	0.2	0.30
J	0.590	0.610	15.0	15.5

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