DATA SHEET

M 65888/M 65889

16,384 × 4
Static R/W RAM

FEATURES

- **BICMOS FOR OPTIMUM SPEED/POWER**
- **HIGH SPEED**
  COMMERCIAL: 8/9/10/12 ns (max)
  MILITARY: 10/12/15 ns (max)
- **LOW ACTIVE POWER**
  735 mW
- **LOW STANDBY POWER**
  263 mW
- **TTL-COMPATIBLE INPUTS AND OUTPUTS**
- **CAPABLE OF WITH STANDING GREATER THAN 2001 V ELECTROSTATIC DISCHARGE**

INTRODUCTION

The M-65888 and M-65889 are high-performance BiCMOS static RaMs organized as 16,384 × 4 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. The 65889 has an active LOW output enable ($\overline{OE}$) feature. Both devices have an automatic power-down feature, reducing the power consumption by 67 % when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW for M-65889) while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

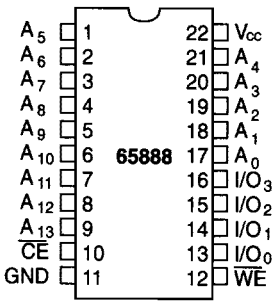
The I/O pins stay in high-impedance state when chip enable ($\overline{CE}$) is HIGH, or write enable ($\overline{WE}$) is LOW (or output enable ($\overline{OE}$) is HIGH for M-65889).

For military/space applications that demand superior levels of performance and reliability the M-65888/889 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

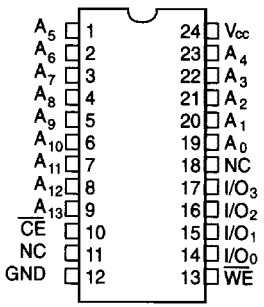
INTERFACE

PIN CONFIGURATION

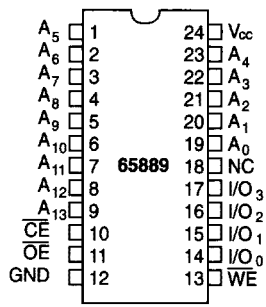
Plastic 300 mils 24 pins, 22 pins, DIL
Ceramic 300 mils 24 pins, 22 pins DIL
SOJ 300 mils 24 pins



Pinout DIL (Top View)

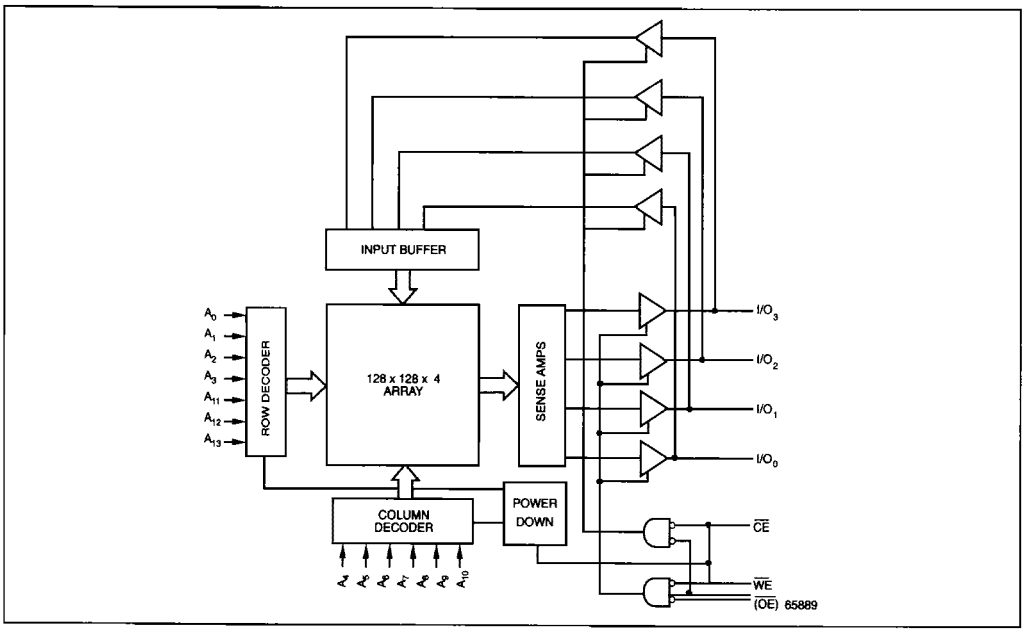


Pinout SOJ (Top View)



Pinout DIL/SOJ (Top View)

BLOCK DIAGRAM



SELECTION GUIDE

		M-65888-08 M-65889-08	M-65888-09 M-65889-09	M-65888-10 M-65889-10	M-65888-12 M-65889-12	M-65888-15 M-65889-15
Maximum Access Time (ns)		8	9	10	12	15
Maximum Operating Current (mA)	Commercial	140	130	130	120	
	Military			145	140	135
Maximum Standby Current (mA)	Commercial	50	50	40	40	
	Military			60	55	50

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(Above which the useful life may be impaired. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. For user guidelines, not tested).

Storage Temperature ..... – 65 °C to + 150 °C
Supply Voltage
to Ground Potential ..... – 0.5 V to + 7.0 V
DC Voltage Applied
to Outputs in High Z State ..... – 0.5 V to + 7.0 V
DC Input Voltage ..... – 3.0 V to + 7.0 V
Output Current into Outputs (Low) ..... 20 mA
Static Discharge Voltage ..... > 2001 V
(per MIL-STD-883, Method 3015)
Latch-up Current ..... >200 mA

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial (2)	– 0 °C to + 70 °C	– 08, – 09 5 V ± 5 %
		– 10, – 12 5 V ± 10 %
Military (2)	– 55 °C to + 125 °C	5 V ± 10 %

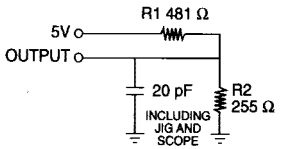
PARAMETERS	DESCRIPTION	TEST CONDITIONS			M-65888-08 M-65889-08		M-65888-09 M-65889-09		M-65888-10 M-65889-10		M-65888-12 M-65889-12		M-65888-15 M-65889-15		UNITS
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = – 4 mA	Com'l	2.4		2.4		2.4		2.4				V
			I_{OH} = – 2 mA	Mil					2.4		2.4		2.4		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA				0.4		0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Level				2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]				– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	– 0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC} Output Disabled			– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	– 10	+ 10	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA f = f max.		Com'l		140		130		130		120			mA
				Mil						145		140		135	mA
I_{SB}	$\overline{CE}_1$ Power-Down Current	$\overline{CE}_1$ ≤ V_{IH}		Com'l		50		50		40		40			mA
				Mil						60		55		50	mA

CAPACITANCE[3]

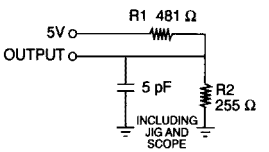
PARAMETER	DESCRIPTION	TEST CONDITIONS	MAXIMUM[4]	UNITS
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	5	pF
C_{OUT}	Output capacitance		7	pF

Notes : 1. V_{IL} (min) = – 3.0 V for pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. Tested initially and after any design or process changes that may affect these parameters.
4. For all packages except Ceramic DIL, which has maximum of C_{IN} = 8 pf, C_{OUT} = 9 pF.

AC TEST LOADS AND WAVEFORMS

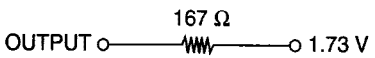


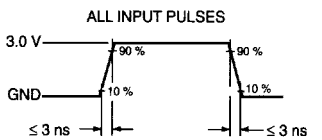
(a)



(b)

Equivalent to : THEVENIN EQUIVALENT





SWITCHING CHARACTERISTICS (OVER THE OPERATING RANGE[5])

READ CYCLE

SYMBOL	PARAMETER		M-65888-08 M-65889-08		M-65888-09 M-65889-09		M-65888-10 M-65889-10		M-65888-12 M-65889-12		M-65888-15 M-65889-15		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAV	Read Cycle Time		8		9		10		12		15		ns
TAVQV	Address to Data Valid			8		9		10		12		15	ns
TAVQX	Data Hold from Address Change		2.5		2.5		3		3		3		ns
TELQV	$\overline{CE}$ LOW to Data Valid			8		9		10		12		15	ns
TGLQV	$\overline{OE}$ LOW to Data Valid	65889		4.2		4.5		5		5		6	ns
TGLQX	$\overline{OE}$ LOW to Low Z	65889	1.5		1.5		2		2		2		ns
TGHQZ	$\overline{OE}$ HIGH to High Z (6)	65889		4		5		5		6		7	ns
TELQX	$\overline{CE}$ to Low Z (7)		2		2		2		2		3		ns
TEHQZ	$\overline{CE}$ HIGH to HIGH Z (6, 7)			4		5		5		6		7	ns

WRITE CYCLE[8]

SYMBOL	PARAMETER	M-65888-08 M-65889-08		M-65888-09 M-65889-09		M-65888-10 M-65889-10		M-65888-12 M-65889-12		M-65888-15 M-65889-15		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TAVAV	Write Cycle Time	8		9		10		12		15		ns
TELWH	$\overline{CE}$ LOW to Write End	7		8		8		8		10		ns
TAVWH	Address Set-Up to Write End	7		8		8		8		10		ns
TWHAX	Address Hold From Write End	0		0		0		0		0		ns
TAVWL	Address Set-Up to Write Start	0		0		0		0		0		ns
TWLWH	$\overline{WE}$ Pulse Width	6.5		7		8		8		10		ns
TDVWH	Data Set-up to Write End	4		4.5		5		6		7		ns
TWHDX	Data Hold from Write End	0		0		0		0		0		ns
TWLQZ	$\overline{WE}$ LOW to High Z[6]		4		5		5		6		7	ns
TWHQX	$\overline{WE}$ HIGH to Low Z	2		2		2		2		3		ns

Notes : 5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH}, and $C_L = 20$ pF.

6. TGHQZ, TEHQZ and TWLQZ are specified with $C_L = 5$ pF as in part (b) in AC Test Loads. Transition is measured ± 220 mV from steady-state voltage.

7. At any given temperature and voltage condition, TEHQZ is less than TELQX for any given device.

8. The internal write time of the memory is defined by the overlap of $\overline{CE}$, LOW, and $\overline{WE}$ LOW. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write. All three signals must be active to initiate a write, and either signal can terminate a write by going inactive.

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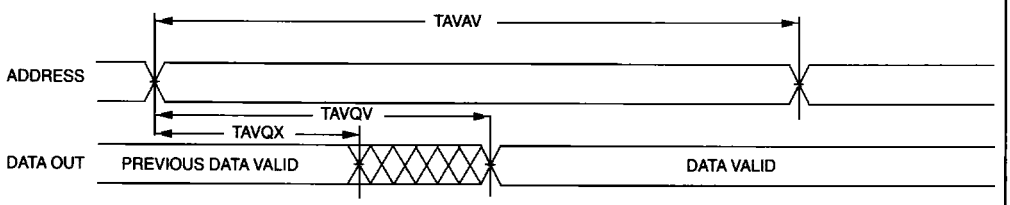
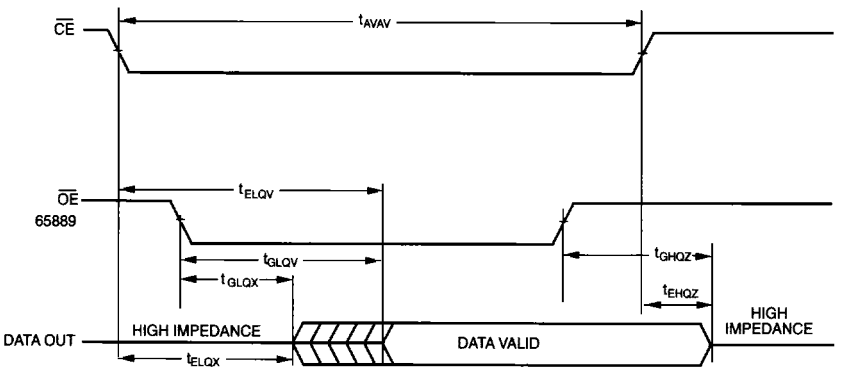
SWITCHING WAVEFORMS

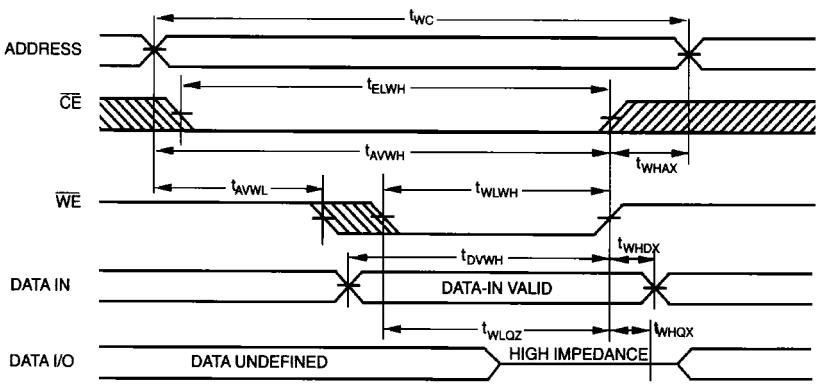
READ CYCLE N° 1 (9, 10)



READ CYCLE N° 2 (9, 11)



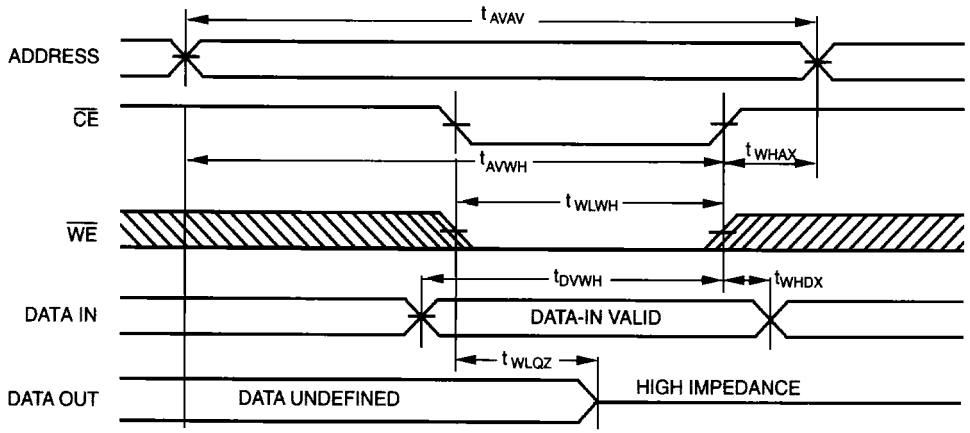
WRITE CYCLE N° 1 (WE Controlled) (8, 12)



Notes : 9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL} (65889 $\overline{OE}$ = V_{IL} also).
11. Address valid prior to or coincident with $\overline{CE}$ transition low.
12. 65889 only : Data I/O will be high impedance if $\overline{OE}$ = V_{IH}.
13. If CE goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remain in a high-impedance state.

SWITCHING WAVEFORMS (continued)

WRITE CYCLE N° 2 ($\overline{CE}$ controlled) (8, 12, 13)



65888 TRUTH TABLE

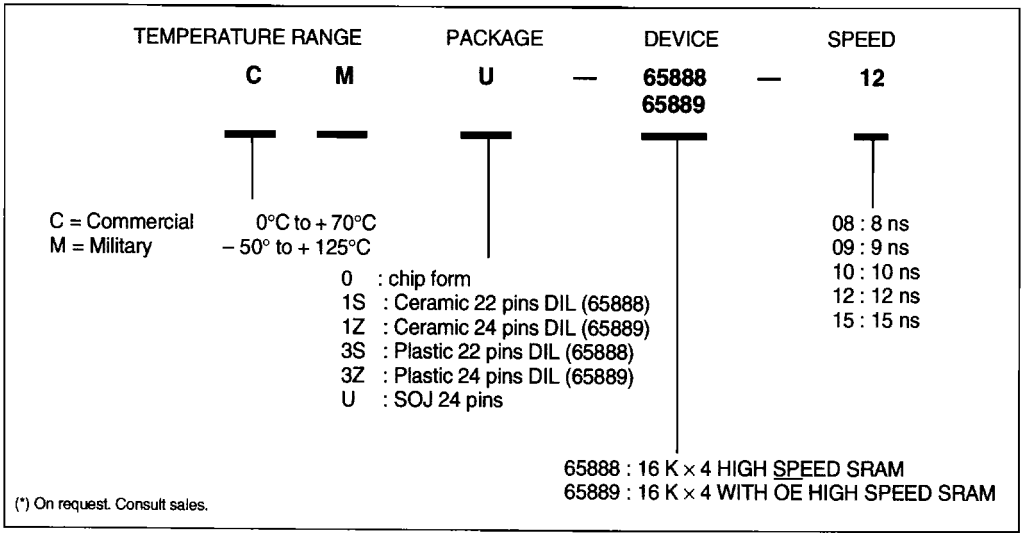
$\overline{CE}$	$\overline{WE}$	INPUTS/OUTPUT	MODE
H	X	High Z	Deselect/ Power-Down
L	H	Data Out	Read
L	L	Data In	Write

65889 TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	INPUTS/OUTPUT	MODE
H	X	X	High Z	Deselect/ Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

6

ORDERING INFORMATION



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