MOTOROLA

MC74AC253
MC74ACT253

Product Preview

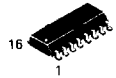
Dual 4-Input Multiplexer with 3-State Outputs

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The MC74AC253/74ACT253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

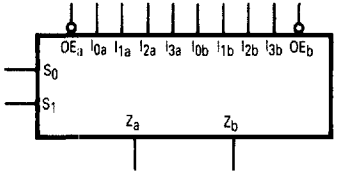
- Multifunctional Capability
- Noninverting 3-State Outputs
- Outputs Source/Sink 24 mA
- 'ACT253 Has TTL Compatible Inputs

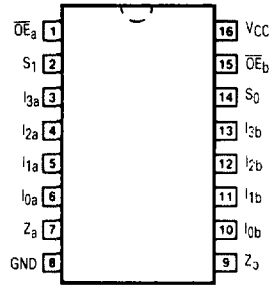
N SUFFIX
CASE 648-08
PLASTIC



D SUFFIX
CASE 751B-03
PLASTIC

LOGIC SYMBOL





PIN NAMES

I_{0a}–I_{3a}	Side A Data Inputs
I_{0b}–I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-State Outputs

TRUTH TABLE

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

FUNCTIONAL DESCRIPTION

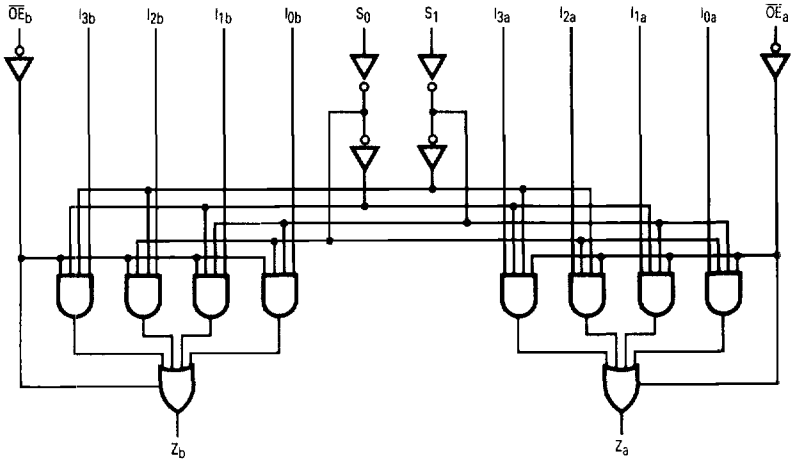
The MC74AC253/74ACT253 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC CHARACTERISTICS (unless otherwise specified)

Symbol	Parameter	Value	Units	Test Conditions
I_{CC}	Maximum Quiescent Supply Current	80	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	μA	V_{IN} = V_{CC} or Ground, V_{CC} = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT253)	1.5	mA	V_{IN} = V_{CC} − 2.1 V, V_{CC} = 5.5 V, T_A = Worst Case

AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	8.5 6.5	15.5 11	1.0 1.0	17.5 12.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	3.3 5.0	1.0 1.0	9.5 7.0	16 11.5	1.0 1.0	18 13	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.0 5.5	14.5 10	1.0 1.0	17 11.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	3.3 5.0	1.0 1.0	7.5 5.5	13 9.5	1.0 1.0	15 11	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	4.5 3.5	8.0 6.0	1.0 1.0	8.5 6.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	5.0 3.5	8.0 6.0	1.0 1.0	9.0 7.0	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.5 5.0	9.5 8.0	1.0 1.0	10 8.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	5.0 4.0	8.0 7.0	1.0 1.0	9.0 7.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC CHARACTERISTICS (For Figures and Waveforms — See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C, C_L = 50 pF			74ACT T_A = −40°C to +85°C, C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	13	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.5	13	1.0	14.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	10	1.0	11	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	6.5	11	1.0	12.5	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.0	8.0	1.0	9.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.0	9.5	1.0	10	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	7.5	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Units	Test Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	50	pF	V_{CC} = 5.0 V

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