- **Members of the Texas Instruments**
  Widebus ™ **Family**

- **Inputs Are TTL-Voltage Compatible**

- **Inverting Logic**

- **Flow-Through Architecture Optimizes**
  PCB Layout

- **Distributed V_{CC} and GND Pin Configuration**
  Minimizes High-Speed Switching Noise

- *EPIC* ™ **(Enhanced-Performance Implanted**
  CMOS) 1-µm Process

- **500-mA Typical Latch-Up Immunity at**
  125°C

- **Package Options Include Plastic 300-mil**
  Shrink Small-Outline (DL) Packages Using
  25-mil Center-to-Center Pin Spacings and
  380-mil Fine-Pitch Ceramic Flat (WD)
  Packages Using 25-mil Center-to-Center
  Pin Spacings

54ACT16620 . . . WD PACKAGE
74ACT16620 . . . DL PACKAGE
(TOP VIEW)

1OEAB	1	48	1$\overline{\text{OEBA}}$
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2OEAB	24	25	2$\overline{\text{OEBA}}$

description

The 'ACT16620 are inverting 16-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.
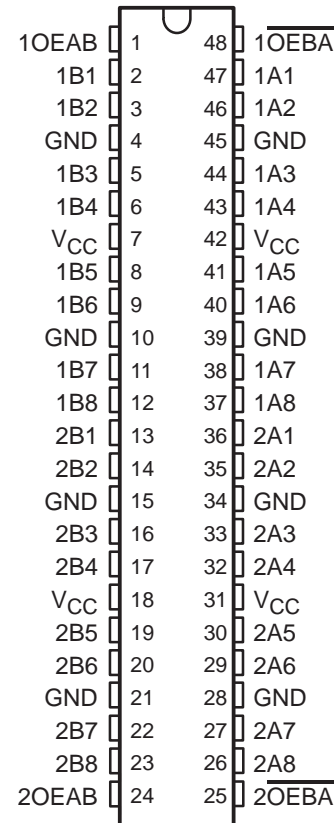
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. They allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the output-enable (OEAB or $\overline{\text{OEBA}}$) inputs. The output-enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the transceiver the capability to store data by simultaneously enabling OEAB and $\overline{\text{OEBA}}$. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, the bus lines remain at their last states.

The 74ACT16620 is packaged in TI's shrink small-outline package, which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54ACT16620 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74ACT16620 is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{\text{OEBA}}$	OEAB	
L	L	$\overline{\text{B}}$ data to A bus
L	H	$\overline{\text{B}}$ data to A bus, $\overline{\text{A}}$ data to B bus
H	L	Isolation
H	H	$\overline{\text{A}}$ data to B bus

logic symbol†
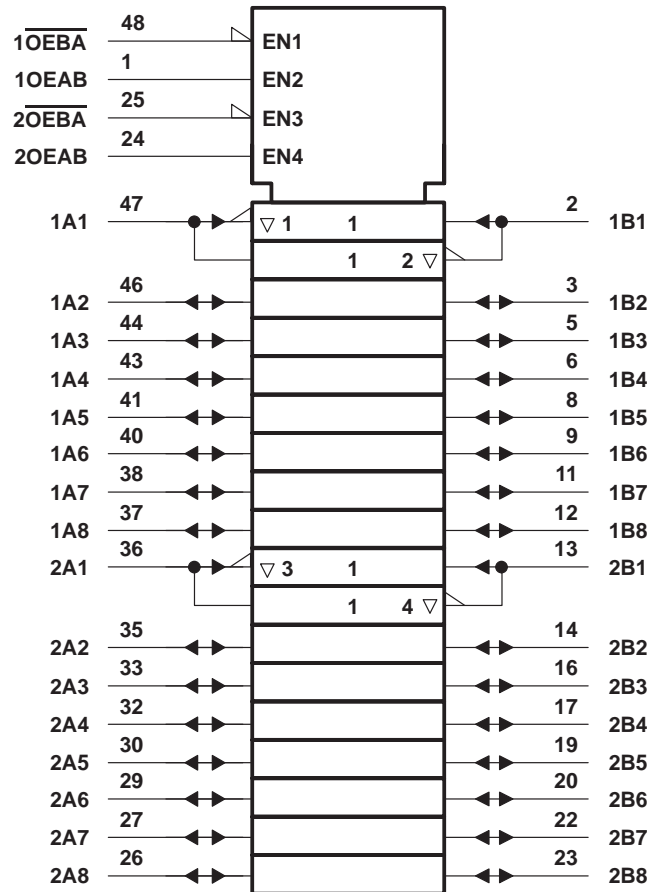
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

TEXAS
INSTRUMENTS
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logic diagram (positive logic)

To Seven Other Channels   **To Seven Other Channels**
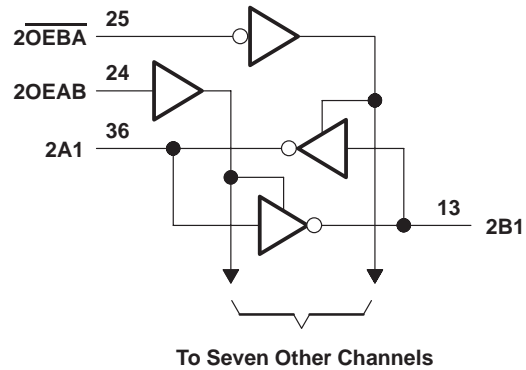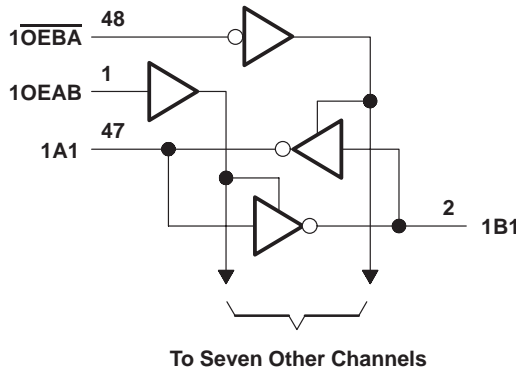
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±400 mA
Maximum package power dissipation at $T_A = 55°C$ (in still air) (see Note 2): DL package .... 1.2 W
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

		54ACT16620			74ACT16620			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			24			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54ACT16620		74ACT16620		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50\ \mu A$	4.5 V	4.4			4.4		4.4		V
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -24\ mA$	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		$I_{OH} = -75\ mA†$	5.5 V				3.85		3.85		
V_{OL}		$I_{OL} = 50\ \mu A$	4.5 V			0.1		0.1		0.1	V
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 24\ mA$	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		$I_{OL} = 75\ mA†$	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V			±0.1		±1		±1	μA
$I_{OZ}‡$	A or B ports	$V_O = V_{CC}$ or GND	5.5 V			±0.5		±5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80		80	μA
$\Delta I_{CC}§$		One input at 3.4 V, Other inputs at V_{CC} or GND	5.5 V			0.9		1		1	mA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		4						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		15						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 5\ V \pm 0.5\ V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25°C$			54ACT16620		74ACT16620		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	5	7.7	2	8.5	2	8.5	ns
t_{PHL}			4	7	9.3	4	10.5	4	10.5	
t_{PZH}	$\overline{OEBA}$	A	2.2	5.5	8.3	2.2	9.1	2.2	9.1	ns
t_{PZL}			2.8	6.4	10	2.8	10.9	2.8	10.9	
t_{PHZ}	$\overline{OEBA}$	A	6	8.8	11	6	11.9	6	11.9	ns
t_{PLZ}			5.1	7.9	10	5.1	10.6	5.1	10.6	
t_{PZH}	OEAB	B	3.6	6.2	7.9	3.6	8.9	3.6	8.9	ns
t_{PZL}			4.4	7.1	9.4	4.4	10.5	4.4	10.5	
t_{PHZ}	OEAB	B	5	7.8	10.1	5	10.8	5	10.8	ns
t_{PLZ}			4.1	6.7	9.1	4.1	9.6	4.1	9.6	

operating characteristics, $V_{CC} = 5\ V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 50\ pF$, f = 1 MHz	57	pF
		Outputs disabled		10	

![Texas Instruments logo]

PARAMETER MEASUREMENT INFORMATION
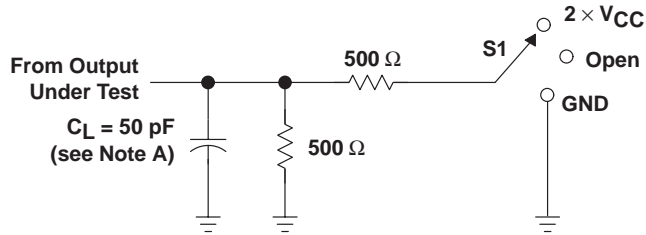
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
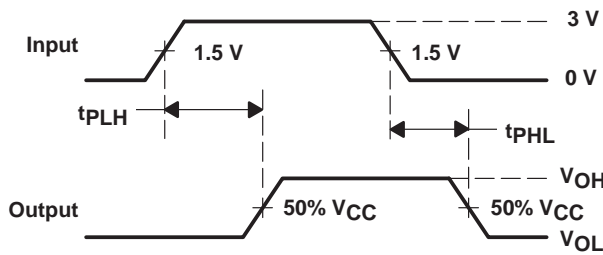
VOLTAGE WAVEFORMS
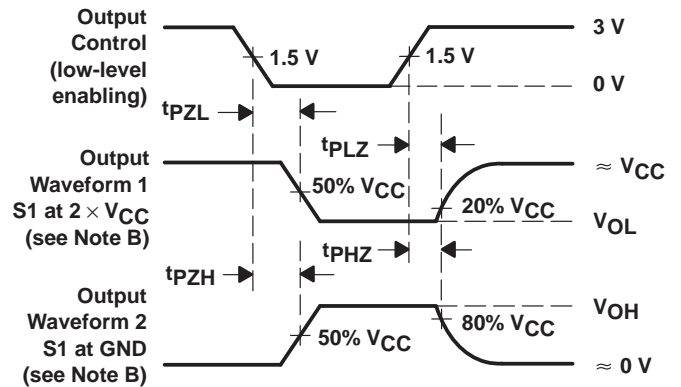
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74ACT16620DL	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI
74ACT16620DLR	OBSOLETE	SSOP	DL	48		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265