



rev 1.1

Features

- FCC approved method of EMI attenuation.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input frequency range: 18MHz to 35MHz.
- Internal loop filter minimizes external components and board space.
- Frequency deviation: Maximum $\pm 1\%$.
- Low cycle-to-cycle jitter.
- 5.0V $\pm 5\%$ operating voltage range.
- TTL or CMOS compatible outputs.
- Ultra-low power CMOS design.
- Available in 8-pin SOIC package.

Product Description

The ASM3P2106A is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies from 18MHz to 35MHz. The ASM3P2106A can generate an EMI reduced clock from crystal, ceramic resonator, or system clock. The ASM3P2106A offers frequency deviation of $\pm 1\%$.

The ASM3P2106A reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The ASM3P2106A allows significant system cost

savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

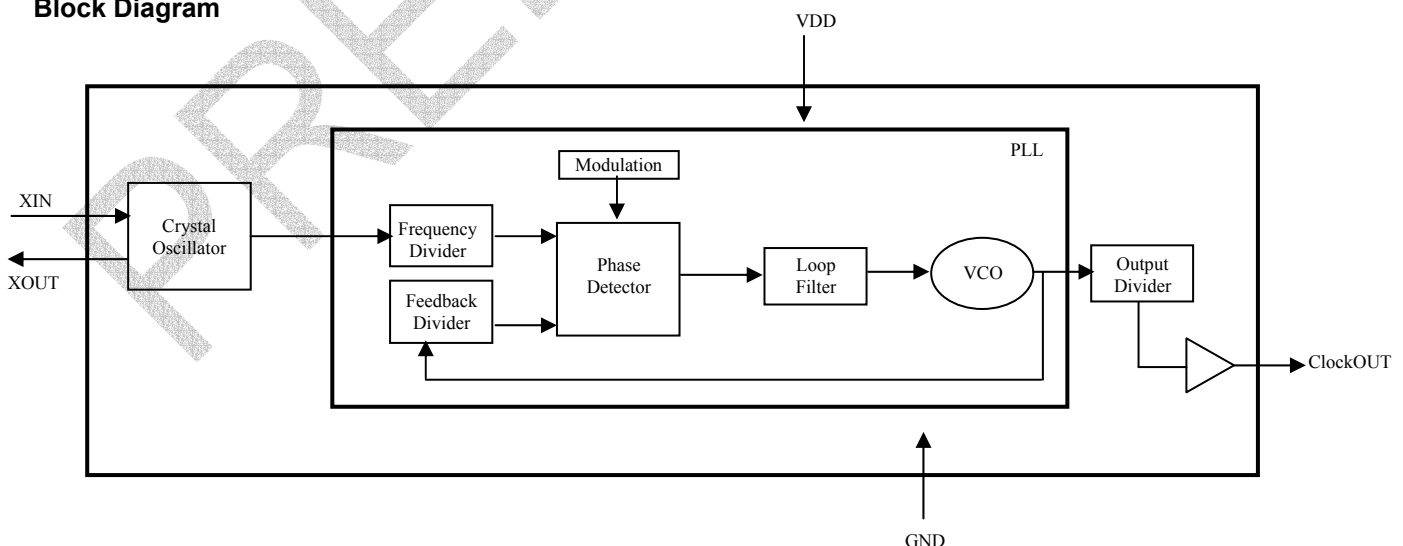
The ASM3P2106A uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The ASM3P2106A modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

Applications

The ASM3P2106A is targeted towards EMI management for high speed digital applications such as PC peripheral devices, consumer electronics and embedded controller systems.

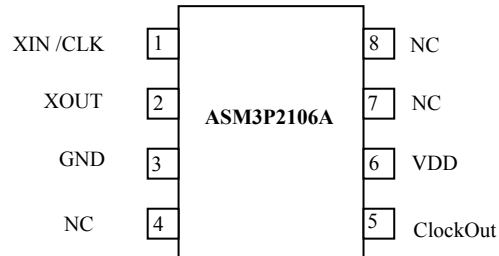
Block Diagram





rev 1.1

Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	XIN/CLK	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected to either an external crystal or an external reference clock.
2	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.
3	GND	P	Ground to entire chip.
4	NC	-	No connect.
5	ClockOut	O	Spread spectrum low EMI output.
6	VDD	P	Power supply for the entire chip (5V).
7	NC	-	No connect.
8	NC	-	No connect.



rev 1.1

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	-0.5 to + 7.0	V
T_{STG}	Storage temperature	-65 to +125	°C
T_A	Operating temperature	0 to 70	°C

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input low voltage	GND – 0.3	-	0.8	V
V_{IH}	Input high voltage	2.0	-	$V_{DD} + 0.3$	V
I_{IL}	Input low current (pull-up resistors on inputs SR0 and DIV2)		44		μA
I_{IH}	Input high current (pull-down resistor on input SSON#)		66		μA
I_{XOL}	X_{OUT} output low current (@ 4.0V, $V_{DD} = 5V$)		3		mA
I_{XOH}	X_{OUT} output high current (@2.5V, $V_{DD} = 5V$)		3		mA
V_{OL}	Output low voltage ($V_{DD} = 5V$, $I_{OL} = 20mA$)			0.4	V
V_{OH}	Output high voltage ($V_{DD} = 5V$, $I_{OH} = 20mA$)	2.5			V
I_{CC}	Dynamic supply current normal mode (5V, 18MHz and 15pF loading)		40		mA
I_{DD}	Static supply current standby mode		40		μA
V_{DD}	Operating voltage	4.75	5.0	5.25	V
t_{ON}	Power up time (first locked clock cycle after power up)	-	0.18	-	mS
Z_{OUT}	Clock out impedance	-	50	-	Ω



rev 1.1

AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input frequency	18	-	35	MHz
MODOUT	Output frequency	18	-	35	MHz
t_{LH}^*	Output rise time (measured at 0.8V to 2.0V)	-	440	-	ps
t_{HL}^*	Output fall time (measured at 2.0V to 0.8V)	-	300	-	ps
t_{JC}	Jitter (cycle to cycle)	-	-	360	ps
t_D	Output duty cycle	45	50	55	%
* $V_{DD} = +5V$, Input Frequency = 18MHz, t_{LH} and t_{HL} are measured into a capacitive load of 15pF					

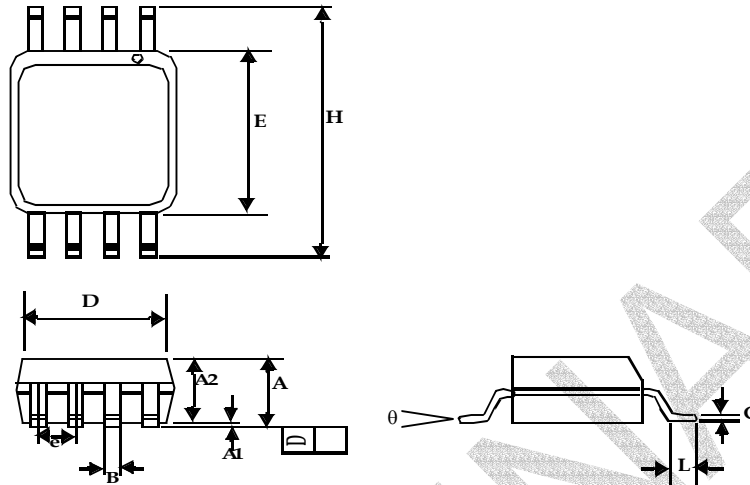
PRELIMINARY



rev 1.1

Package Information

8-Pin SOIC (Pb Free Parts)



Symbol	Dimensions in inches		Dimensions in millimeters	
	Min	Max	Min	Max
A	0.057	0.071	1.45	1.80
A1	0.004	0.010	0.10	0.25
A2	0.053	0.069	1.35	1.75
B	0.012	0.020	0.31	0.51
C	0.004	0.01	0.10	0.25
D	0.186	0.202	4.72	5.12
E	0.148	0.164	3.75	4.15
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.012	0.028	0.30	0.70
θ	0°	8°	0°	8°



rev 1.1

Ordering Codes

Part Number	Package	
ASM3P2106AF-08SR	8-PIN SOIC	TAPE AND REEL
ASM3P2106AF-08ST	8-PIN SOIC	TUBE

Device Ordering Information

A S M 3 P 2 1 0 6 A F - 0 8 S R

OR - SOT23/T/R	SR - SOIC, T/R
TT - TSSOP, TUBE	QR - QFN, T/R
TR - TSSOP, T/R	QT - QFN, TUBE
VT - TVSOP, TUBE	BT - BGA, TUBE
VR - TVSOP, T/R	BR - BGA, T/R
ST - SOIC, TUBE	

Pin Count

F = Pb FREE

PART NUMBER

X = Automotive	I = Industrial	P or n/c = Commercial
1 - reserved	6 - power management	
2 - Non PLL based	7 - power management	
3 - EMI Reduction	8 - power management	
4 - DDR support products	9 - Hi performance	
5 - STD Zero Delav Buffer	0 - reserved	

Alliance Semiconductor Mixed Signal Product

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.



rev 1.1



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Preliminary Information
Part Number: ASM3P2106A
Document Version: v1.1

Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Dan Hariton / Alliance Semiconductor, dated 11-11-2003

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