8-Bit Latches, 8-Bit Registers with Inverting Outputs
SN54/74LS533   SN54/74S533
SN54/74LS534   SN54/74S534

Features/Benefits
- Inverting outputs
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS373/4 or SN54/74S373/4 — can be direct replacement when bus polarity must be changed

Description
In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of non-inverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive-low bus.

The latch passes eight bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched"

Ordering Information

PART NUMBER	PKG	TEMP	POLARITY	TYPE	POWER
54LS533	J,W,L	Mil		Latch	LS
74LS533	N,J	Com			
54LS534	J,W,L	Mil		Register	
74LS534	N,J	Com	Invert		
54S533	J,W,L	Mil		Latch	S
74S533	N,J	Com			
54S534	J,W,L	Mil		Register	
74S534	N,J	Com			

when the gate (G) goes low. The register loads eight bits of input data and passes it to the output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{OE}$ is low, and high-impedance when $\overline{OE}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

Function Tables

'533 8-Bit Latch (Inverting)

$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'534 8-Bit Register (Inverting)

$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	H
L	↑	L	L
L	L or H or ↓	X	Q_0
H	X	X	Z

Logic Symbols

'533 8-Bit Latch (Inverting)
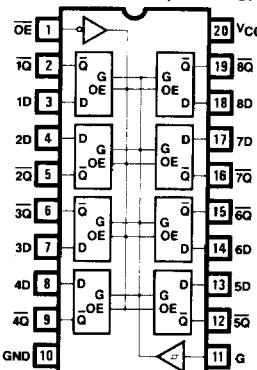
'533 8-Bit Register (Inverting)
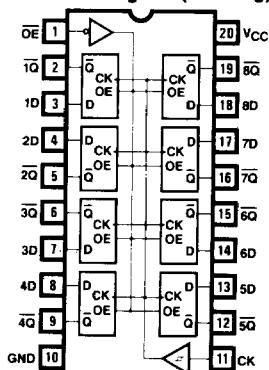
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Monolithic Memories MMI

IEEE Symbols

'S533

$\overline{OE}$ — 1	EN	
G — 11	G1	
1D — 3	1D	2 — $\overline{1Q}$
2D — 4		5 — $\overline{2Q}$
3D — 7		6 — $\overline{3Q}$
4D — 8		9 — $\overline{4Q}$
5D — 13		12 — $\overline{5Q}$
6D — 14		15 — $\overline{6Q}$
7D — 17		16 — $\overline{7Q}$
8D — 18		19 — $\overline{8Q}$

'S534

$\overline{OE}$ — 1	EN	
CK — 11	C1	
1D — 3	1D	2 — $\overline{1Q}$
2D — 4		5 — $\overline{2Q}$
3D — 7		6 — $\overline{3Q}$
4D — 8		9 — $\overline{4Q}$
5D — 13		12 — $\overline{5Q}$
6D — 14		15 — $\overline{6Q}$
7D — 17		16 — $\overline{7Q}$
8D — 18		19 — $\overline{8Q}$
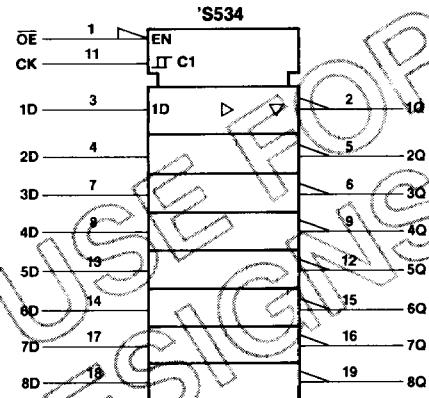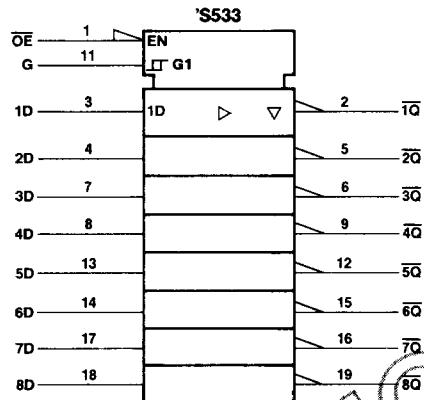
Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 7 V
Off-state output voltage .... 5.5 V
Storage temperature .... −65° to +150° C

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		−55		125	0		75	°C
t_w	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{su}	Setup time	LS533	3↓			3↓			ns
		LS534	20↑			20↑			
t_h	Hold time	LS533	10↓			10↓			ns
		LS534	0↑			0↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18mA				−1.5			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4V				−0.4			−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.7V				20			20	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 7V				0.1			0.1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	I_{OL} = 12mA			0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA						0.35	0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = 2V	I_{OH} = −1mA		2.4	3.4					V
			I_{OH} = −2.6mA					2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX V_{IL} = MAX V_{IH} = 2V	V_O = 0.4V							−20	μA
I_{OZH}			V_O = 2.7V				20			20	μA
I_{OS}	Output short-circuit current *	V_{CC} = MAX			−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX Outputs open	LS533			36	48		36	48	mA
			LS534			27	48		27	48	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS533			LS534			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{MAX}	Maximum Clock frequency					35	50		MHz
t_{PLH}	Data to Output delay			17	25				ns
t_{PHL}				12	25				ns
t_{PLH}	Clock/Gate to output delay	C_L = 45pF R_L = 667Ω		20	35		19	30	ns
t_{PHL}				18	35		15	30	ns
t_{PZL}	Output Enable delay			25	36		21	30	ns
t_{PZH}				17	30		20	30	ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 667Ω		18	29		18	29	ns
t_{PHZ}				16	24		16	24	ns

Absolute Maximum Ratings

Supply voltage V_{CC} .... 7 V
Input voltage .... 5.5 V
Off-state output voltage .... 5.5 V
Storage temperature .... –65° to +150°C

Operating Conditions

SYMBOL	PARAMETER		MILITARY			COMMERCIAL			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature		–55		125	0		75	°C
t_w	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			
t_{su}	Setup time	S533	0↓			0↓			ns
		S534	5↑			5↑			
t_h	Hold time	S533	10↓			10↓			ns
		S534	5↑			5↑			

↑↓ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition, ↓ for the high-to-low transition.

## Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IH}	High-level input voltage			2			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.2			–1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5V			–0.25			–0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			50			50	µA
I_I	Maximum input current	V_{CC} = MAX,	V_I = 5.5V			1			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 20mA			0.5			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = –2mA	2.4	3.4					V
			I_{OH} = –6.5mA				2.4	3.1		
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V	V_O = 0.5V			–50			–50	µA
I_{OZH}			V_O = 2.4V			50			50	µA
I_{OS}	Output short-circuit current *	V_{CC} = MAX		–40		–100	–40		–100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open	S533		105	160		105	160	mA
			S534		90	140		90	140	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)		S533			S534		UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	Maximum Clock frequency					75	100		MHz
t_{PLH}	Data to Output delay			9	18				ns
t_{PHL}				5	16				ns
t_{PLH}	Clock/Gate to output delay	C_L = 15pF R_L = 280Ω		12	22	11	20		ns
t_{PHL}				7	20	8	18		ns
t_{PZL}	Output Enable delay			11	20	11	20		ns
t_{PZH}				8	17	8	17		ns
t_{PLZ}	Output Disable delay	C_L = 5pF R_L = 280Ω		8	16	7	16		ns
t_{PHZ}				6	13	5	13		ns

Test Waveforms
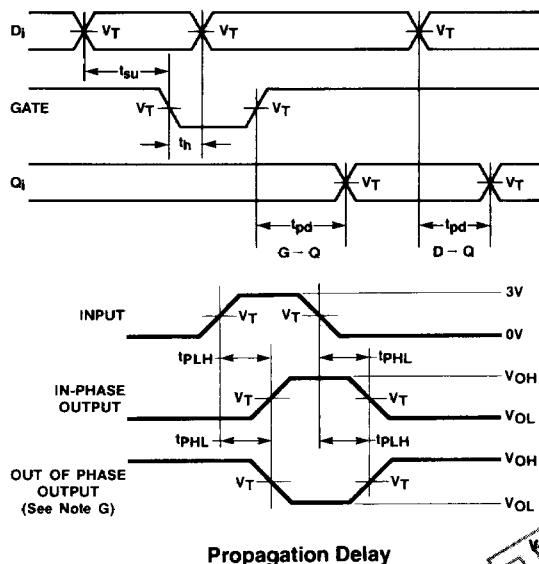
Propagation Delay
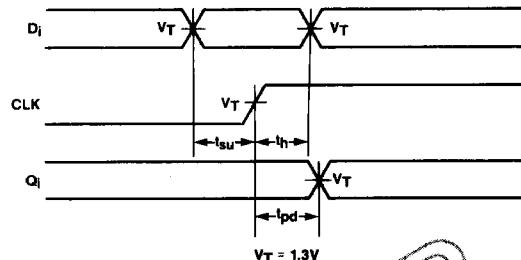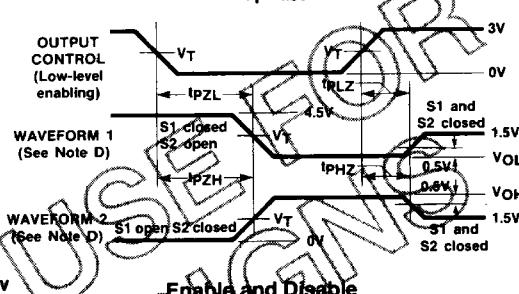
Enable and Disable

$V_T = 1.3V$

Test Load
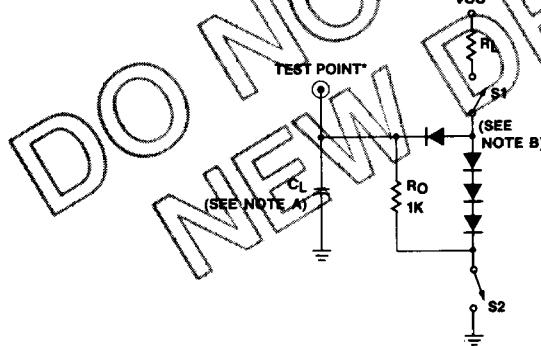
* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

NOTES: A. C_L includes probe and jig capacitance.

        B. All diodes are 1N916 or 1N3064.

        C. For Series 54/74S, R_O = 1K, V_T = 1.5 V.
           For Series 54/74LS, R_O = 5K, V_T = 1.3 V.

        D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

           Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

        E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

        F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{OUT} = 50Ω and:
           For Series 54/74S, t_R ≤ 2.5 ns, t_F ≤ 2.5 ns.
           For Series 54/74LS and PALs, t_R ≤ 15 ns. t_F ≤ 6 ns.

        G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.