DATA SHEET

NEC
ELECTRON DEVICE

PHOTO COUPLERS
PS2651 , PS2652
PS2651L2, PS2652L2

LONG CREEPAGE TYPE HIGH ISOLATION VOLTAGE 6PIN PHOTO COUPLER

DESCRIPTION

PS2651, PS2652 are optically coupled isolators containing a GaAs light emitting diode and an NPN silicon photo-transistor in a plastic DIP (Dual In-line Package).

PS2651 has base pin and PS2652 has no base pin.

Creepage distance and clearance of leads are over 8 millimeters.

PS2651L2, PS2652L2 are lead bending type (Gull-wing) for surface mounting.

FEATURES

- High isolation voltage (BV: 5 $kV_{r.m.s.}$ MIN.)
- Long creepage and clearance distance (8 mm MIN.)
- High collector to emitter voltage (V_{CEO}: 80 V MIN.)
- High speed switching (t_r = 3 μs, t_f = 5 μs TYP.)
- High current transfer ratio (CTR: 200 % TYP.)
- 6 pin Dual In-line Package

APPLICATIONS

Interface circuit for various instrumentations control equipments

- AC Line Digital Logic ..... Isolate high voltage transients
- Digital Logic Interface ..... Eliminate spurious ground loops
- Twisted Pair Line Receiver ..... Eliminate ground loop pick-up
- Telephone Telegraph Line Receiver ..... Isolate high voltage transients
- High Frequency Power Supply Feedback Control ... Maintain floating ground
- Relay Contact Monitor ..... Isolate floating grounds and transients
- Power Supply Monitor ..... Isolate transients and ground systems

ORDERING INFORMATION

ORDER CODE	PACKAGE	SAFETY STANDARD APPROVAL	QUALITY GRADE
PS2651 PS2652	6 pin DIP 6 pin DIP	Normal speck products · UL Approved · BSI Approved	Standard
PS2651L2 PS2652L2	6 pin DIP, lead bending type 6 pin DIP, lead bending type		
PS2651-V PS2652-V	6 pin DIP 6 pin DIP	VDE0884 speck products · VDE Approved · UL Approved · BSI Approved	Standard
PS2651L2-V PS2652L2-V	6 pin DIP, lead bending type 6 pin DIP, lead bending type		

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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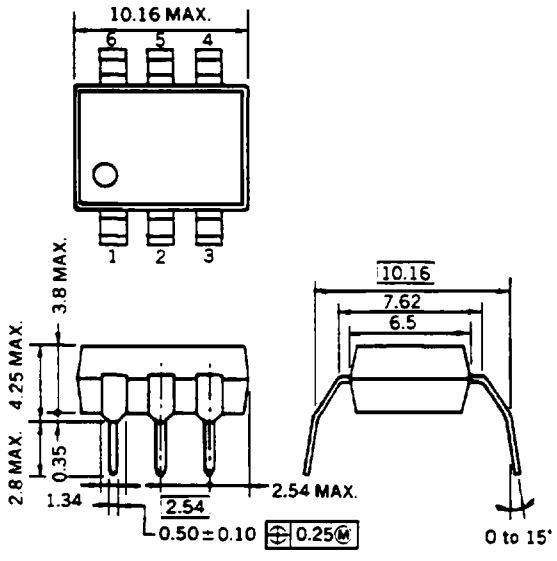
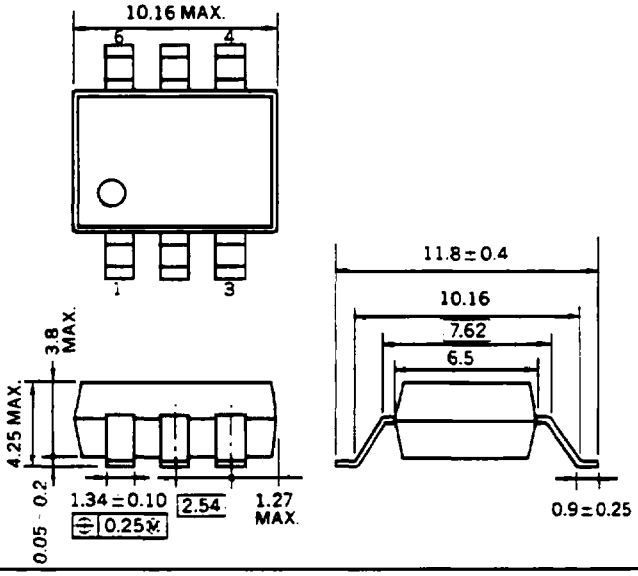
Printed in Japan

PACKAGE DIMENSIONS (Unit: mm)

PS2651
PS2652

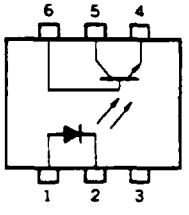


PS2651L2
PS2652L2



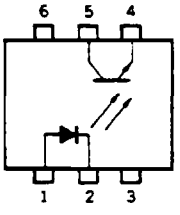
PIN CONNECTION (Top View)

PS2651
PS2651L2



1. Anode
2. Cathode
3. NC
4. Emitter
5. Collector
6. Base

PS2652
PS2652L2



1. Anode
2. Cathode
3. NC
4. Emitter
5. Collector
6. NC

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Diode			
Reverse Voltage	V_R	6	V
Forward Current (DC)	I_F	80	mA
Power Dissipation	P_D	150	mW
Peak Forward Current (PW = 100 μs, Duty Cycle 1 %)	$I_{F\ (Peak)}$	1	A
Transistor			
Collector to Emitter Voltage	V_{CEO}	80	V
Emitter to Collector Voltage	V_{ECO}	7	V
Collector Current	I_C	50	mA
Power Dissipation	P_C	150	mW
Coupled			
Isolation Voltage *1)	BV	5000	$V_{r.m.s.}$
Storage Temperature	T_{stg}	−55 to +150	°C
Operating Temperature	T_{opt}	−55 to +100	°C

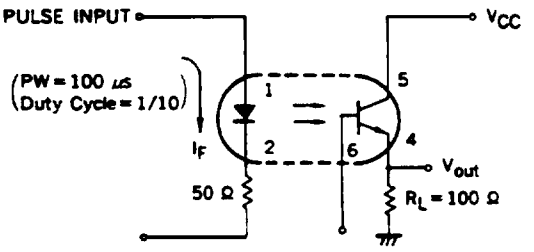
*1) AC voltage for 1 minute at T_a = 25 °C, RH = 60 % between input (Pin No. 1, 2, 3 Common) and output (Pin No. 4, 5, 6 Common).

ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

	PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Diode	Forward Voltage	V_F		1.1	1.4	V	I_F = 10 mA
	Reverse Current	I_R			5	μA	V_R = 5 V
	Junction Capacitance	C		30		pF	V = 0, f = 1.0 MHz
Transistor	Collector to Emitter Dark Current	I_{CEO}			100	nA	V_{CE} = 80 V, I_F = 0
	Collector to Emitter Breakdown Voltage	BV_{CEO}	80			V	I_C = 1 mA, I_B = 0
	Emitter to Collector Breakdown Voltage	BV_{ECO}	7			V	I_E = 100 μA, I_B = 0
Coupled	Current Transfer Ratio *2)	CTR	50	200	400	%	I_F = 5 mA, V_{CE} = 5 V
	Collector Saturation Voltage	$V_{CE\ (sat)}$			0.3	V	I_F = 10 mA, I_C = 2 mA
	Isolation Resistance	R_{1-2}	10^{11}			Ω	V_{in-out} = 1.0 kV
	Isolation Capacitance	C_{1-2}		0.6		pF	V = 0, f = 1.0 MHz
	Rise Time *3)	t_r		3		μs	V_{CC} = 5 V, I_C = 2 mA
	Fall Time *3)	t_f		5		μs	V_{CC} = 5 V, I_C = 2 mA

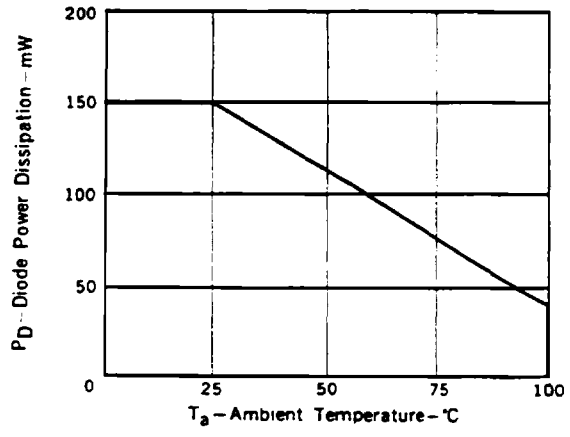
*2) CTR rank
- K : 160 to 400 (%)
- L : 80 to 240 (%)
- M : 50 to 120 (%)

*3) Test Circuit for Switching Time

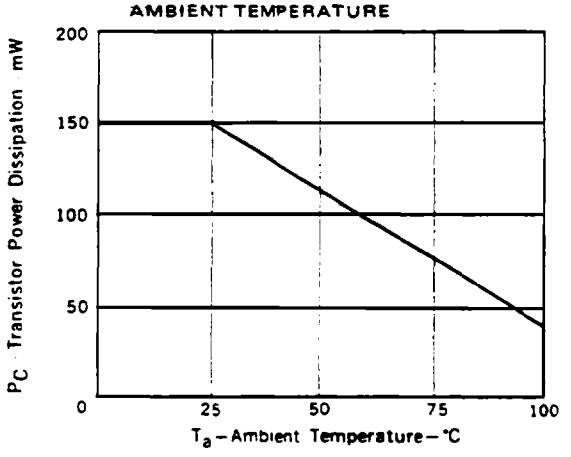


TYPICAL CHARACTERISTICS (T_a = 25 °C)

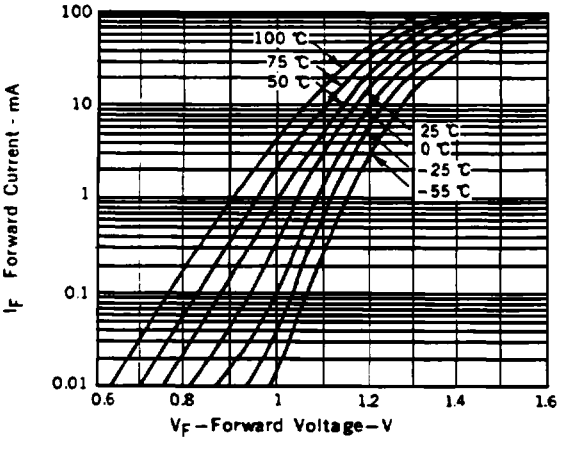
DIODE POWER DISSIPATION vs. AMBIENT TEMPERATURE



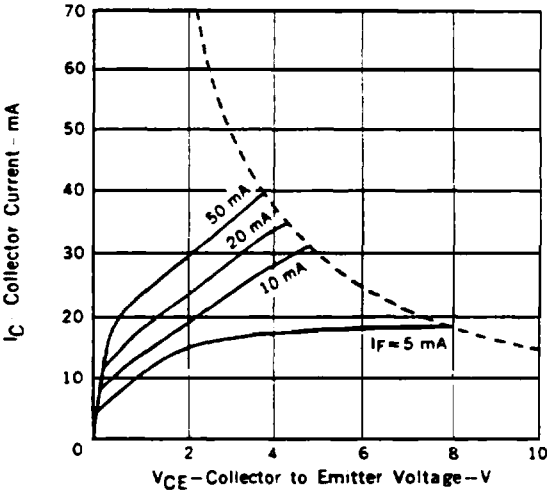
TRANSISTOR POWER DISSIPATION vs. AMBIENT TEMPERATURE



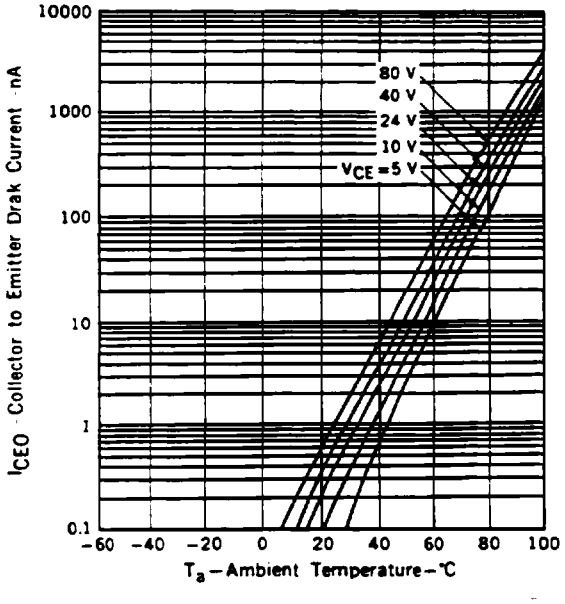
FORWARD CURRENT vs. FORWARD VOLTAGE



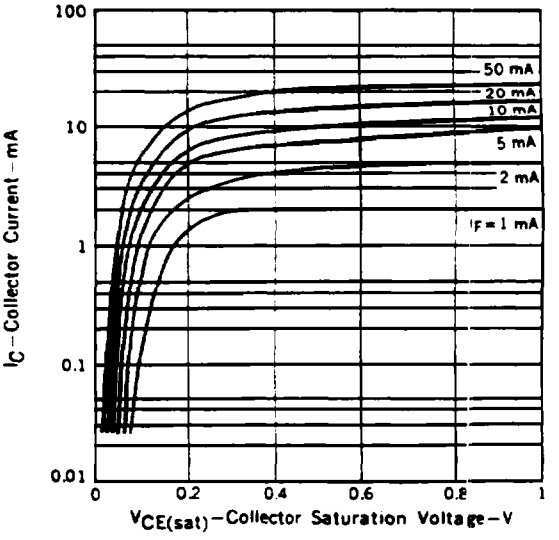
COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



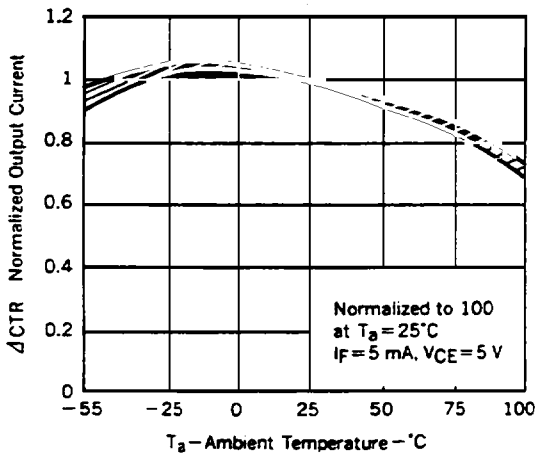
COLLECTOR TO EMITTER DARK CURRENT vs. AMBIENT TEMPERATURE



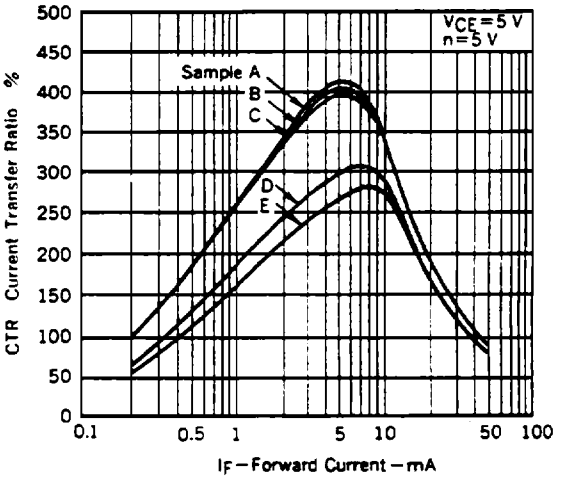
COLLECTOR CURRENT vs. COLLECTOR SATURATION VOLTAGE



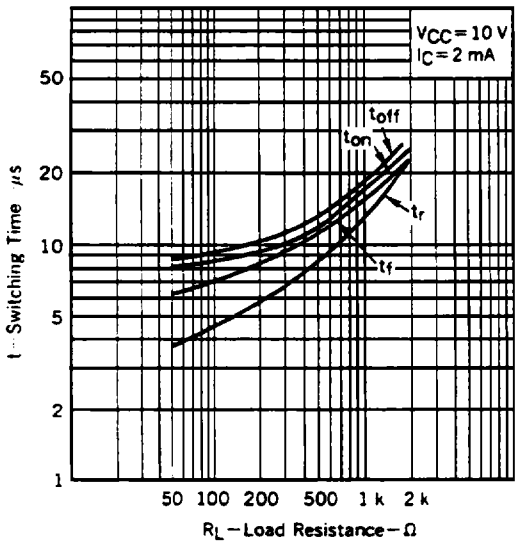
NORMALIZED OUTPUT CURRENT vs. AMBIENT TEMPERATURE



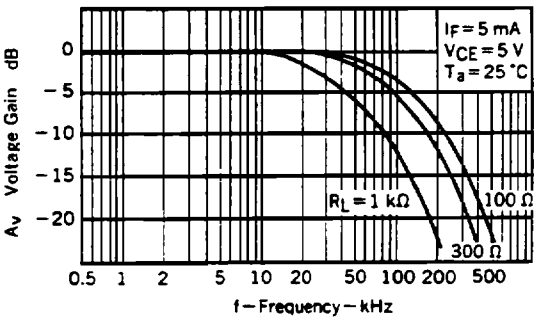
CURRENT TRANSFER RATIO (CTR) vs. FORWARD CURRENT



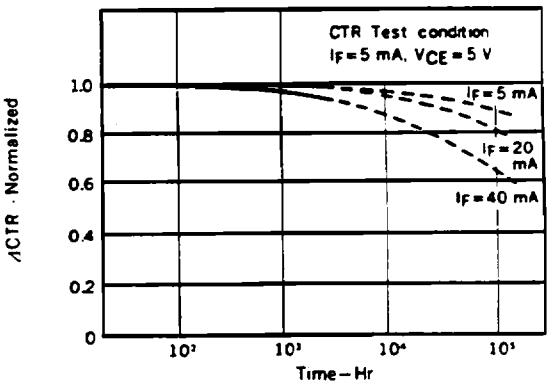
SWITCHING TIME vs. LOAD RESISTANCE



FREQUENCY RESPONSE



CTR DEGRADATION

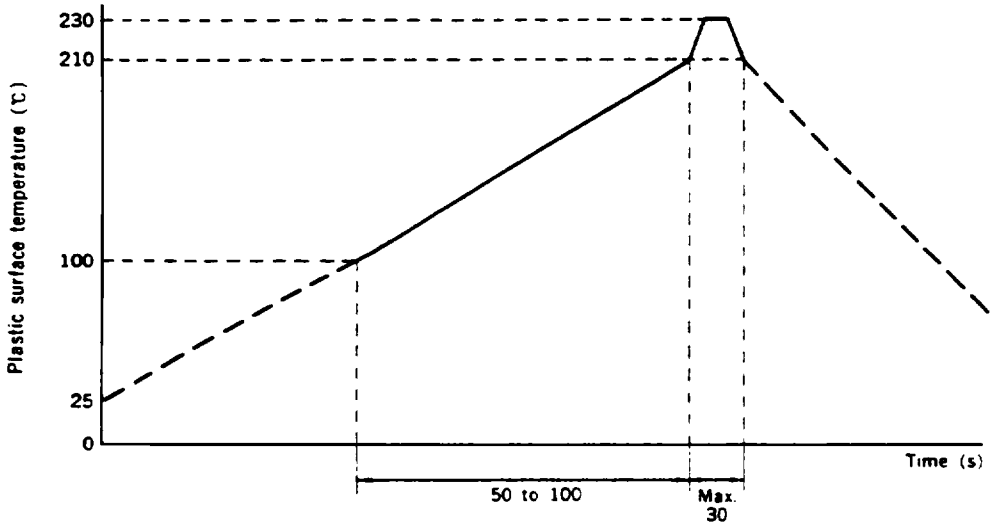


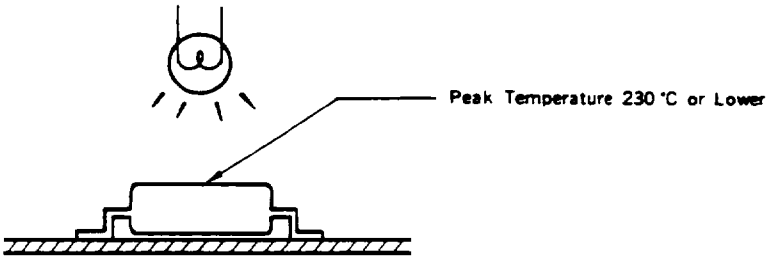
SOLDERING PRECAUTION

(1) Infrared reflow soldering

- Peak temperature : 230 °C or lower (plastic surface)
- Time : 30 s or less
  (Time during plastic surface temperature overs 210 °C)
- No. of reflow times : 1
- Flux : Rosin-base flux

Reflow Temperature Profile





(2) Dip soldering

- Peak temperature : 260 °C or lower
- Time : 10 s or less
- Flux : Rosin-base flux

SPECIFICATION OF VDE MARKS LICENSE DOCUMENT (VDE0884)

PARAMETER	SYMBOL	SPECK	UNIT
Application classification (DIN VDE 0109)			
for rated line voltages ≦ 300 V_{eff}		IV	
for rated line voltages ≦ 600 V_{eff}		III	
Climatic test class (DIN IEC 68 Teil 1/09.80)		55/100/21	
Dielectric strength			
maximum operating isolation voltage	U_{IORM}	890	Vpeak
Test voltage (partial discharge test Procedure a for type test and random test) $Upr = 1.2 \times U_{IORM}$, Pd < 5 pC	Upr	1 068	Vpeak
Test voltage (partial discharge test Procedure b for random test) $Upr = 1.6 \times U_{IORM}$, Pd < 5 pC	Upr	1 424	Vpeak
Highest permissible overvoltage	U_{TR}	8 000	Vpeak
Degree of pollution (DIN VDE 0109)		2	
Clearance distance		> 8.0	mm
Creepage distance[1]		> 8.0	mm
Comperative tracking index (DIN IEC 112/VDE 0303 part 1)	CTI	175	
Material group (DIN VDE 0109)		IIIa	
Storage temperature range	Tstg	−55 to +150	Cel
Operating temperature range	Tamb	−55 to +100	Cel
Isolation resistance, minimum value			
U_{IO} = 500 V dc at 25 Cel	Ris min	10^{12}	ohm
U_{IO} = 500 V dc at T_{amp} maximum at least 100 Cel	Ris min	10^{11}	ohm
Safety maximum ratings (maximum permissible in case of fault, see thermal derating curve)			
Package temperature	Tsi	175	Cel
Current (input current IF, P_{si} = 0)	Isi	400	mA
Power (output or total power dissipation)	Psi	700	mW
Isolation resistance U_{IO} = 500 V dc at 175 Cel (Tsi)	Ris min	10^{9}	ohm

[1] If a printed circuit is incorporated, the creepage distance and clearance may be reduced below this value (e.g. at a standard distance between soldering eye centers of 7.5 mm). If this is not permissible, the user shall take suitable measures.