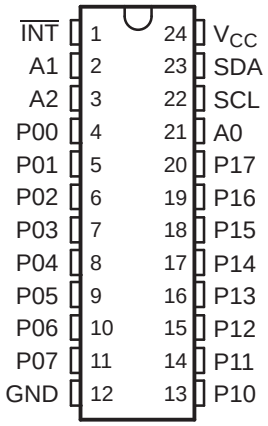
PCF8575C
REMOTE 16-BIT I²C AND SMBus LOW-POWER I/O EXPANDER WITH INTERRUPT OUTPUT

SCPS123E–MARCH 2005–REVISED OCTOBER 2007

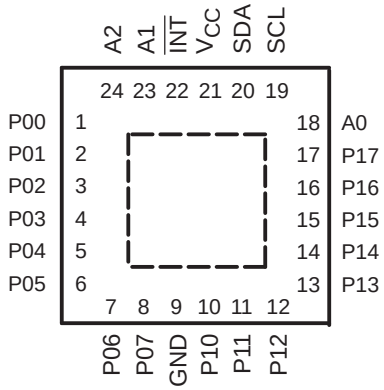
FEATURES

- **Low Standby-Current Consumption of 10 µA Maximum**
- **I²C to Parallel-Port Expander**
- **Open-Drain Interrupt Output**
- **Compatible With Most Microcontrollers**
- **400-kHz Fast I²C Bus**
- **Address by Three Hardware Address Pins for Use of up to Eight Devices**
- **Latched Outputs With High-Current Drive Capability for Directly Driving LEDs**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



RGE PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 16-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 4.5-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – DBQ	Reel of 2500	PCF8575CDBQR	PCF8575C
	TVSOP – DGV	Reel of 2000	PCF8575CDGVR	PF575C
	SOIC – DW	Tube of 25	PCF8575CDW	PCF8575C
		Reel of 2000	PCF8575CDWR	
	SSOP – DB	Tube of 60	PCF8575CDB	PF575C
		Reel of 2000	PCF8575CDBR	
	TSSOP – PW	Tube of 60	PCF8575CPW	PF575C
		Reel of 1200	PCF8575CPWR	
		Reel of 250	PCF8575CPWT	
	QFN – RGE	Reel of 3000	PCF8575CRGER	PF575C

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The PCF8575C provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07–P00, P17–P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are in 3-state mode. The strong pullup to V_{CC} allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set to 3-state, all of them can be used as inputs. Any change in setting of the I/Os as either inputs or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (I_{OL}) flows to GND.

The PCF8575C provides an open-drain interrupt ($\overline{INT}$) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time (t_{iv}), the signal $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit.

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I^2C bus. Thus, the PCF8575C can remain a simple slave device.

Every data transmission to or from the PCF8575C must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07–P00), and the second data byte in every pair refers to port 1 (P17–P10). To write to the ports (output mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 0. The PCF8575C acknowledges and the master sends the first data byte for P07–P00. After the first data byte is acknowledged by the PCF8575C, the second data byte (P17–P10) is sent by the master. Once again, the PCF8575C acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575C receives the pairs of data bytes, the first byte is referred to as P07–P00 and the second byte as P17–P10. The third byte is referred to as P07–P00, the fourth byte as P17–P10, and so on.

Before reading from the PCF8575C, all ports desired as input should be set to logic 1. To read from the ports (input mode), the master first addresses the slave device, setting the last bit of the byte containing the slave address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the master can read, this data may be lost.

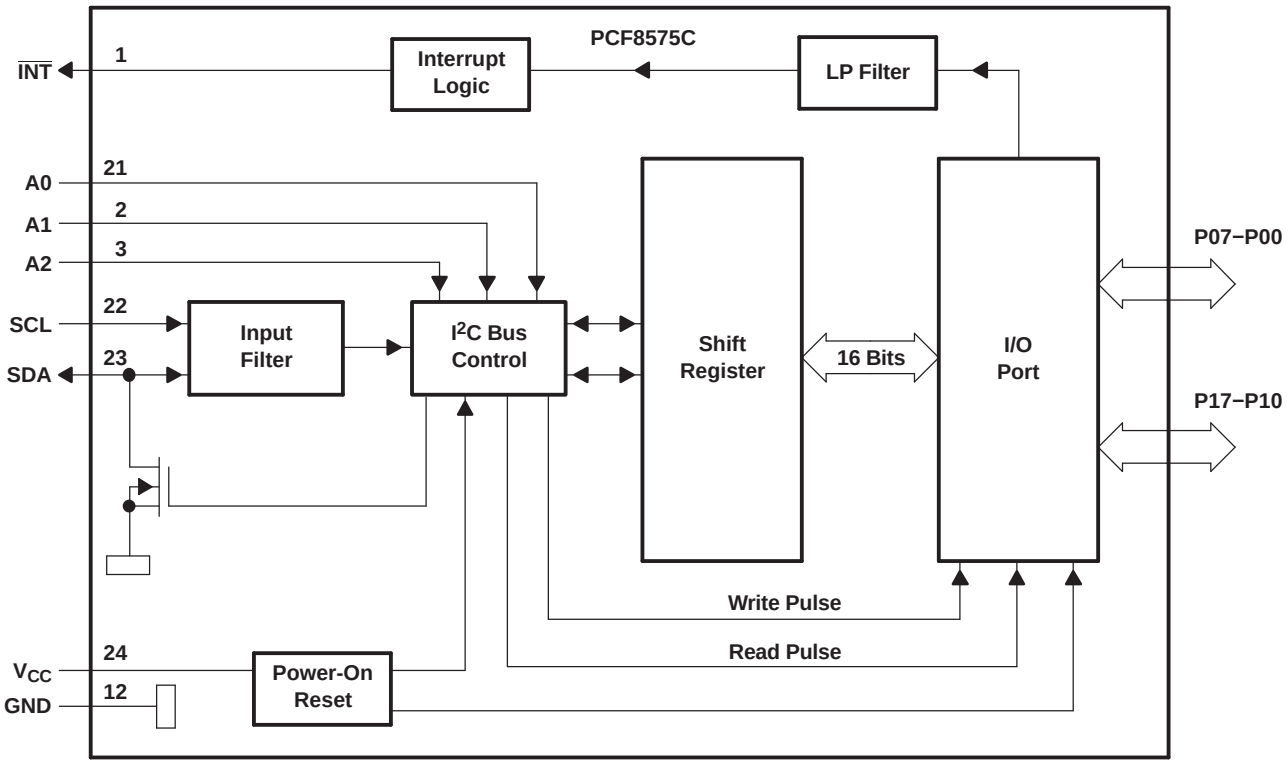
When power is applied to V_{CC}, an internal power-on reset holds the PCF8575C in a reset state until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the device I^2C-bus state machine initializes the bus to its default state.

The hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address, and allow up to eight devices to share the same I^2C bus or SMBus. The fixed I^2C address of the PCF8575C is the same as the PCF8575, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I^2C bus or SMBus.

TERMINAL FUNCTIONS

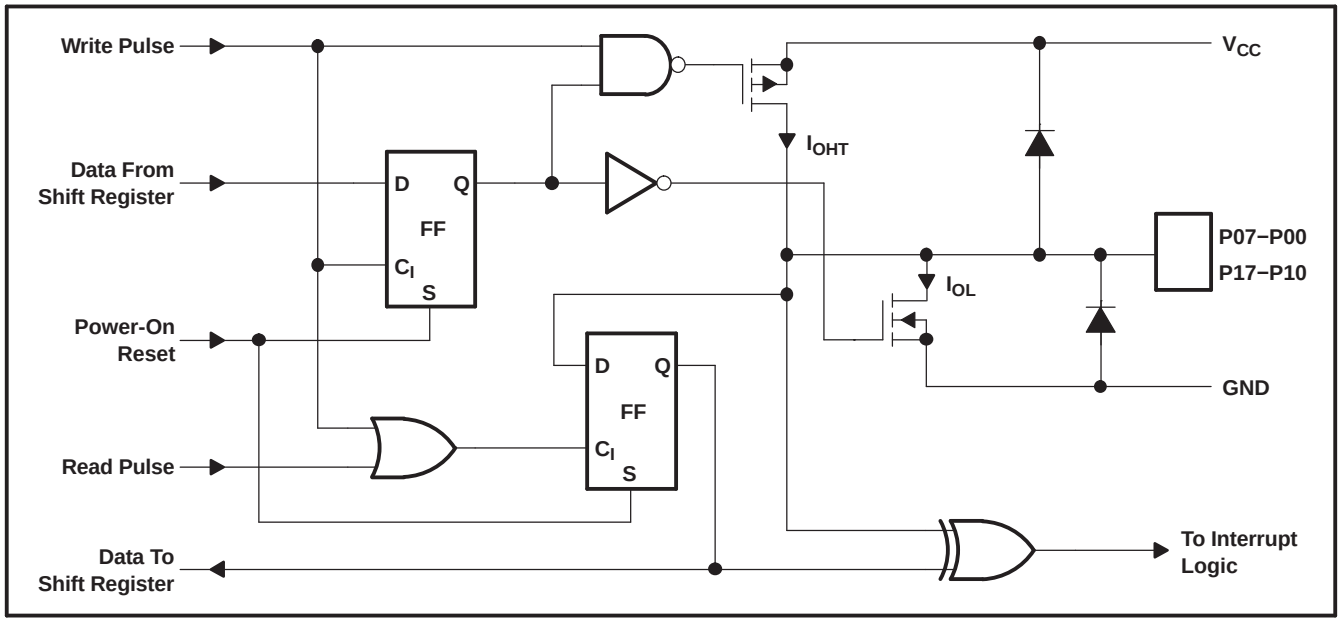
NO.		NAME	FUNCTION
DB, DBQ, DGV, DW, AND PW	RGE		
1	22	$\overline{INT}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	23	A1	Address input 1. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
3	24	A2	Address input 2. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
4	1	P00	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
5	2	P01	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
6	3	P02	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
7	4	P03	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
8	5	P04	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
9	6	P05	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
10	7	P06	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
11	8	P07	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
12	9	GND	Ground
13	10	P10	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
14	11	P11	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
15	12	P12	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
16	13	P13	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
17	14	P14	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
18	15	P15	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
19	16	P16	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
20	17	P17	P-port input/output. Open-drain design structure. Connect to V_{CC} through a pullup resistor.
21	18	A0	Address input 0. Connect directly to V_{CC} or ground. Pullup resistors are not needed.
22	19	SCL	Serial clock line. Connect to V_{CC} through a pullup resistor
23	20	SDA	Serial data line. Connect to V_{CC} through a pullup resistor.
24	21	V_{CC}	Supply voltage

LOGIC DIAGRAM (POSITIVE LOGIC)(A)



A. Pin numbers shown are for the DB, DBQ, DGV, DW, and PW packages.

SIMPLIFIED SCHEMATIC DIAGRAM OF EACH P-PORT INPUT/OUTPUT



I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/$\overline{W}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2–A0) of the slave device must not be changed between the start and the stop conditions.

The data byte follows the address ACK. If the R/$\overline{W}$ bit is high, the data from this device are the values read from the P port. If the R/$\overline{W}$ bit is low, the data are from the master, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the master, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (t_{pv}) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 2).

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. Also, a master must generate an ACK after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). Setup and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a stop condition.

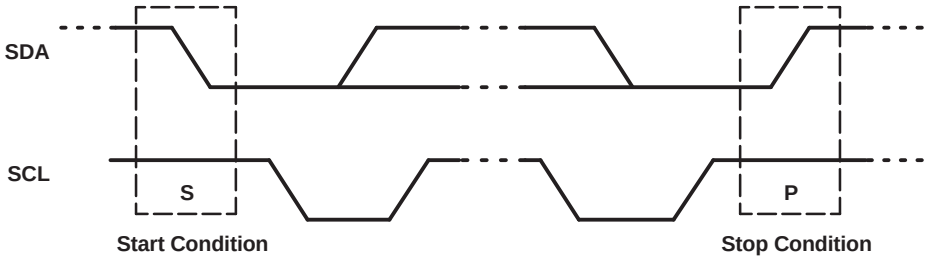


Figure 1. Definition of Start and Stop Conditions

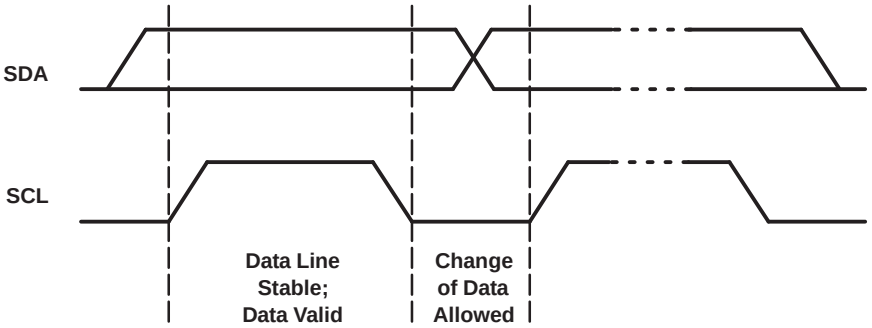


Figure 2. Bit Transfer

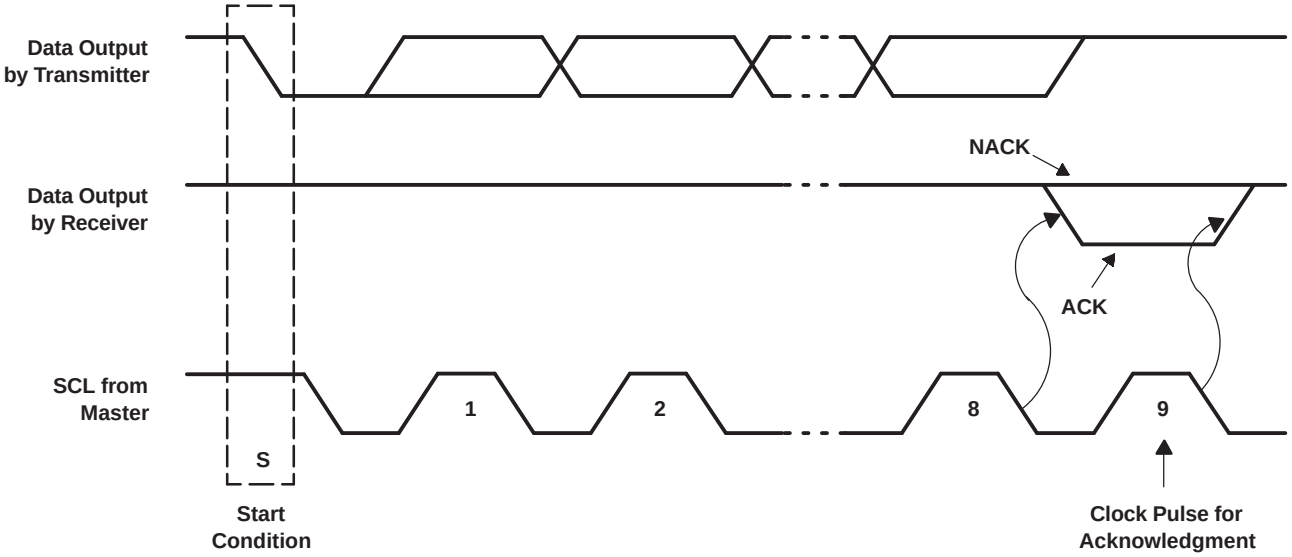


Figure 3. Acknowledgment on I²C Bus

Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I²C slave address	L	H	L	L	A2	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

Figure 4 and Figure 5 show the address and timing diagrams for the write and read modes, respectively.

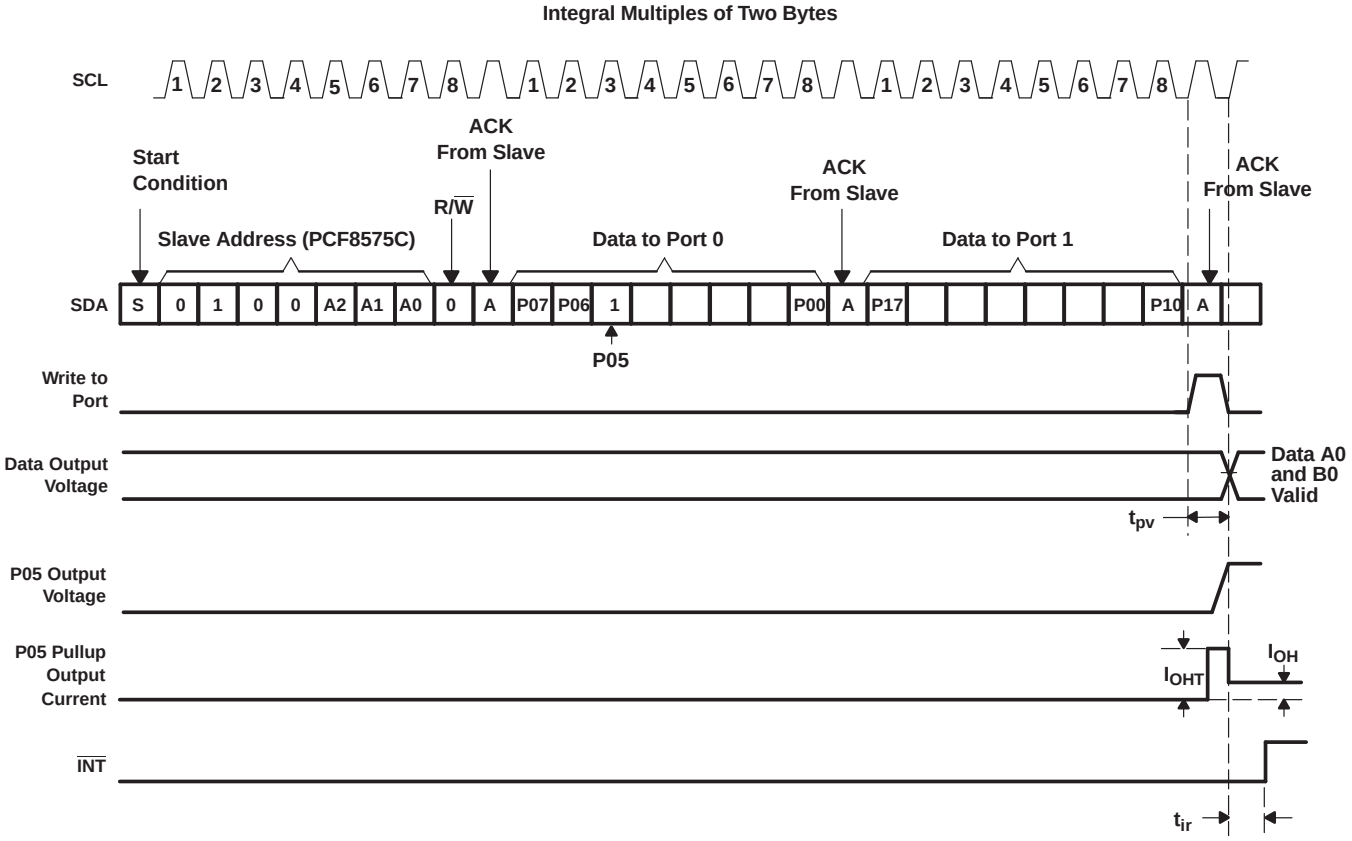
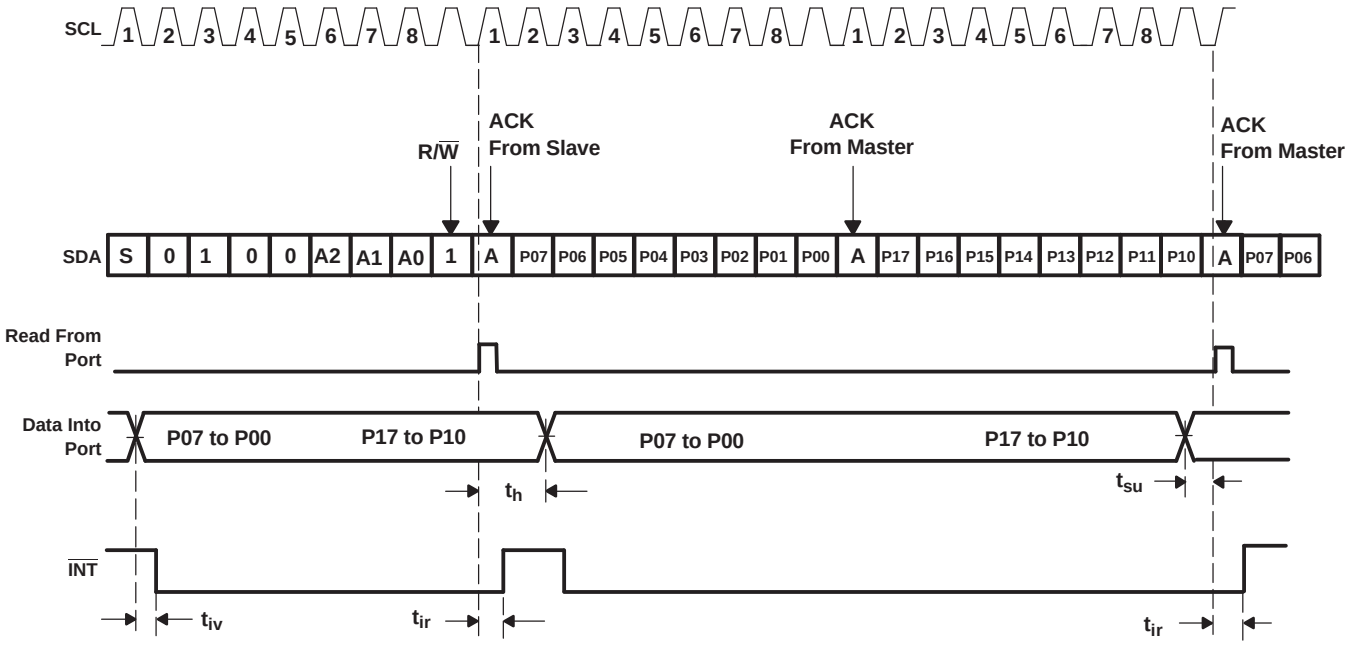


Figure 4. Write Mode (Output)



A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

Figure 5. Read Mode (Input)

Address Reference

INPUTS			I²C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	32 (decimal), 20 (hexadecimal)
L	L	H	33 (decimal), 21 (hexadecimal)
L	H	L	34 (decimal), 22 (hexadecimal)
L	H	H	35 (decimal), 23 (hexadecimal)
H	L	L	36 (decimal), 24 (hexadecimal)
H	L	H	37 (decimal), 25 (hexadecimal)
H	H	L	38 (decimal), 26 (hexadecimal)
H	H	H	39 (decimal), 27 (hexadecimal)

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0		–20	mA
I_{OK}	Input/output clamp current	V_O < 0 or V_O > V_{CC}		±400	µA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–4	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(3)	DB package		63	°C/W
		DBQ package		61	
		DGV package		86	
		DW package		46	
		PW package		88	
		RGE package		53	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage	A0, A1, A2, SDA, and SCL	0.7 × V_{CC}	V_{CC} + 0.5	V
		P07–P00 and P17–P10	0.8 × V_{CC}	V_{CC} + 0.5	
V_{IL}	Low-level input voltage	A0, A1, A2, SDA, and SCL	–0.5	0.3 × V_{CC}	V
		P07–P00 and P17–P10	–0.5	0.6 × V_{CC}	
I_{OHT}	P-port transient pullup current			–10	mA
I_{OL}	P-port low-level output current			25	mA
T_A	Operating free-air temperature		–40	85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	4.5 V to 5.5 V	–1.2			V
V_{POR}	Power-on reset voltage(2)	$V_I = V_{CC}$ or GND, I_O = 0	V_{POR}		1.2	1.8	V
I_{OHT}	P-port transient pullup current	High during ACK V_{OH} = GND	4.5 V	–0.5	–1		mA
I_{OL}	SDA	V_{OL} = 0.4 V	4.5 V to 5.5 V	3			mA
	P port	V_{OL} = 0.4 V	4.5 V to 5.5 V	5	15		
		V_{OL} = 1 V		10	25		
	$\overline{INT}$	V_{OL} = 0.4 V	4.5 V to 5.5 V	1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	4.5 V to 5.5 V			±2	µA
	A0, A1, A2					±1	
I_{IHL}	P port	$V_I \geq V_{CC}$ or $V_I \leq$ GND	4.5 V to 5.5 V			±400	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, f_{SCL} = 400 kHz	5.5 V		100	200	µA
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0, f_{SCL} = 0 kHz			2.5	10	
ΔI_{CC}	Supply current increase	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	4.5 V to 5.5 V			200	µA
C_i	SCL	$V_I = V_{CC}$ or GND	4.5 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	4.5 V to 5.5 V		3	7	pF
	P port				4	10	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The power-on reset circuit resets the I²C bus logic with $V_{CC} < V_{POR}$ and sets all I/Os to logic high (with current source to V_{CC}).

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6)

			MIN	MAX	UNIT
f_{scl}	I²C clock frequency			400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$(1)	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$(1)	300	ns
t_{ocf}	I²C output fall time (10-pF to 400-pF bus)			300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
t_{vd}	Valid-data time	SCL low to SDA output valid		1.2	µs
C_b	I²C bus capacitive load			400	pF

(1) C_b = total bus capacitance of one bus line in pF

Switching Characteristics

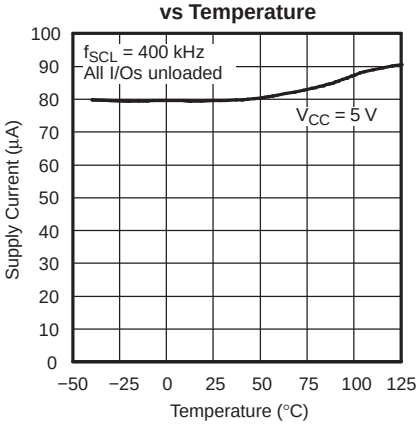
over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see Figure 7 and Figure 8)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P port		4	µs
t_{su}	Input data setup time	P port	SCL	0		µs
t_h	Input data hold time	P port	SCL	4		µs

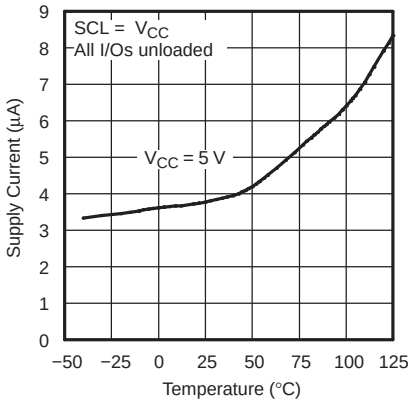
TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C (unless otherwise noted)

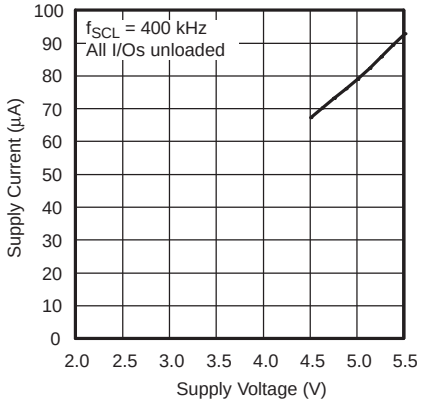
Supply Current vs Temperature



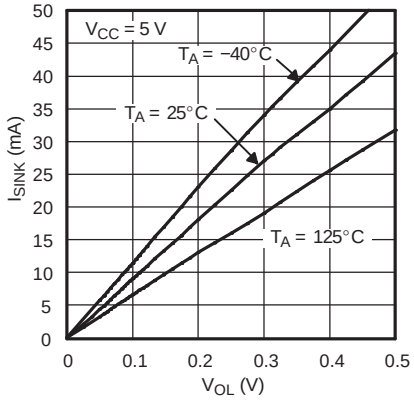
Standby Supply Current vs Temperature



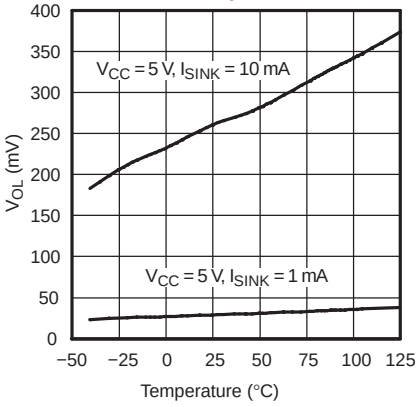
Supply Current vs Supply Voltage



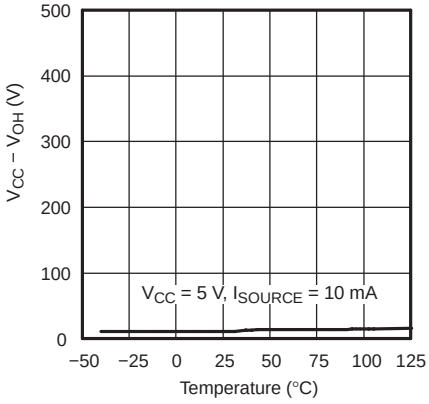
I/O Sink Current vs Output Low Voltage



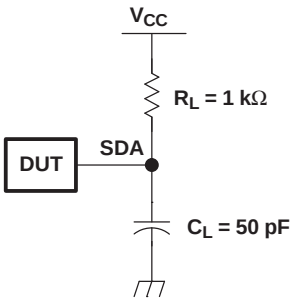
I/O Output Low Voltage vs Temperature



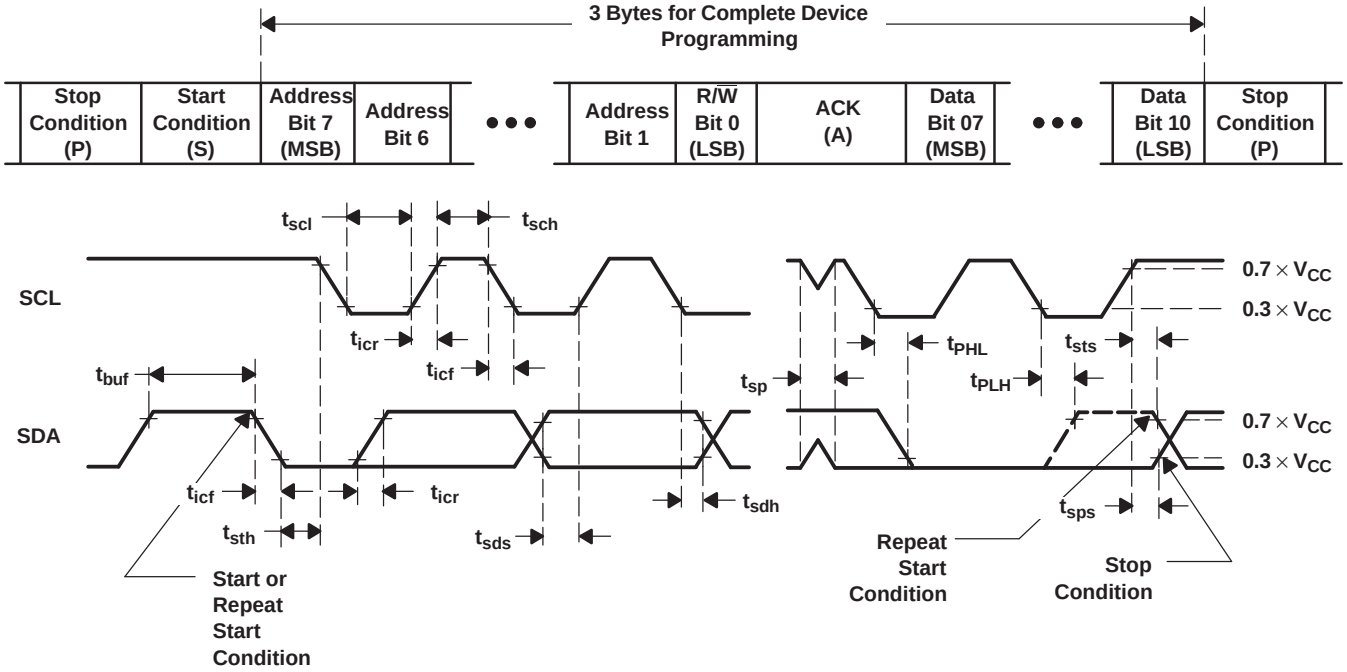
I/O High Voltage vs Temperature



PARAMETER MEASUREMENT INFORMATION



SDA LOAD CONFIGURATION

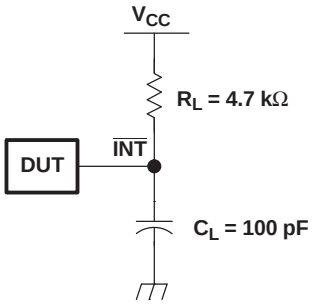


VOLTAGE WAVEFORMS

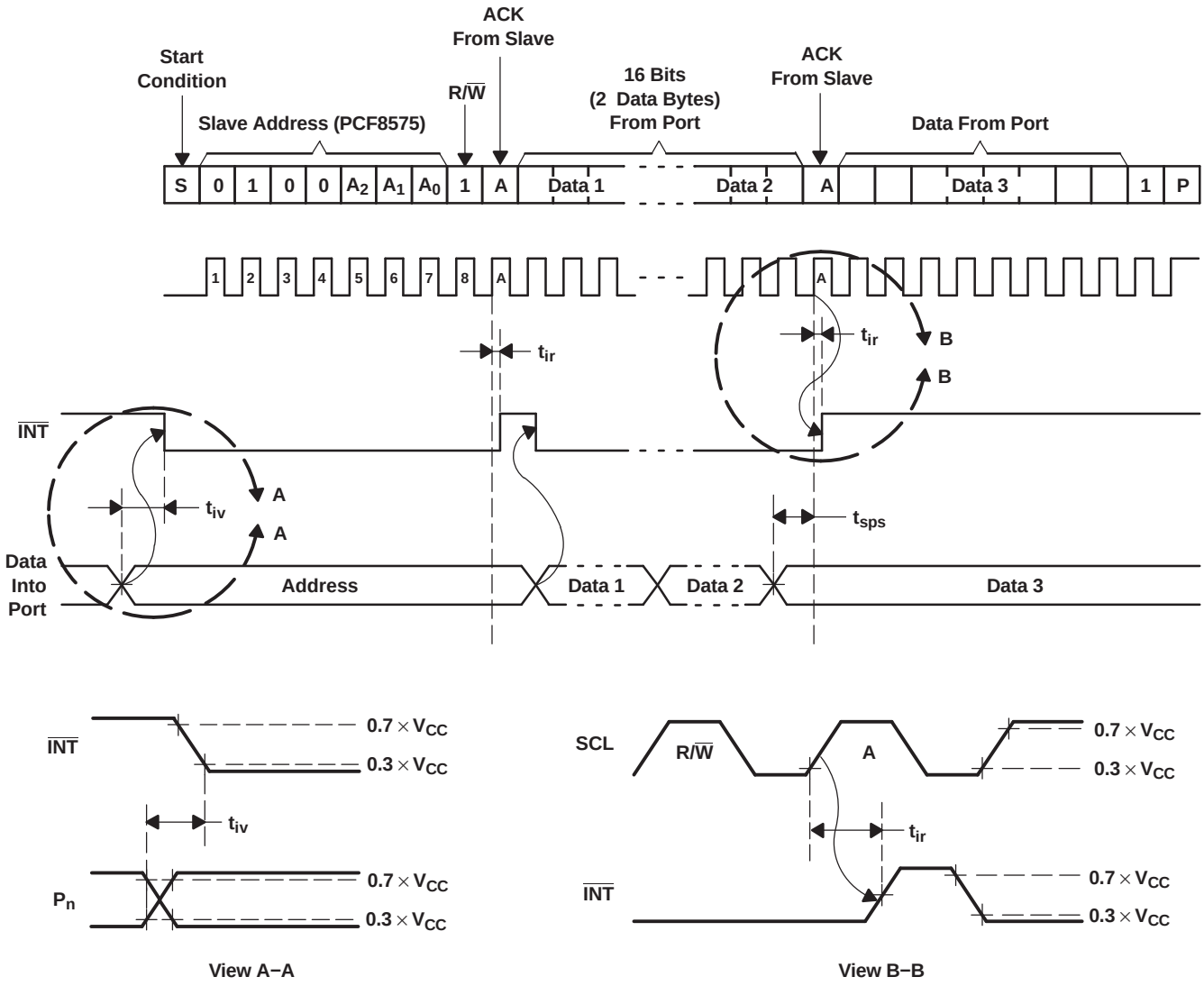
BYTE	DESCRIPTION
1	I²C address
2, 3	P-port data

Figure 6. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



INTERRUPT LOAD CONFIGURATION

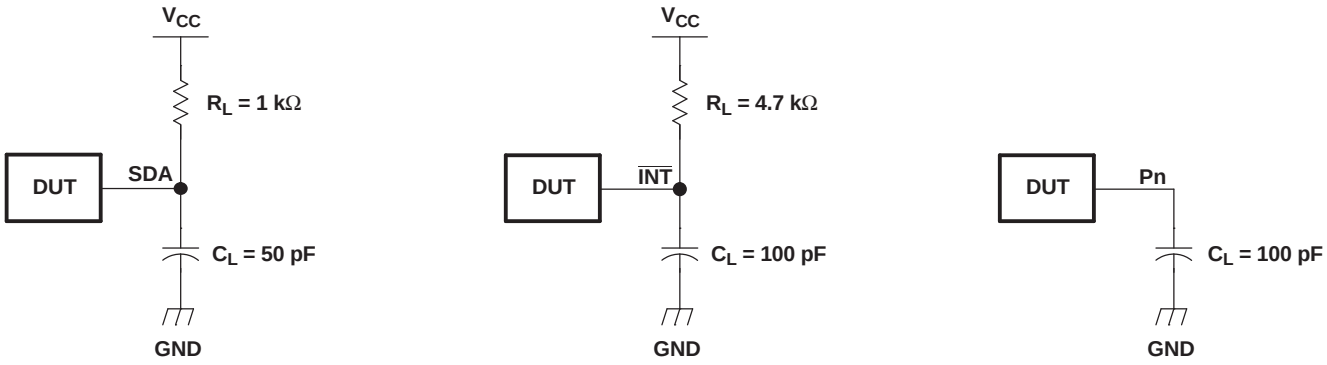


View A–A

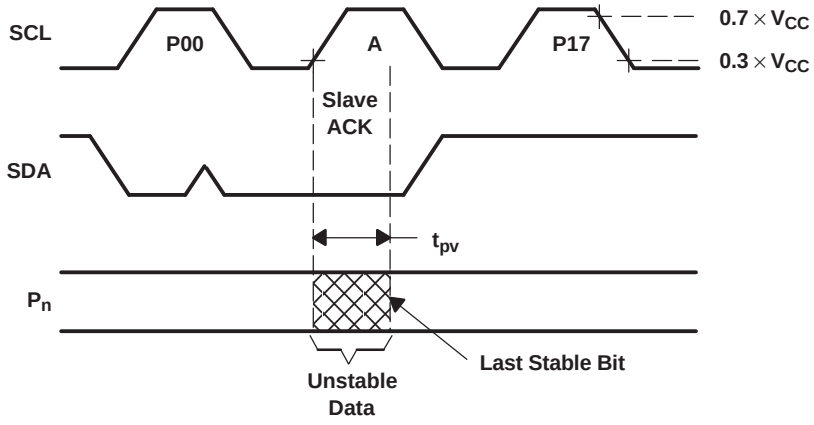
View B–B

Figure 7. Interrupt Load Circuit and Voltage Waveforms

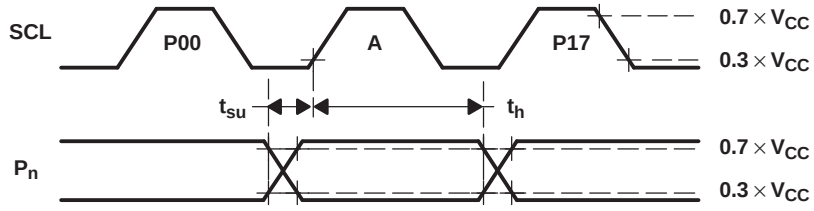
PARAMETER MEASUREMENT INFORMATION (continued)



SDA LOAD CONFIGURATION | INTERRUPT LOAD CONFIGURATION | P-PORT LOAD CONFIGURATION



Write-Mode Timing (R/$\overline{W}$ = 0)



Read-Mode Timing (R/$\overline{W}$ = 1)

Figure 8. P-Port Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575CDB	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CDBE4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CDBG4	ACTIVE	SSOP	DB	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575C	Samples
PCF8575CDBQRE4	ACTIVE	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDBQRG4	ACTIVE	SSOP	DBQ	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CDBRE4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDBRG4	ACTIVE	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CDGVRE4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDGVRG4	ACTIVE	TVSOP	DGV	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	Samples
PCF8575CDWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	Samples
PCF8575CDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	Samples
PCF8575CDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575C	Samples
PCF8575CDWRE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CDWRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575CPW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CPWE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CPWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575C	Samples
PCF8575CPWRE4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CPWRG4	ACTIVE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85		Samples
PCF8575CRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575C	Samples
PCF8575CRGERG4	ACTIVE	VQFN	RGE	24		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

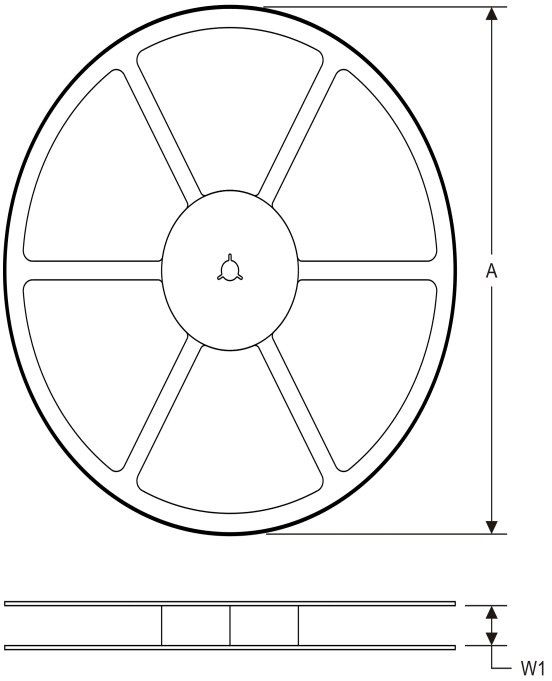
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

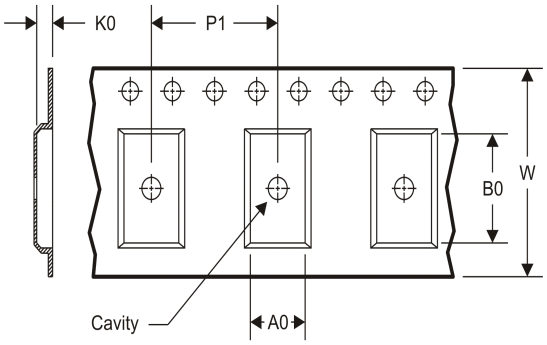
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



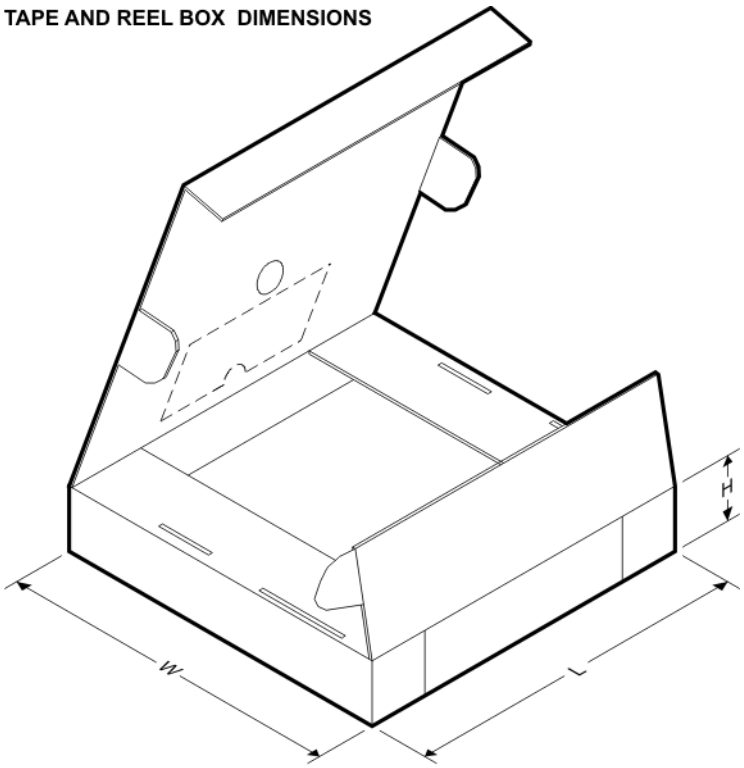
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8575CDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCF8575CDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575CDGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8575CDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCF8575CPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCF8575CRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

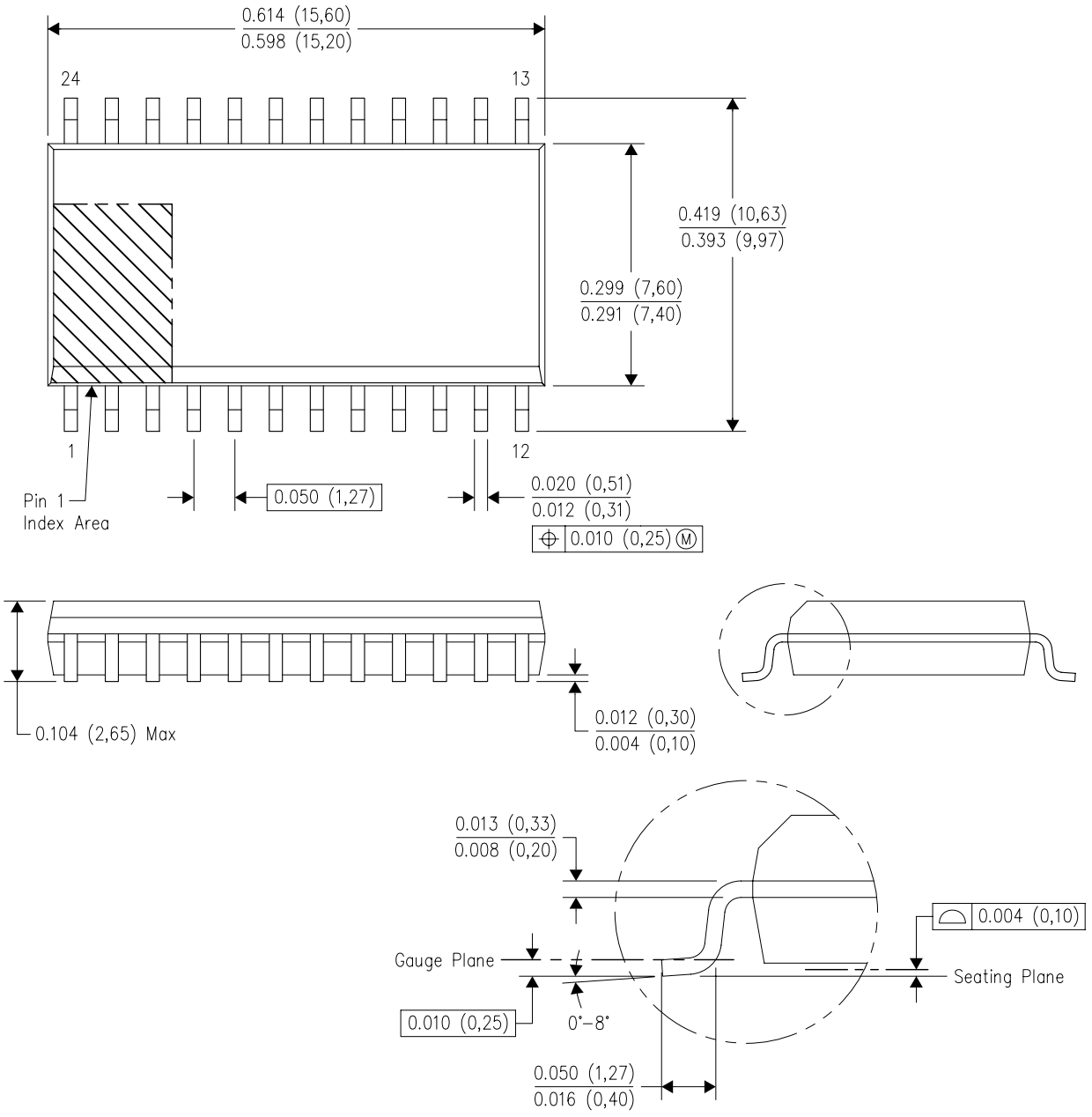
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

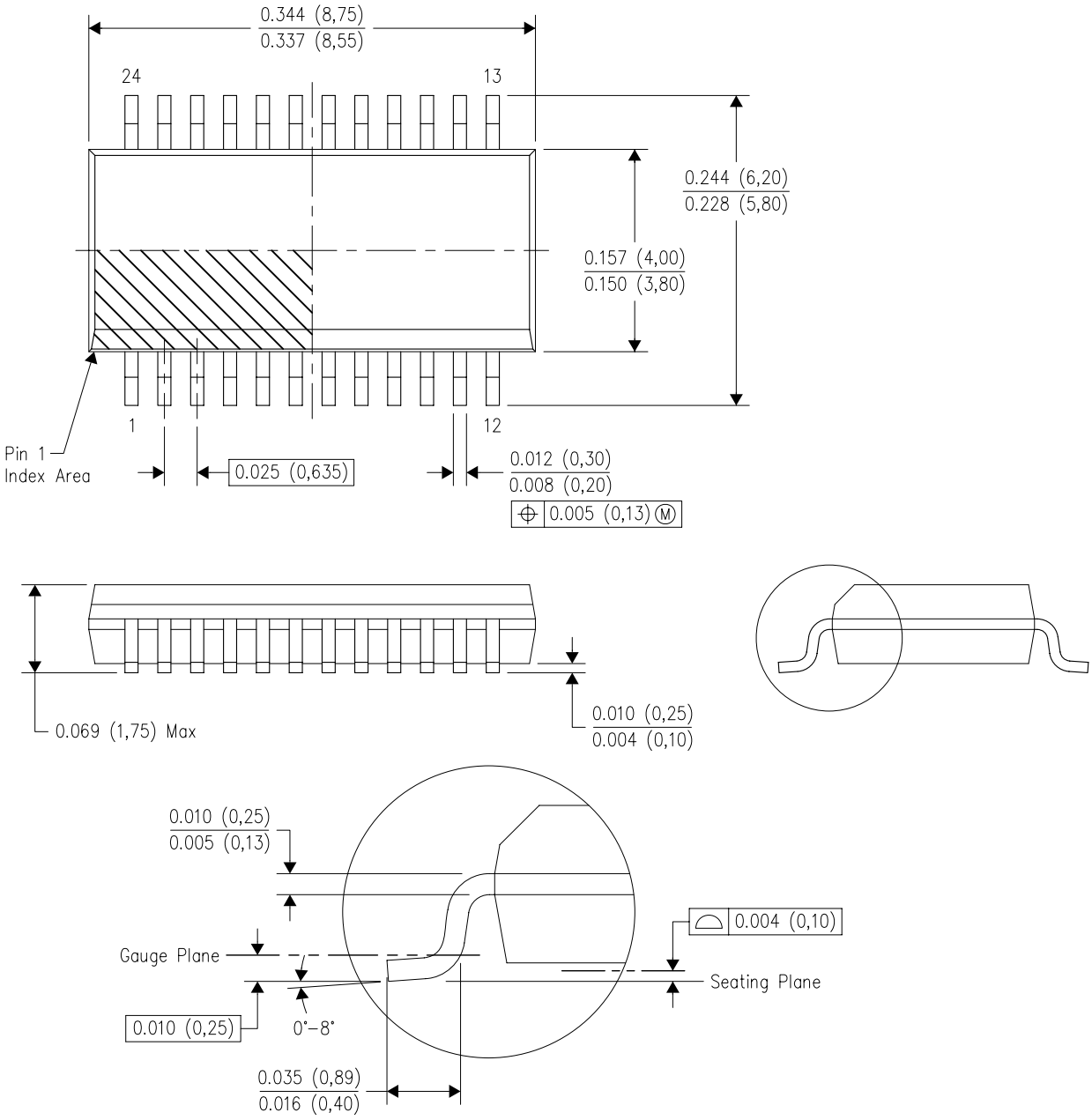
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8575CDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
PCF8575CDBR	SSOP	DB	24	2000	367.0	367.0	38.0
PCF8575CDGVR	TVSOP	DGV	24	2000	367.0	367.0	35.0
PCF8575CDWR	SOIC	DW	24	2000	367.0	367.0	45.0
PCF8575CPWR	TSSOP	PW	24	2000	367.0	367.0	38.0
PCF8575CRGER	VQFN	RGE	24	3000	367.0	367.0	35.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



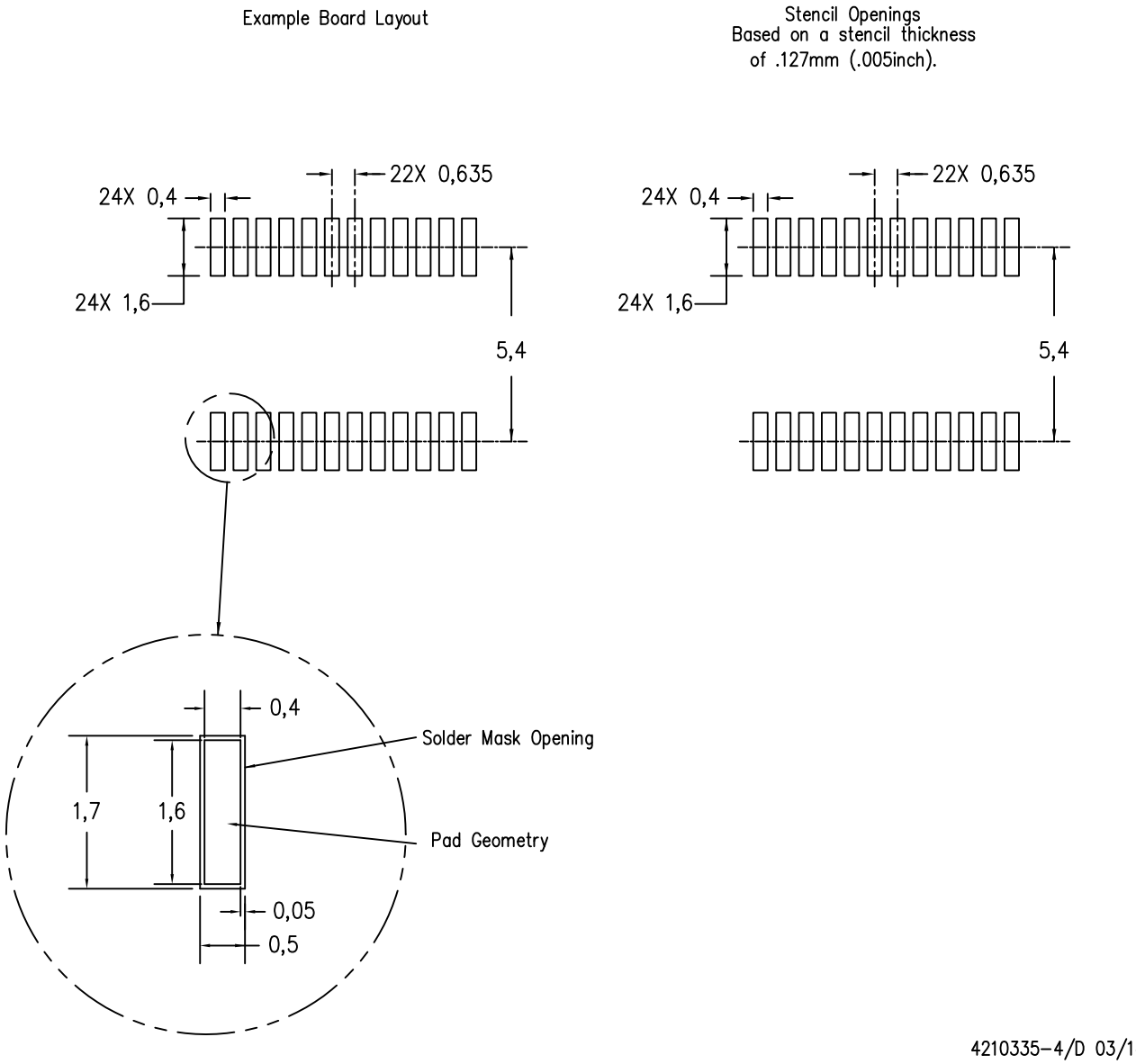
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



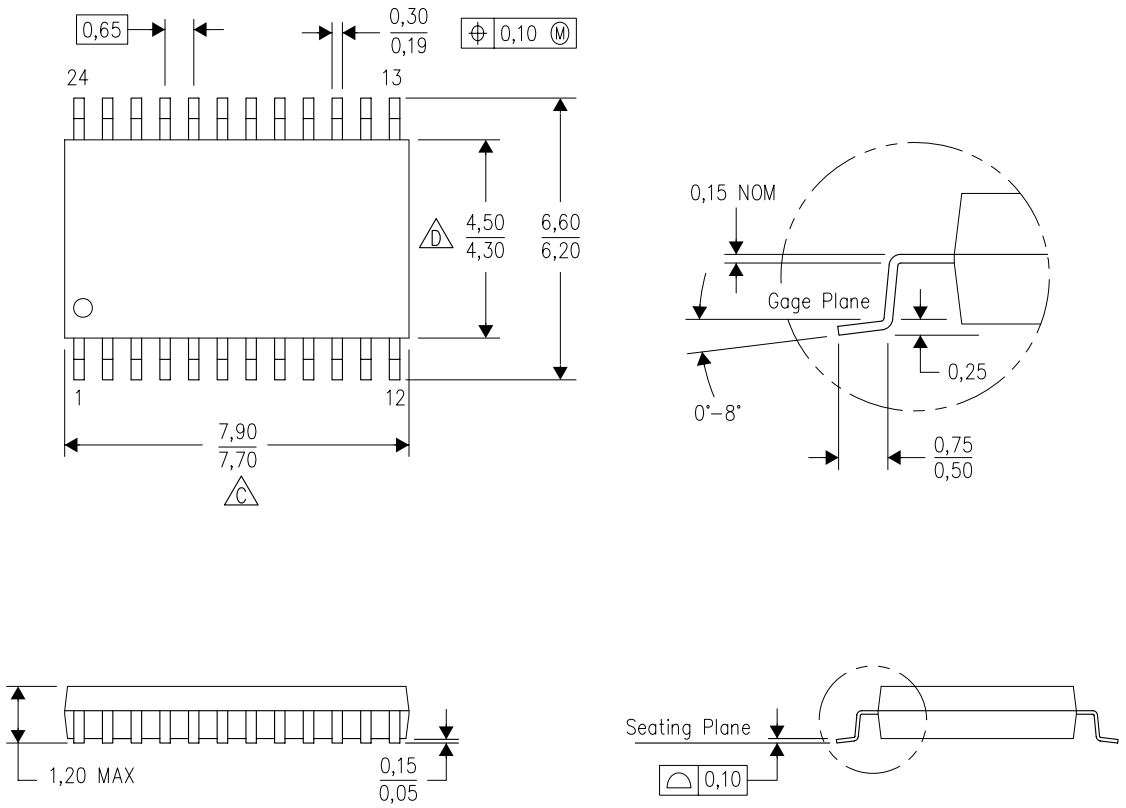
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

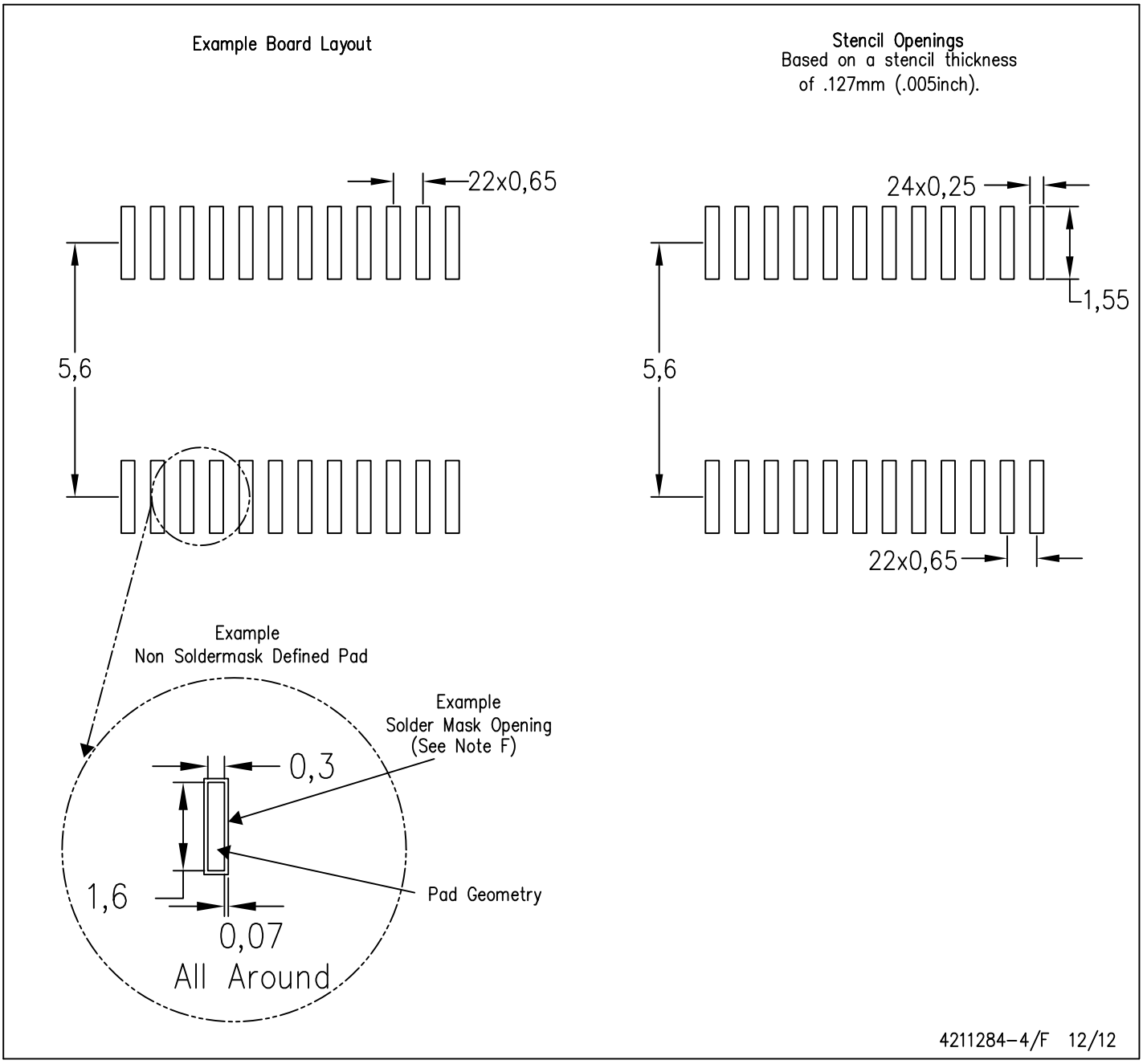
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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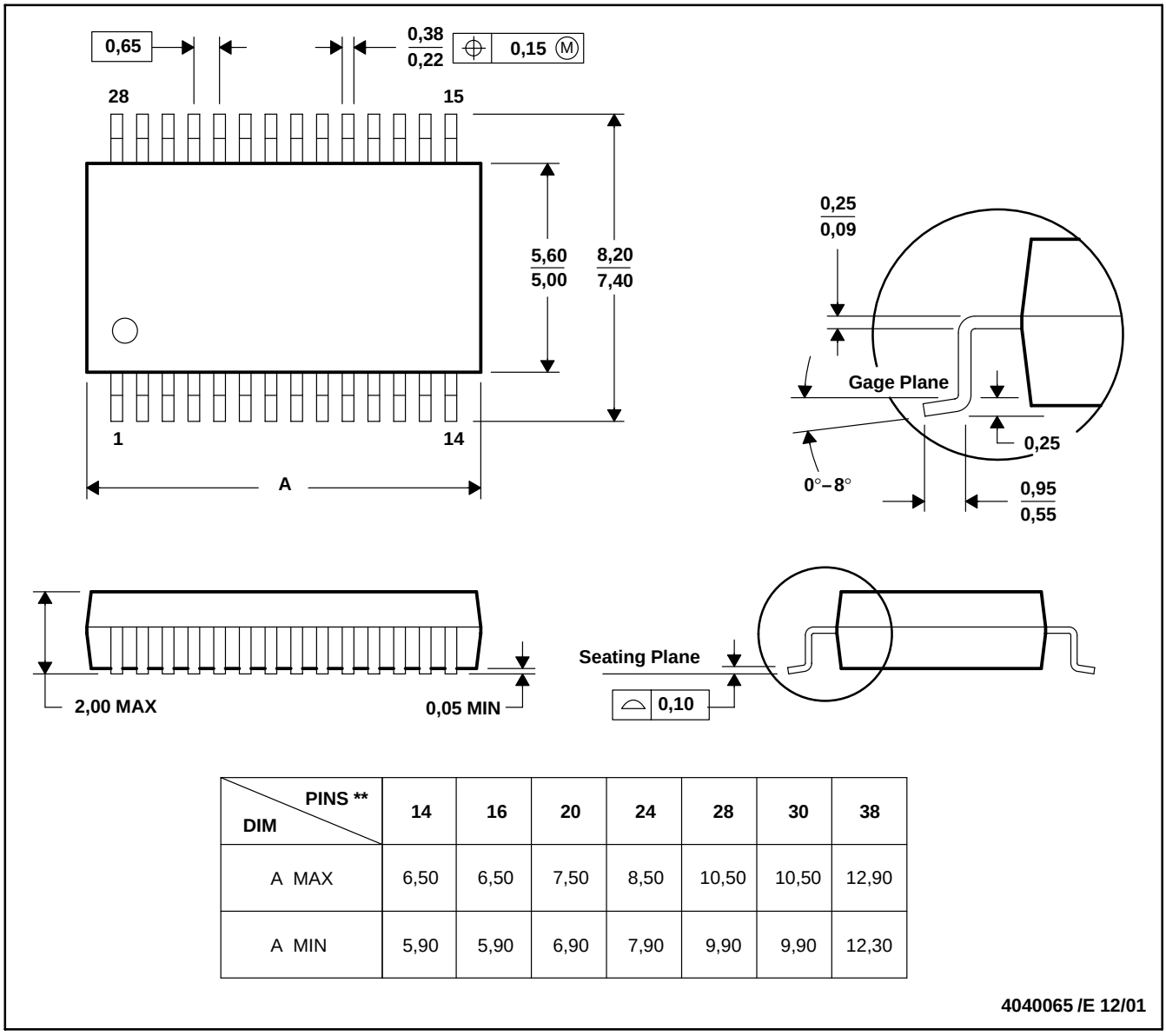
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

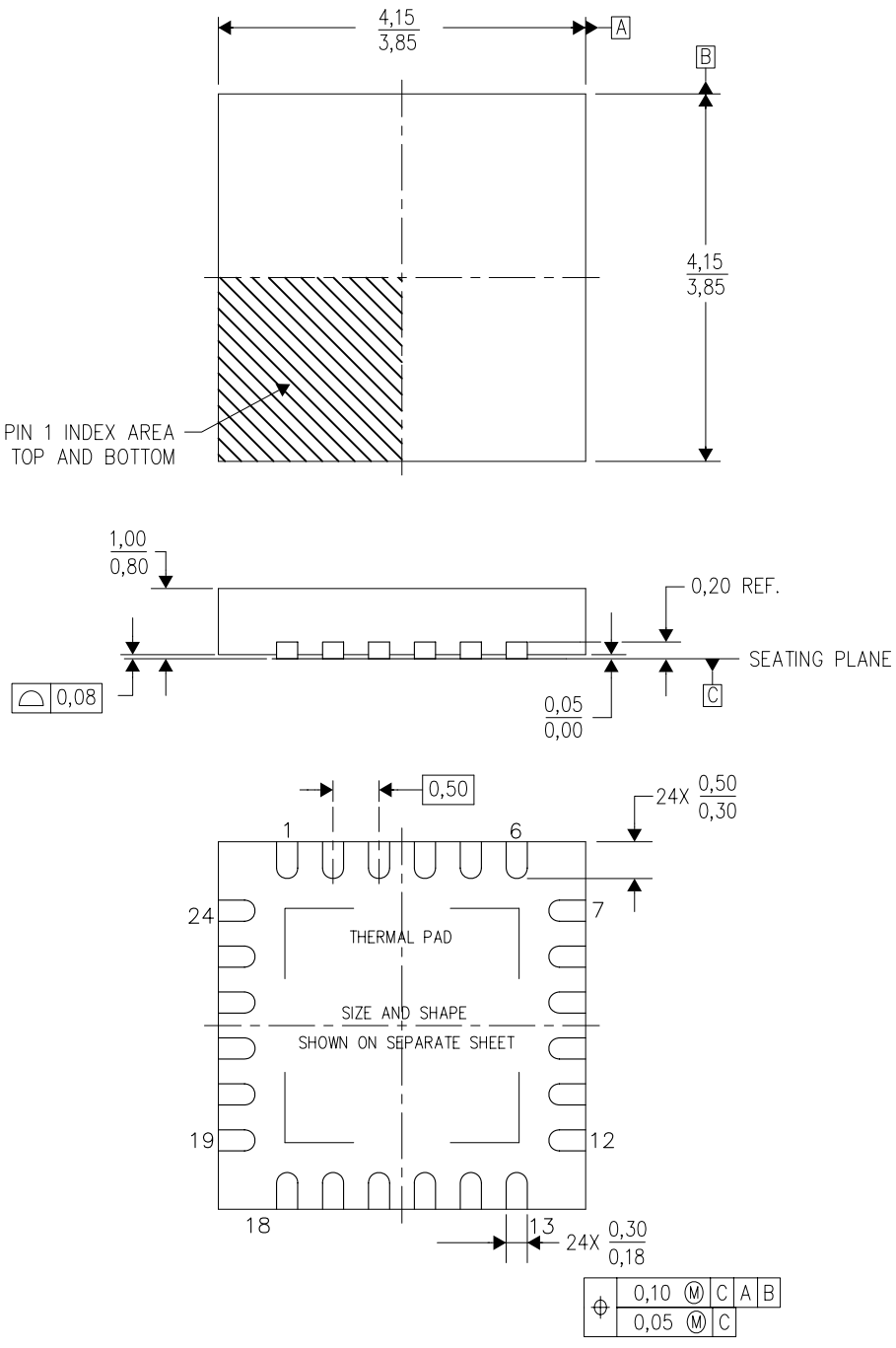


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

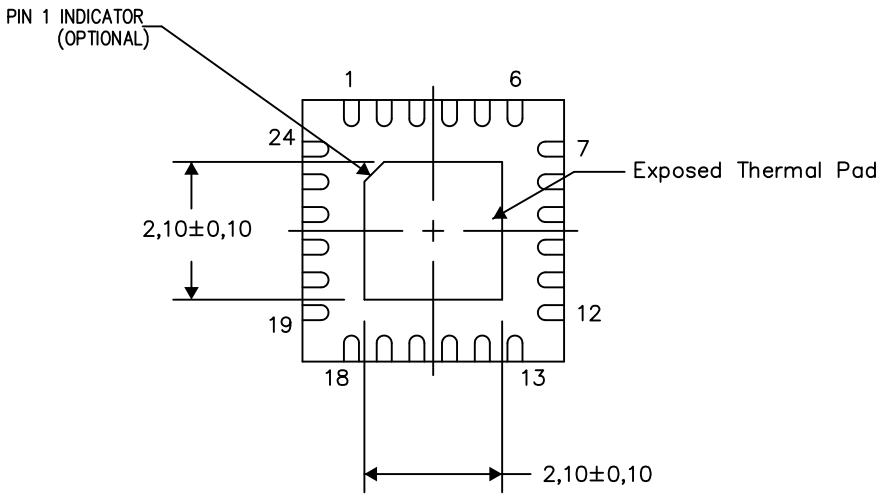
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



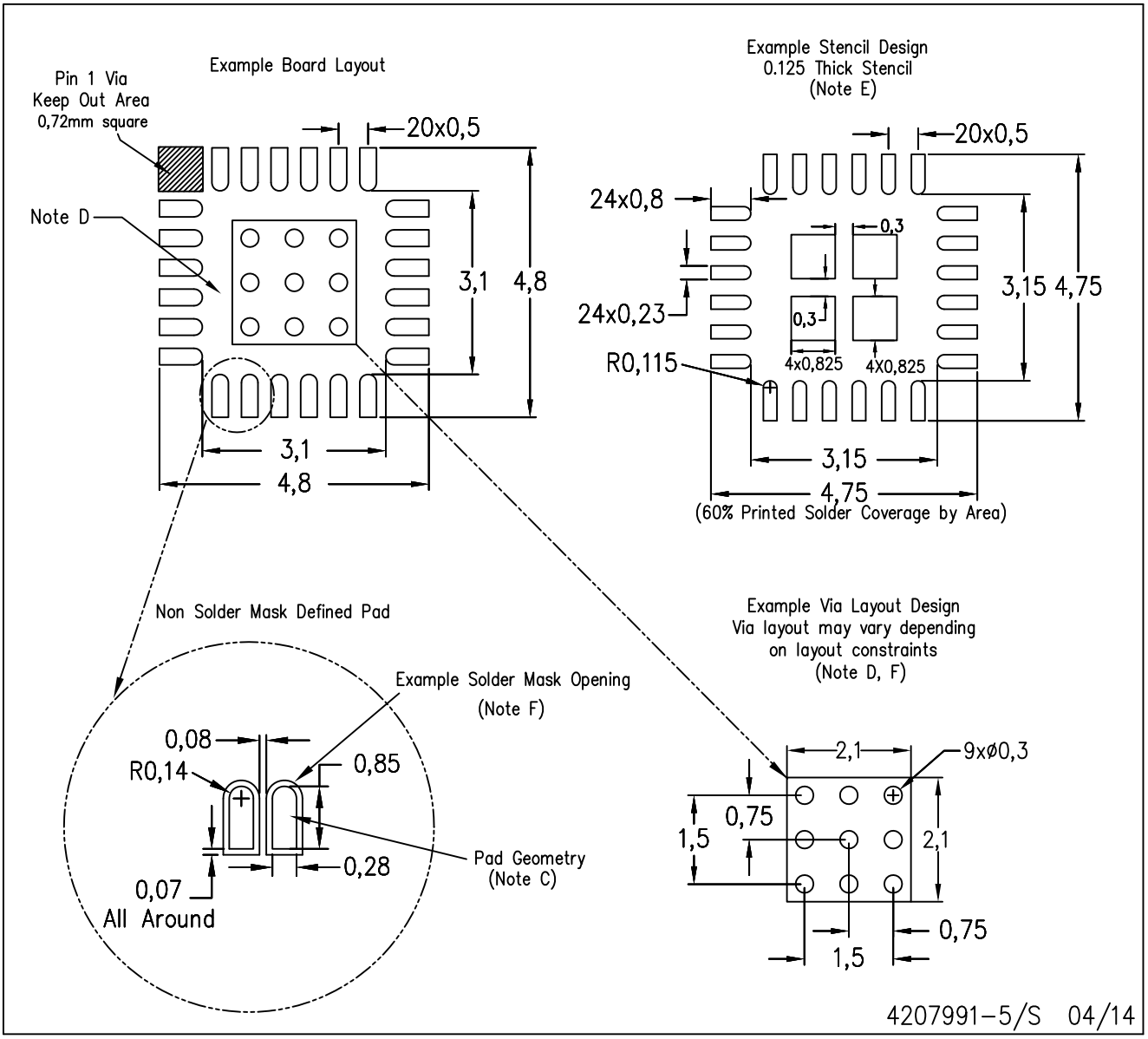
Bottom View

Exposed Thermal Pad Dimensions

4206344–6/AG 04/14

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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