

**Document Title****128K x8 bit Low Power and Low Voltage CMOS Static RAM****Revision History**

<b><u>Revision No.</u></b>	<b><u>History</u></b>	<b><u>Draft Data</u></b>	<b><u>Remark</u></b>
0.0	Initial draft	July 3, 1996	Preliminary
1.0	Finalize - Increased I <sub>SB</sub> , I <sub>DR</sub> Commercial part = 10 $\mu$ A Industrial part = 20 $\mu$ A	December 16, 1996	Final
2.0	Revise - Change speed bin KM68V1000C Family: 70/85ns $\rightarrow$ 70/100ns KM68U1000C Family: 70/100ns $\rightarrow$ 85/100ns - Improved operating current: 40mA $\rightarrow$ 35mA - Improved power dissipation PD: 0.7W $\rightarrow$ 1.0W - Improved standby current Extended/Industrial: 20 $\rightarrow$ 10 $\mu$ A - VIL: 0.4V $\rightarrow$ 0.6V	November 25, 1997	Final

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## 128K x8 bit Low Power and Low Voltage CMOS Static RAM

### FEATURES

- Process Technology: 0.4μm CMOS
- Organization: 128K x8
- Power Supply Voltage:
  - K6T1008V2C family: 3.0~3.6V
  - K6T1008U2C family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-SOP-525, 32-TSOP1-0820F/R, 32-TSOP1-0813.4F/R

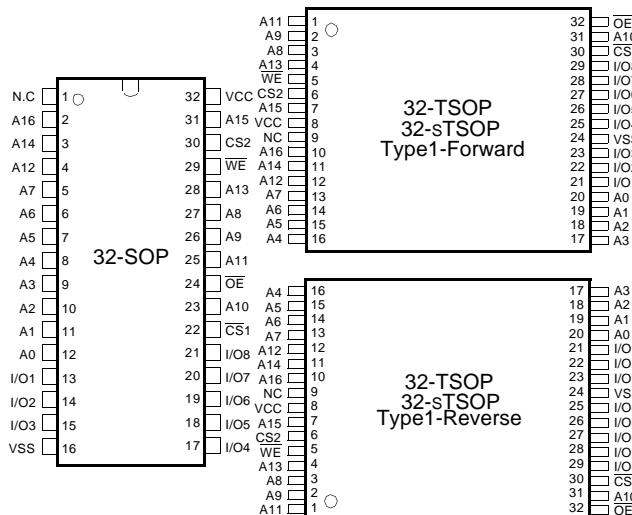
### GENERAL DESCRIPTION

The K6T1008V2C and K6T1008U2C families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

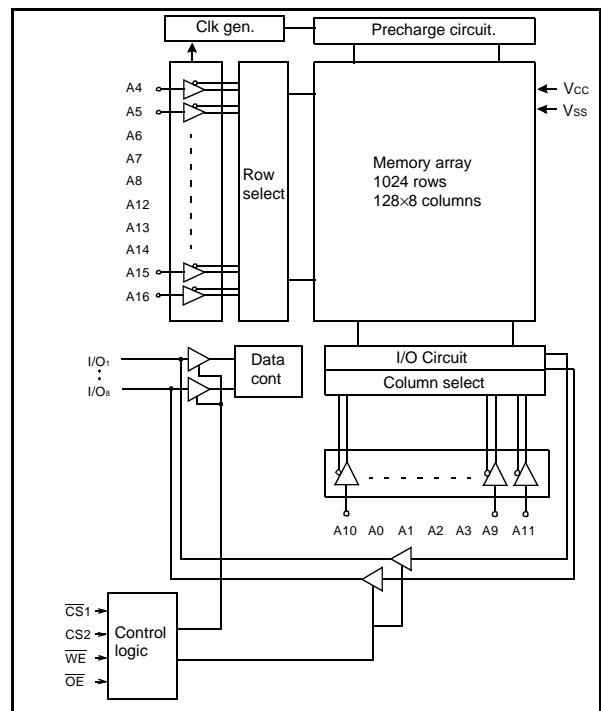
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I <sub>sb1</sub> , Max)	Operating (I <sub>cc2</sub> , Max)	
K6T1008V2C-B K6T1008U2C-B	Commercial(0~70°C)	3.0~3.6V 2.7~3.3V	70/100ns 85/100ns	10μA	35mA	32-SOP 32-TSOP1-F/R 32-sTSOP1-F/R
K6T1008V2C-D K6T1008U2C-D	Extended(-25~85°C)	3.0~3.6V 2.7~3.3V	70/100ns 85/100ns			
K6T1008V2C-F K6T1008U2C-F	Industrial(-40~85°C)	3.0~3.6V 2.7~3.3V	70/100ns 85/100ns			

### PIN DESCRIPTION



Name	Function
CS <sub>1</sub> , CS <sub>2</sub>	Chip Select Inputs
OE	Output Enable Input
WE	Write Enable Input
A <sub>0</sub> ~A <sub>16</sub>	Address Inputs
I/O <sub>1</sub> ~I/O <sub>8</sub>	Data Inputs/Outputs
Vcc	Power
Vss	Ground
N.C	No Connection

### FUNCTIONAL BLOCK DIAGRAM



SAMSUNG ELECTRONICS CO., LTD. reserves the right to change products and specifications without notice.

## PRODUCT LIST

Commercial Temperature Products (0~70°C)		Extended Temperature Products (-25~85°C)		Industrial Temperature Products (-40~85°C)	
Part Name	Function	Part Name	Function	Part Name	Function
K6T1008V2C-GB70	32-SOP, 70ns, 3.3V	K6T1008V2C-GD70	32-SOP, 70ns, 3.3V	K6T1008V2C-GF70	32-SOP, 70ns, 3.3V
K6T1008V2C-GB10	32-SOP, 100ns, 3.3V	K6T1008V2C-GD10	32-SOP, 100ns, 3.3V	K6T1008V2C-GF10	32-SOP, 100ns, 3.3V
K6T1008V2C-TB70	32-TSOP F, 70ns, 3.3V	K6T1008V2C-TD70	32-TSOP F, 70ns, 3.3V	K6T1008V2C-TF70	32-TSOP F, 70ns, 3.3V
K6T1008V2C-TB10	32-TSOP F, 100ns, 3.3V	K6T1008V2C-TD10	32-TSOP F, 100ns, 3.3V	K6T1008V2C-TF10	32-TSOP F, 100ns, 3.3V
K6T1008V2C-RB70	32-TSOP R, 70ns, 3.3V	K6T1008V2C-RD70	32-TSOP R, 70ns, 3.3V	K6T1008V2C-RF70	32-TSOP R, 70ns, 3.3V
K6T1008V2C-RB10	32-TSOP R, 100ns, 3.3V	K6T1008V2C-RD10	32-TSOP R, 100ns, 3.3V	K6T1008V2C-RF10	32-TSOP R, 100ns, 3.3V
K6T1008U2C-GB85	32-SOP, 85ns, 3.0V	K6T1008U2C-GD85	32-SOP, 85ns, 3.0V	K6T1008U2C-GF85	32-SOP, 85ns, 3.0V
K6T1008U2C-GB10	32-SOP, 100ns, 3.0V	K6T1008U2C-GD10	32-SOP, 100ns, 3.0V	K6T1008U2C-GF10	32-SOP, 100ns, 3.0V
K6T1008U2C-TB85	32-TSOP F, 85ns, 3.0V	K6T1008U2C-TD85	32-TSOP F, 85ns, 3.0V	K6T1008U2C-TF85	32-TSOP F, 85ns, 3.0V
K6T1008U2C-TB10	32-TSOP F, 100ns, 3.0V	K6T1008U2C-TD10	32-TSOP F, 100ns, 3.0V	K6T1008U2C-TF10	32-TSOP F, 100ns, 3.0V
K6T1008U2C-RB85	32-TSOP R, 85ns, 3.0V	K6T1008U2C-RD85	32-TSOP R, 85ns, 3.0V	K6T1008U2C-RF85	32-TSOP R, 85ns, 3.0V
K6T1008U2C-RB10	32-TSOP R, 100ns, 3.0V	K6T1008U2C-RD10	32-TSOP R, 100ns, 3.0V	K6T1008U2C-RF10	32-TSOP R, 100ns, 3.0V
K6T1008V2C-YB70	32-sTSOP F, 70ns, 3.3V	K6T1008V2C-YD70	32-sTSOP F, 70ns, 3.3V	K6T1008V2C-YF70	32-sTSOP F, 70ns, 3.3V
K6T1008V2C-YB10	32-sTSOP F, 100ns, 3.3V	K6T1008V2C-YD10	32-sTSOP F, 100ns, 3.3V	K6T1008V2C-YF10	32-sTSOP F, 100ns, 3.3V
K6T1008V2C-NB70	32-sTSOP R, 70ns, 3.3V	K6T1008V2C-ND70	32-sTSOP R, 70ns, 3.3V	K6T1008V2C-NF70	32-sTSOP R, 70ns, 3.3V
K6T1008V2C-NB10	32-sTSOP R, 100ns, 3.3V	K6T1008V2C-ND10	32-sTSOP R, 100ns, 3.3V	K6T1008V2C-NF10	32-sTSOP R, 100ns, 3.3V
K6T1008U2C-YB85	32-sTSOP F, 85ns, 3.0V	K6T1008U2C-YD85	32-sTSOP F, 85ns, 3.0V	K6T1008U2C-YF85	32-sTSOP F, 85ns, 3.0V
K6T1008U2C-YB10	32-sTSOP F, 100ns, 3.0V	K6T1008U2C-YD10	32-sTSOP F, 100ns, 3.0V	K6T1008U2C-YF10	32-sTSOP F, 100ns, 3.0V
K6T1008U2C-NB85	32-sTSOP R, 85ns, 3.0V	K6T1008U2C-ND85	32-sTSOP R, 85ns, 3.0V	K6T1008U2C-NF85	32-sTSOP R, 85ns, 3.0V
K6T1008U2C-NB10	32-sTSOP R, 100ns, 3.0V	K6T1008U2C-ND10	32-sTSOP R, 100ns, 3.0V	K6T1008U2C-NF10	32-sTSOP R, 100ns, 3.0V

## FUNCTIONAL DESCRIPTION

CS <sub>1</sub>	CS <sub>2</sub>	OE	WE	I/O Pin	Mode	Power
H	X <sup>1)</sup>	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
X <sup>1)</sup>	L	X <sup>1)</sup>	X <sup>1)</sup>	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X <sup>1)</sup>	L	Din	Write	Active

1. X means don't care(Must be in high or low status.)

## ABSOLUTE MAXIMUM RATINGS<sup>1)</sup>

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V	-
Voltage on Vcc supply relative to	V <sub>CC</sub>	-0.3 to 4.6	V	-
Power Dissipation	P <sub>D</sub>	1.0	W	-
Storage temperature	T <sub>STG</sub>	-65 to 150	°C	-
Operating Temperature	T <sub>A</sub>	0 to 70	°C	K6T1008V2C-B/K6T1008U2C-B
		-25 to 85	°C	K6T1008V2C-D/K6T1008U2C-D
		-40 to 85	°C	K6T1008V2C-F/K6T1008U2C-F
Soldering temperature and time	T <sub>SOLDER</sub>	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS<sup>1)</sup>

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	K6T1008V2C Family	3.0	3.3	3.6	V
		K6T1008U2C Family	2.7	3.0	3.3	
Ground	V <sub>SS</sub>	All Family	0	0	0	V
Input high voltage	V <sub>IH</sub>	K6T1008V2C, K6T1008U2C Family	2.2	-	V <sub>CC</sub> +0.3 <sup>2)</sup>	V
Input low voltage	V <sub>IL</sub>	K6T1008V2C, K6T1008U2C Family	-0.3 <sup>3)</sup>	-	0.6	V

1. Commercial Product: T<sub>A</sub>=0 to 70°C, unless otherwise specified  
 Extended Product: T<sub>A</sub>=-25 to 85°C, unless otherwise specified  
 Industrial Product: T<sub>A</sub>=-40 to 85°C, unless otherwise specified
2. Overshoot: V<sub>CC</sub>+3.0V in case of pulse width ≤30ns
3. Undershoot: -3.0V in case of pulse width ≤30ns
4. Overshoot and undershoot is sampled, not 100% tested.

## CAPACITANCE<sup>1)</sup> (f=1MHz, T<sub>A</sub>=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output capacitance	C <sub>IO</sub>	V <sub>IO</sub> =0V	-	8	pF

1. Capacitance is sampled, not 100% tested

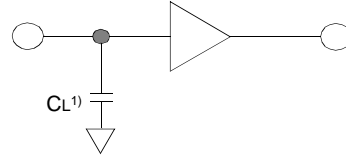
## DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output leakage current	I <sub>LO</sub>	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating power supply	I <sub>CC</sub>	I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , Read	-	2	5	mA	
Average operating current	I <sub>CC1</sub>	Cycle time=1μs, 100% duty, I <sub>IO</sub> =0mA, CS <sub>1</sub> ≤0.2V, CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤0.2V or V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V	Read	-	1.5	5	mA
			Write	-	10	15	
	I <sub>CC2</sub>	Cycle time=Min, 100% duty, I <sub>IO</sub> =0mA, $\overline{CS}_1=V_{IL}$ , CS <sub>2</sub> =V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>	-	25	35	mA	
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1mA	-	-	0.4	V	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0mA	2.2	-	-	V	
Standby Current(TTL)	I <sub>SB</sub>	$\overline{CS}_1=V_{IH}$ , CS <sub>2</sub> =V <sub>IL</sub> , Other inputs=V <sub>IL</sub> or V <sub>IH</sub>	-	-	0.3	mA	
Standby Current(CMOS)	I <sub>SB1</sub>	$\overline{CS}_1≥V_{CC}-0.2V$ , CS <sub>2</sub> ≥V <sub>CC</sub> -0.2V or CS <sub>2</sub> ≤0.2V, Other inputs=0~V <sub>CC</sub>	-	0.3	10	μA	

## AC OPERATING CONDITIONS

### TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V  
 Input rising and falling time: 5ns  
 Input and output reference voltage: 1.5V  
 Output load (see right):  $C_L = 100\text{pF} + 1\text{TTL}$



1. Including scope and jig capacitance

## AC CHARACTERISTICS (Commercial product: $T_A = 0$ to $70^\circ\text{C}$ , Extended product: $T_A = -25$ to $85^\circ\text{C}$ , Industrial product: $T_A = -40$ to $85^\circ\text{C}$ )

K6T1008V2C Family:  $V_{CC} = 3.0 \sim 3.6\text{V}$ , K6T1008U2C Family:  $V_{CC} = 2.7 \sim 3.3\text{V}$ )

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	t <sub>RC</sub>	70	-	85	-	100	-	ns
	Address access time	t <sub>AA</sub>	-	70	-	85	-	100	ns
	Chip select to output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	70	-	85	-	100	ns
	Output enable to valid output	t <sub>OE</sub>	-	35	-	40	-	50	ns
	Chip select to low-Z output	t <sub>LZ</sub>	10	-	10	-	10	-	ns
	Output enable to low-Z output	t <sub>OLZ</sub>	5	-	5	-	5	-	ns
	Chip disable to high-Z output	t <sub>HZ</sub>	0	25	0	25	0	30	ns
	Output disable to high-Z output	t <sub>OHZ</sub>	0	25	0	25	0	30	ns
	Output hold from address change	t <sub>OH</sub>	10	-	15	-	15	-	ns
Write	Write cycle time	t <sub>WC</sub>	70	-	85	-	100	-	ns
	Chip select to end of write	t <sub>CW</sub>	60	-	70	-	80	-	ns
	Address set-up time	t <sub>AS</sub>	0	-	0	-	0	-	ns
	Address valid to end of write	t <sub>AW</sub>	60	-	70	-	80	-	ns
	Write pulse width	t <sub>WP</sub>	55	-	60	-	70	-	ns
	Write recovery time	t <sub>WR</sub>	0	-	0	-	0	-	ns
	Write to output high-Z	t <sub>WHZ</sub>	0	25	0	30	0	30	ns
	Data to write time overlap	t <sub>DW</sub>	30	-	35	-	40	-	ns
	Data hold from write time	t <sub>DH</sub>	0	-	0	-	0	-	ns
	End write to output low-Z	t <sub>OW</sub>	5	-	5	-	5	-	ns

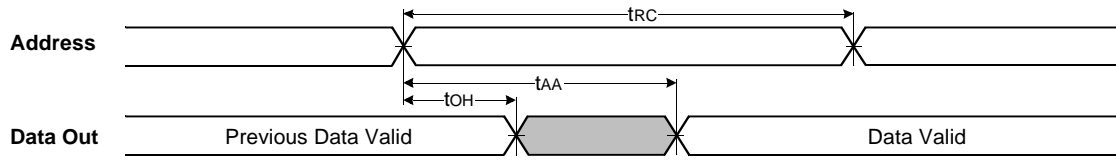
## DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition <sup>1)</sup>	Min	Typ	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	$\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$	2.0	-	3.6	V
Data retention current	I <sub>DR</sub>	$V_{CC} = 3.0\text{V}$ , $\overline{CS}_1 \geq V_{CC} - 0.2\text{V}$ , $CS_2 \geq V_{CC} - 0.2\text{V}$ , or $CS_2 \leq 0.2\text{V}$	-	0.3	5	$\mu\text{A}$
Data retention set-up time	t <sub>SDR</sub>	See data retention waveform	0	-	-	ms
Recovery time	t <sub>RDR</sub>		5	-	-	

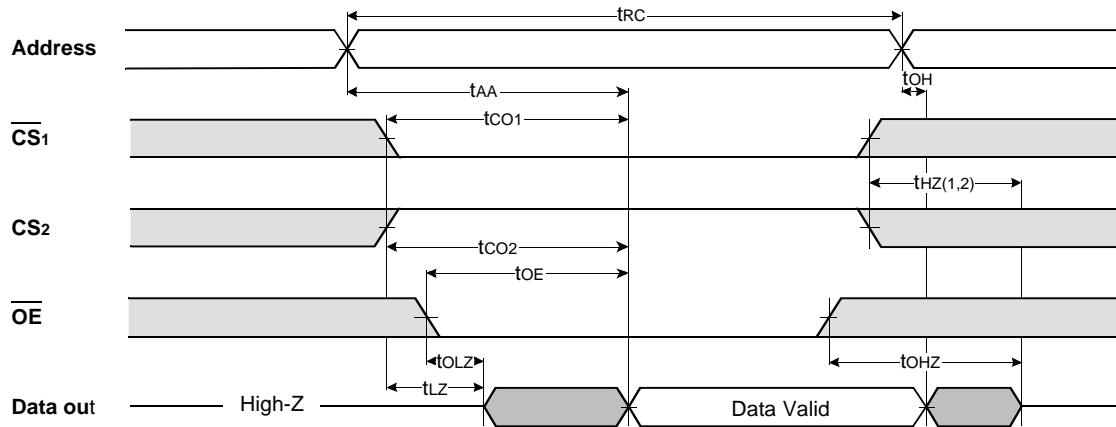
1.  $CS_1 \geq V_{CC} - 0.2\text{V}$ ,  $CS_2 \geq V_{CC} - 0.2\text{V}$ , or  $CS_2 \leq 0.2\text{V}$

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ )



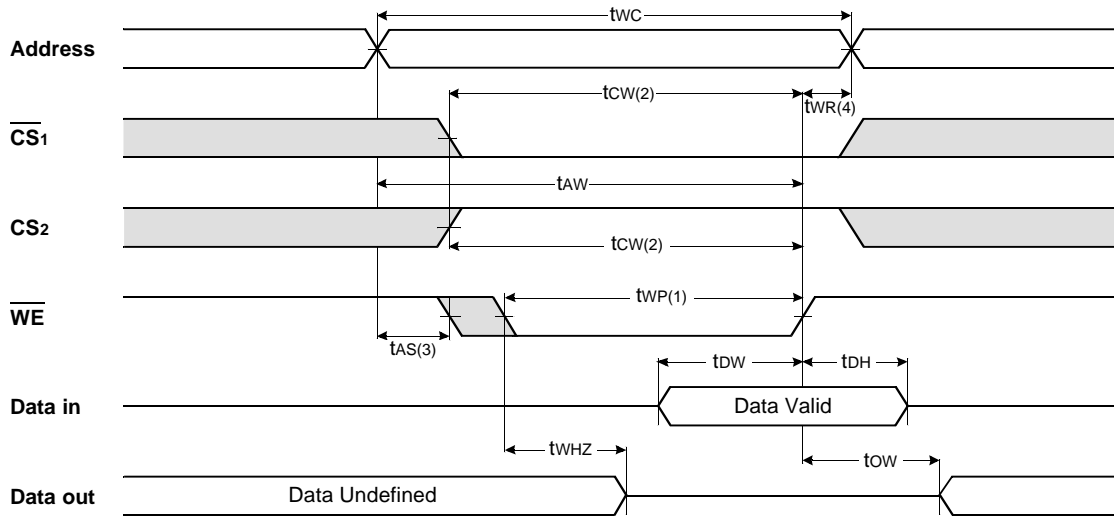
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



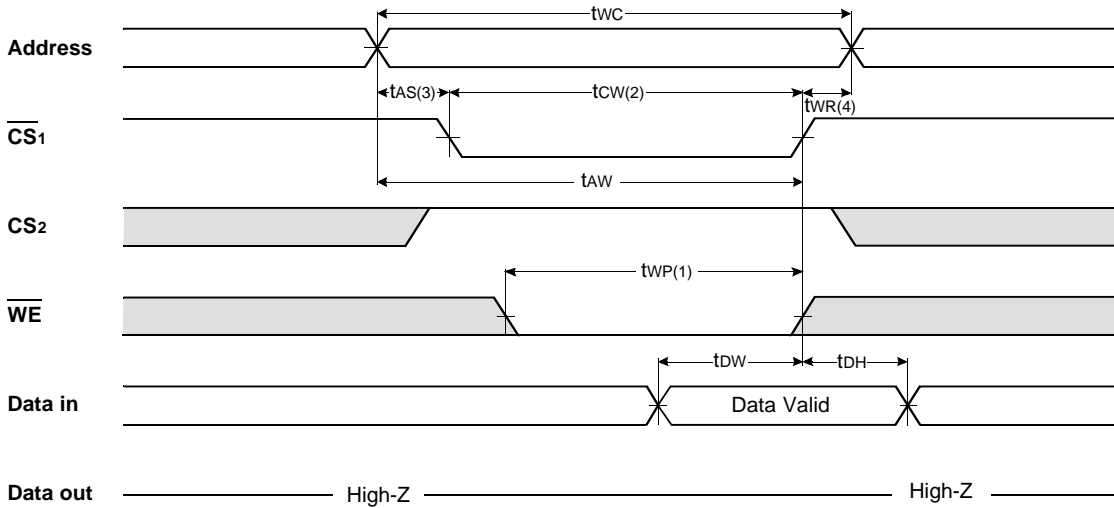
NOTES (READ CYCLE)

1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, tHZ(Max.) is less than tLZ(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{WE}$  Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{CS1}$  Controlled)



## TIMING WAVEFORM OF WRITE CYCLE(3) (CS<sub>2</sub> Controlled)

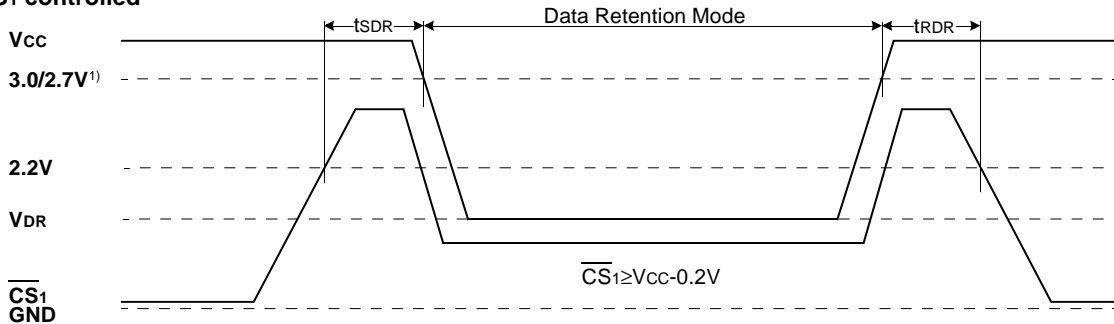


### NOTES (WRITE CYCLE)

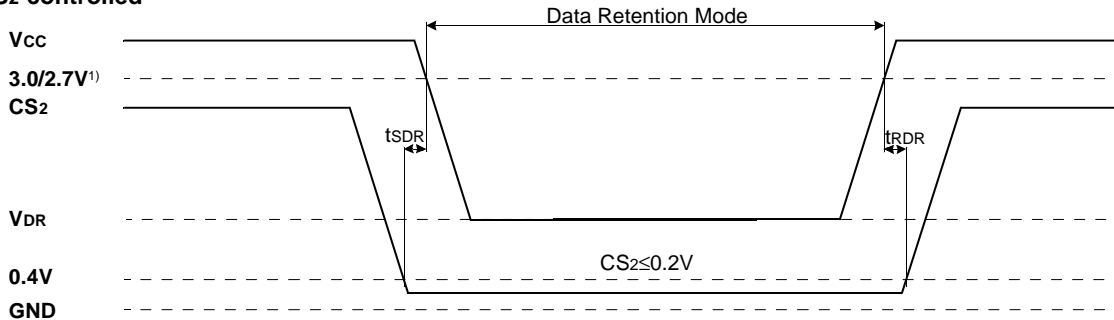
1. A write occurs during the overlap of a low  $\overline{CS}_1$ , a high  $CS_2$  and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS}_1$  goes low,  $CS_2$  going high and  $\overline{WE}$  going low: A write ends at the earliest transition among  $CS_1$  going high,  $CS_2$  going low and  $\overline{WE}$  going high:  $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the  $\overline{CS}_1$  going low or  $CS_2$  going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR(1)}$  applied in case a write ends as  $\overline{CS}_1$  or  $\overline{WE}$  going high  $t_{WR(2)}$  applied in case a write ends as  $CS_2$  going to low.

## DATA RETENTION WAVE FORM

### $\overline{CS}_1$ controlled



### $CS_2$ controlled



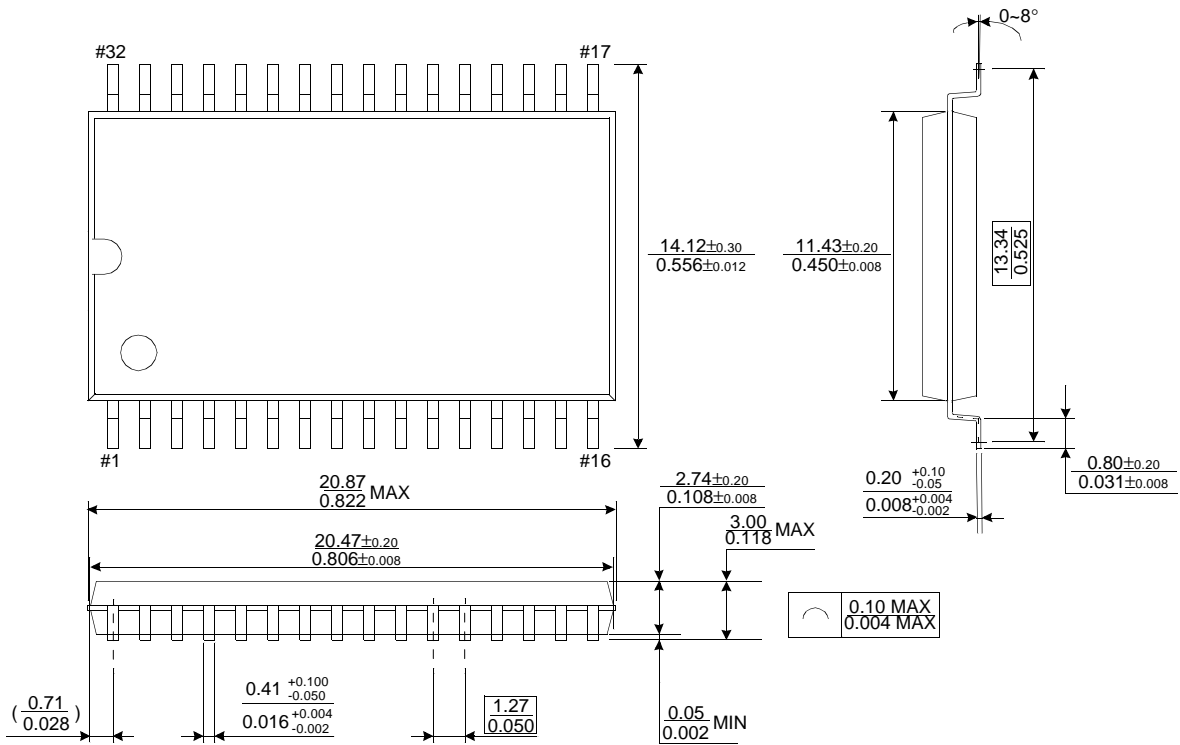
1. 3.0V for K6T1008V2C Family, 2.7V for K6T1008U2C Family



PACKAGE DIMENSIONS

Units: millimeter(inch)

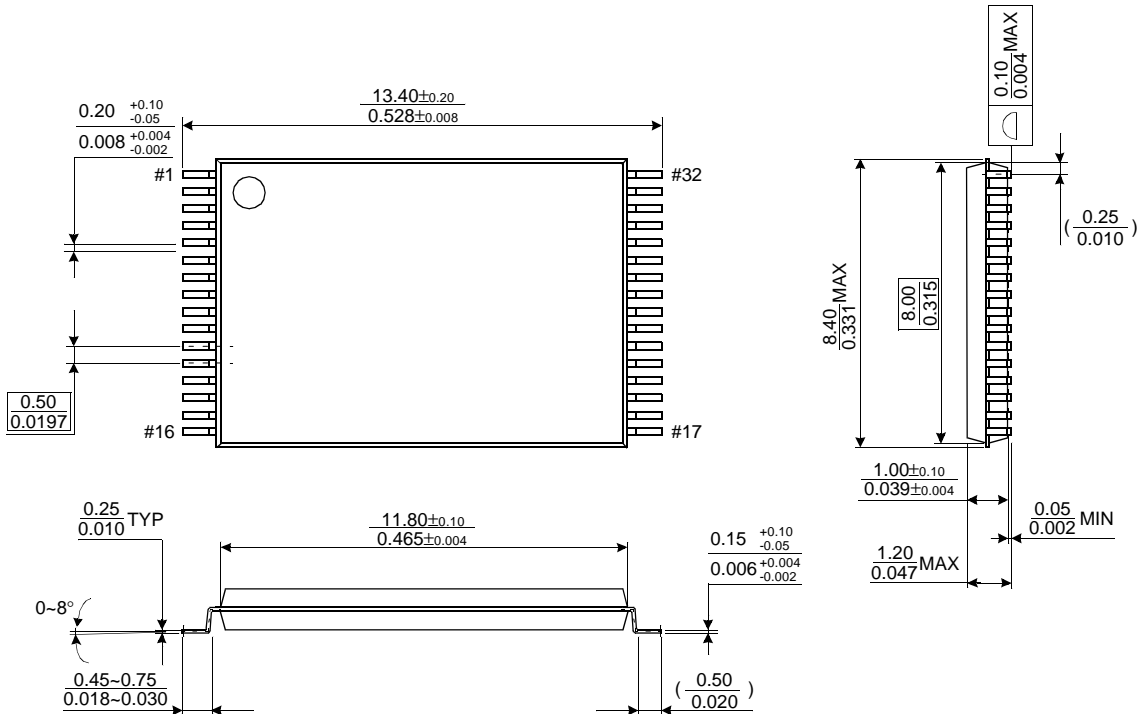
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



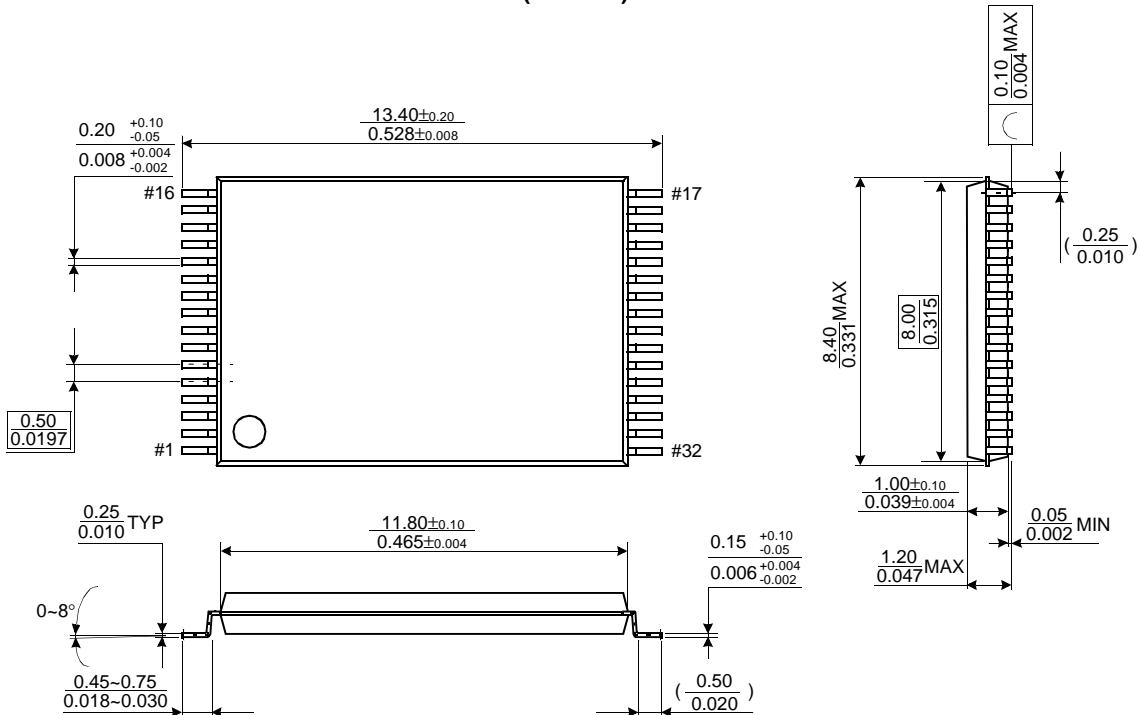
## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)



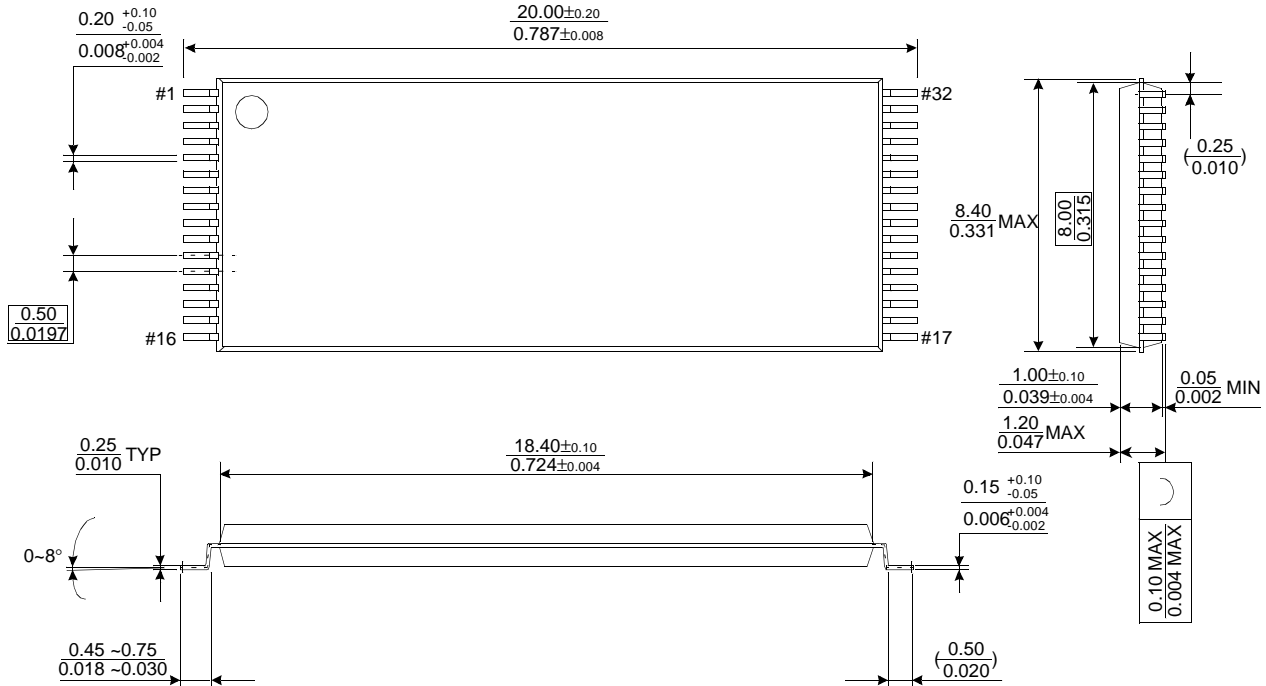
### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4R)



## PACKAGE DIMENSIONS

Units: millimeter(inch)

### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



### 32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820R)

