HS-7541

12-Bit Monolithic CMOS MDAC

Features

- 12-Bit Endpoint Linearity (±1/2 LSB)
- Full 4 Quadrant Multiplication
- Pretrimmed Gain
- Low Feedthrough Error
- Superior Power Supply Rejection
- Low Gain Tempco
- TTL/CMOS Compatible
- Low Power Consumption
- Latch-Up Resistant
- Direct Replacement For AD7521 and AD7541

Applications

- Programmable Amplifiers
- Function Generators
- Digitally Controlled Attenuators
- Digitally Controlled Power Supplies
- Digital Filters
- Digital/Synchro Conversion
- Ratiometric A/D Conversion
- CRT Graphics Generator

Description

The HS-7541 is a 12 bit, 4-quadrant multiplying digital-to-analog converter contained in a single high density monolithic CMOS chip. It is manufactured using an advanced oxide isolated, silicon-gate, monolithic CMOS technology.

The HS-7541 consists of a highly stable thin-film R-2R ladder network and twelve NMOS current switches on a monolithic chip. The thin-film resistors are laser trimmed to provide true 12 bit linearity and excellent absolute accuracy. The NMOS switches are temperature-compensating and their "ON" resistances are binarily scaled, so that the voltage drop across each switch is identical. This is essential in maintaining the accuracy of the binarily weighted current division performed by the ladder network. The internal feedback resistor used in the output's current-to-voltage conversion operation is matched to the R-2R ladder.

The HS-7541 is a pin-compatible replacement for Analog Device's AD7521 and AD7541 with equal or better performance. The part is available in both plastic and hermetic packages as well as screened to the commercial, industrial and military temperature ranges. Mil-Std-883 Revision C versions are also available (consult factory for applicable data sheet)

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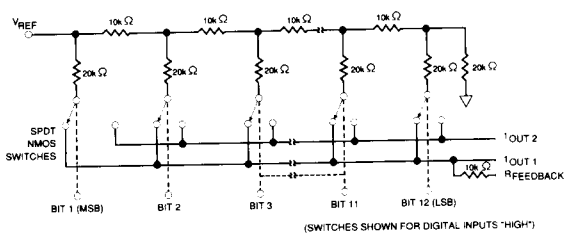
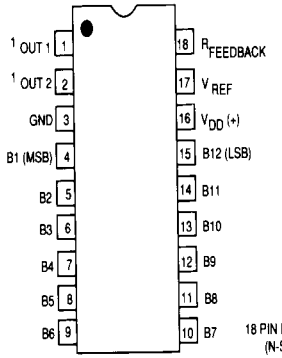
Functional Diagram



Pin Connections



18 PIN Epoxy Dip
(N-Suffix)

18 PIN Hermetic Dip
(Q-Suffix)

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Absolute Maximum Ratings

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND)	+17V
V_{REF}(to GND)	±25V
V_{RFB}(to GND)	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	-0.3V, to V_{DD}
Power Dissipation (Package)	450mW
Derate Above +75°C	6mW/°C

Operating Temperature Range (T_A = Full)

HS 7541 JN/KN	0° C to 70°C
HS 7541 AQ/BQ	-25°C to +85°C
HS 7541 SQ/TQ	-55°C to +125°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to 150°C
Lead Temperature (Soldering, 60sec)	300°C

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
Use proper ESD handling procedures.
Stresses above those listed under absolute maximum ratings may cause permanent damage to the device.

Electrical Characteristics

V_{DD} = +15V, V_{REF} =+10V, Out $_1$=Out $_2$=0V, T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Static Accuracy						
Resolution	N		12			Bits
Nonlinearity	INL	HS - 7541 KN/BQ/TQ (monotonic to 12-bits) HS - 7541 JN/AQ/SQ (monotonic to 11-bits)			±1/2 ±1	LSB LSB
Gain Error	G_{FSE}	Using Internal Feedback Resistor T_A = 25°C T_A = Full			±12.5 ±16.7	LSB LSB
Power Supply Rejection $\Delta Gain/\Delta V_{DD}$	PSRR	T_A = 25°C;ΔVD = ±0.5V T_A = Full; ΔVD = ±0.5V			±.0.01 ±0.02	%/% %/%
Output Leakage Current	I_{LKG}	I_{OUT1}; Digital Inputs = V_{IL} T_A = 25°C T_A = Full I_{OUT2}; Digital Inputs = V_{IH} T_A = 25°C T_A = Full			 ±50 ±200 ±50 ±200	 nA nA nA nA
Reference Input						
Input Resistance	R_{REF}		5		20	KΩ
Input Resistance Tempco (ΔR/ΔT)	TC_{R-REF}			300		PPM/°C
Dynamic Performance						
Output Current Settling Tlime	t_S	To ±1/2 LSB of FSR			1.0	µS
Feedthrough Error	FT	V_{REF} = 20V_{P-P} @ f = 10kHz All digital inputs low			1.0	mV_{P-P}

Electrical Characteristics

V_{DD} = +15V, V_{REF} =+10V, Out $_1$=Out $_2$=0V, T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Digital Inputs						
Digital Input High	V_{IH}		2.4			V
Digital Inputs Low	V_{INL}				0.8	V
Input Leakage Current	I_{IL}	V_{IN} = 0 to 15V			±1	µA
Input Capacitance	C_{IN}				10	pF
Analog Outputs						
Output Capacitance	C_{OUT1}	Digital Inputs = V_{IH}		189	220	pF
		Digital Inputs = V_{IL}		95	120	pF
	C_{OUT2}	Digital Inputs = V_{IH}		36	60	pF
		Digital Inputs = V_{IL}		134	165	pF
Power Suppy						
Supply Current	I_{DD}	Digital Inputs = V_{IL} or V_{IH}			2	ma

Circuit Description

General

The HS-7541 is a 12-bit multiplying D/A converter consisting of a highly stable, silicon-chrome thin film R-2R ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier. A simplified circuit of the HS-7541 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ BUS lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The design includes a matching switch in series with the feedback (R_{FB}) and terminating resistors. These switches (Figure 1) provide improved gain and linearity performance over the operating temperature range. The twelve output current-steering switches are in series with the R-2R resistor ladder, and therfore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each remains constant. If for example switch 1 (Figure 1) was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc.m a constant 5mV drop will then be maintained across each switch.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are LOW and $I_{OUT\,1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore modulated between the low and high values.

Output Impedance

The output resistance, as in the case of the ouput capacitance, is also modulated by the digital input code. The resistance looking back into the $I_{OUT\,1}$ terminal, may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). The static accuracy and dynamic performance will be affected by this modification.

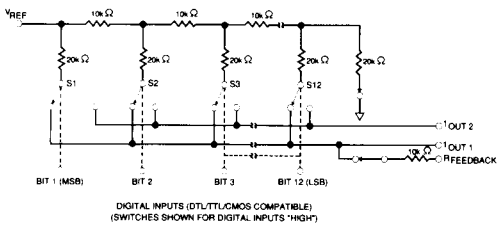

FIGURE 1: Simplified DAC Circuit

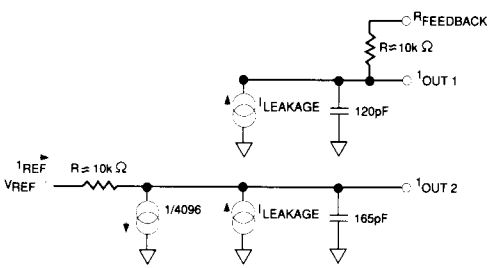

FIGURE 2: HS-7541 Equivalent Circuit (All Inputs Low)

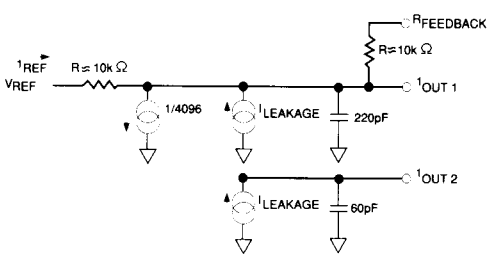

FIGURE 3: HS-7541 Equivalent Circuit (All Inputs High)

Application Information

Unipolar Operation

The connections required for digital unipolar operation are shown in Figure 4. The reference voltage V_{REF} may be either positive or negative. The 2kΩ potentiometer in the V_{REF} line and the 1kΩ resistor in the feedback loop are optional and are only needed when the gain error must be trimmed to less than 0.3% F.S.R. They should track each other to better than 0.1%, but don't have to track 7541's internal network resistors.

As shown in Figure 4 the DAC current output is typically connected to an external OP-AMP with it's non-inverting input tied to ground. The amplifier selected should have a low input bias current and low drift over temperature. To maintain specified HS-7541 linearity, the amplifiers input offset voltage should be nulled to less than ±200μV (o.1LSB). Table 1 shows the code table for unipolar operation.

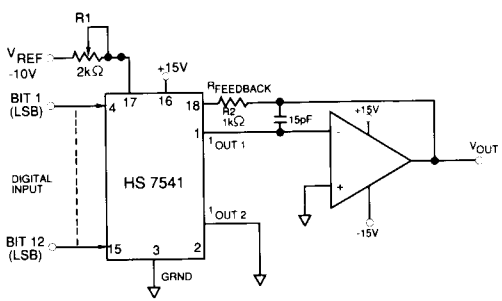

FIGURE 4: Unipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99975 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.50000V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	-0.49975 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	0

TABLE 1: Unipolar Operation Code Table

Bipolar Operation

The connections required for bipolar operation are shown in Figure 5. The digital input is offset binary coded and produces an output according to the code table shown in Table 2.

As in the case of unipolar operation the gain trim resistors can be omitted in applications that do not require minimum gain error. Amplifier considerations of low input bias current, low drift and offset nulling are also applicable for bipolar operation.

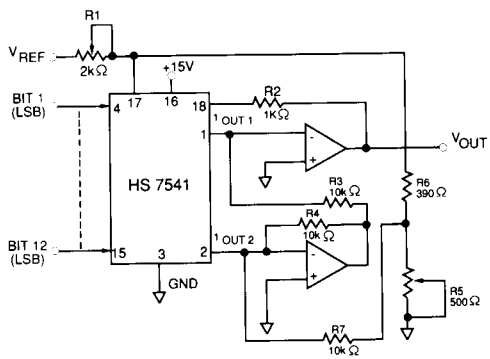

FIGURE 5: Bipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99951 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.00049V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	+0.50000 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	+1.00000 V_{REF}

TABLE 2: Bipolar Operation Code Table

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Ordering Information

PART #	PACKAGE	T_A-TEMP RANGE (°C)	RELATIVE ACCURACY (LSB's)	GAIN ERROR (LSB's)
HS 7541 JN	20-Pin Epoxy Dip	0 to 70	± 1	± 16.7
HS 7541 KN	20-Pin Epoxy Dip	0 to 70	± 1/2	± 16.7
HS 7541 AQ	20-Pin Hermetic Cerdip	-25 to 85	± 1	± 16.7
HS 7541 BQ	20-Pin Hermetic Cerdip	-25 to 85	± 1/2	± 16.7
HS 7541 SQ	20-Pin Hermetic Cerdip	-55 to 125	± 1	± 16.7
HS 7541 TQ	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 16.7
HS 7541 SQ/883	20-Pin Hermetic Cerdip	-55 to125	+1	± 16.7
HS 7541 TQ/883	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 16.7

NOTES: 1) Consult Factory For 883 Data Sheet
2) Package Designations: Suffix N-Plastic Dip, Suffix Q-Hermetic Dip.
For package mechanical dimensions, call DataLinear at (408) 945-9080.

CROSS REFERENCE INFORMATION

ADI Part No.	DataLinear Part No.
AD 7541 JN	HS 7541 JN
AD 7541 KN	HS 7541 KN
AD 7541 AD	HS 7541 AQ
AD 7541 BD	HS 7541 BQ
AD 7541 SD	HS 7541 SQ
AD 7541 TD	HS 7541 TQ
AD 7541 SD/883	HS 7541 SQ/883
AD 7528 TD/883	HS 7541 TQ/883