



8K x 8 HIGH-SPEED CMOS STATIC RAM

FEATURES

- High-speed access time: 12, 15, 20, 25 ns
- Automatic power-down when chip is deselected
- CMOS low power operation
 - 450 mW (typical) operating
 - 250 μ W (typical) standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Two Chip Enables ($\overline{\text{CE1}}$ and CE2) for simple memory expansion

DESCRIPTION

The *ISSI* IS61C64AH is a very high-speed, low power, 8192-word by 8-bit static RAM. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 12 ns with low power consumption.

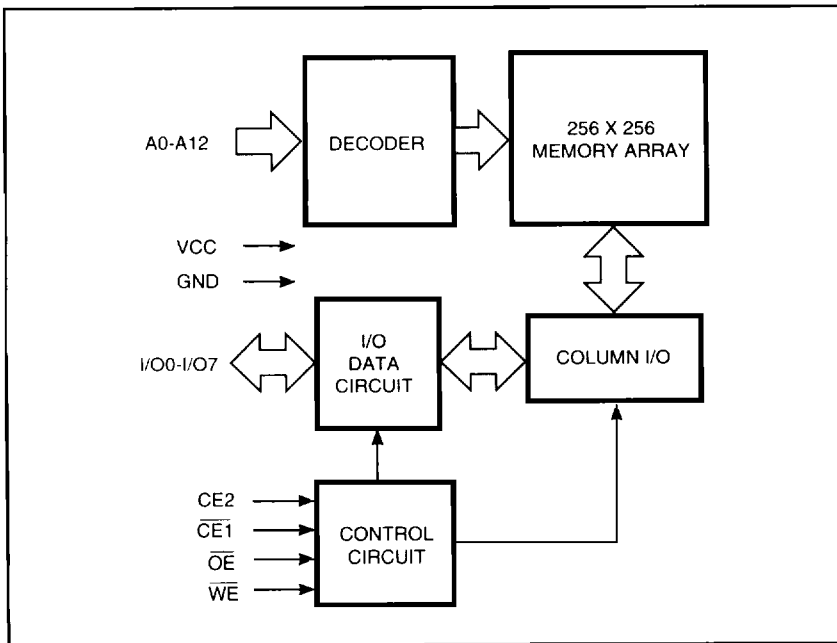
2

When $\overline{\text{CE1}}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250 μ W (typical) with CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{\text{CE1}}$ and CE2. The active LOW Write Enable ($\overline{\text{WE}}$) controls both writing and reading of the memory.

The IS61C64AH is packaged in the JEDEC standard 28-pin, 300-mil DIP and SOJ.

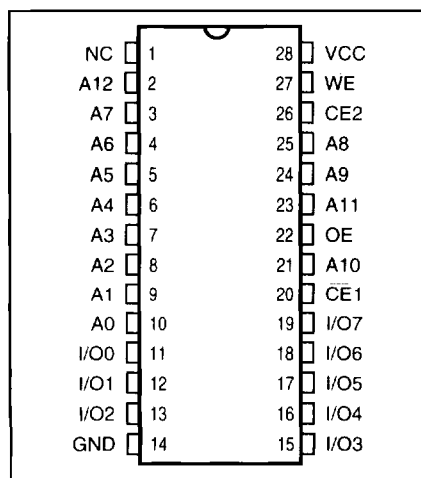
FUNCTIONAL BLOCK DIAGRAM



ISSI reserves the right to make changes to its products at any time without notice in order to improve design and supply the best possible product. We assume no responsibility for any errors which may appear in this publication. © Copyright 1995, Integrated Silicon Solution, Inc.

PIN CONFIGURATION

28-Pin DIP and SOJ



PIN DESCRIPTIONS

A0-A12	Address Inputs
CE1	Chip Enable 1 Input
CE2	Chip Enable 2 Input
OE	Output Enable Input
WE	Write Enable Input
I/O0-I/O7	Input/Output
Vcc	Power
GND	Ground

TRUTH TABLE

Mode	WE	CE1	CE2	OE	I/O Operation	Vcc Current
Not Selected (Power-down)	X	H	X	X	High-Z	IsB1, IsB2
Output Disabled	H	L	H	H	High-Z	Icc1, Icc2
Read	H	L	H	L	DOUT	Icc1, Icc2
Write	L	L	H	X	DIN	Icc1, Icc2

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	5V ± 10%
Industrial ⁽¹⁾	-40°C to +85°C	5V ± 10%

Notes:

1. Industrial supplement specification available upon request.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA	—	0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ⁽¹⁾		-0.5	0.8	V
I _I	Input Leakage	GND ≤ V _{IN} ≤ V _{CC}	-2	2	μA
I _O	Output Leakage	GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled	-2	2	μA

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	-12 ns		-15 ns		-20 ns		-25 ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{CC1}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = 0	—	95	—	80	—	80	—	80	mA
I _{CC2}	V _{CC} Dynamic Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX}	—	175	—	135	—	120	—	110	mA
I _{SB1}	TTL Standby Current (TTL Inputs)	V _{CC} = Max., V _{IN} = V _{IH} or V _{IL} , CE1 ≥ V _{IH} or CE2 ≤ V _{IL} , f = 0	—	30	—	20	—	20	—	20	mA
I _{SB2}	CMOS Standby Current (CMOS Inputs)	V _{CC} = Max., CE1 ≥ V _{CC} - 0.2V, CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0	—	10	—	6	—	6	—	6	mA

Notes:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.


READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

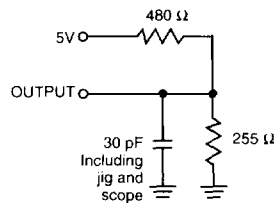
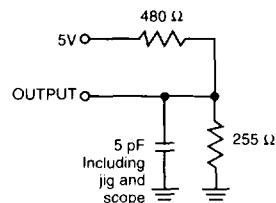
Symbol	Parameter	-12 ns		-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{OHA}	Output Hold Time	3	—	3	—	3	—	3	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	12	—	15	—	20	—	25	ns
t_{ACE2}	$\overline{CE2}$ Access Time	—	12	—	15	— <td 20	—	25	ns	
t_{DOE}	\overline{OE} Access Time	—	6	—	7	—	7	—	9	ns
$t_{LZOE}^{(2)}$	\overline{OE} to Low-Z Output	0	—	0	—	0	—	0	—	ns
$t_{HZOE}^{(2)}$	\overline{OE} to High-Z Output	—	5	—	6	—	7	—	9	ns
$t_{LZCE1}^{(2)}$	$\overline{CE1}$ to Low-Z Output	2	—	3	—	3	—	3	—	ns
$t_{LZCE2}^{(2)}$	$\overline{CE2}$ to Low-Z Output	2	—	3	—	3	—	3	—	ns
$t_{HZCE}^{(2)}$	$\overline{CE1}$ or $\overline{CE2}$ to High-Z Output	—	6	—	8	—	10	—	12	ns
$t_{PU}^{(3)}$	$\overline{CE1}$ or $\overline{CE2}$ to Power-Up	0	—	0	—	0	—	0	—	ns
$t_{PD}^{(3)}$	$\overline{CE1}$ or $\overline{CE2}$ to Power-Down	—	12	—	15	—	20	—	20	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

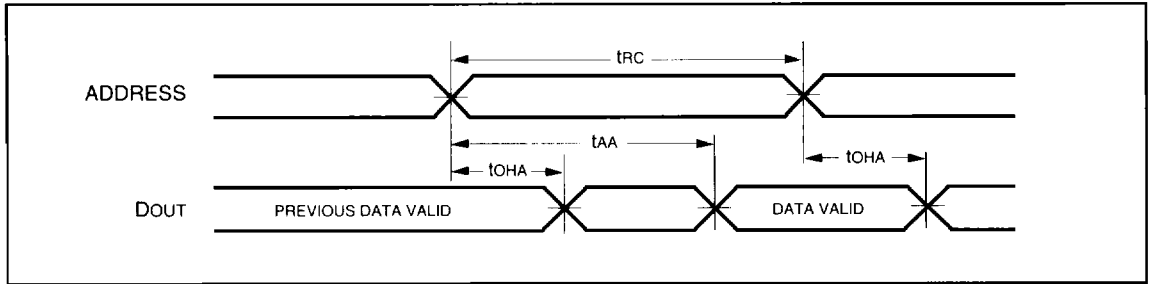
AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1a and 1b

AC TEST LOADS

Figure 1a.

Figure 1b.

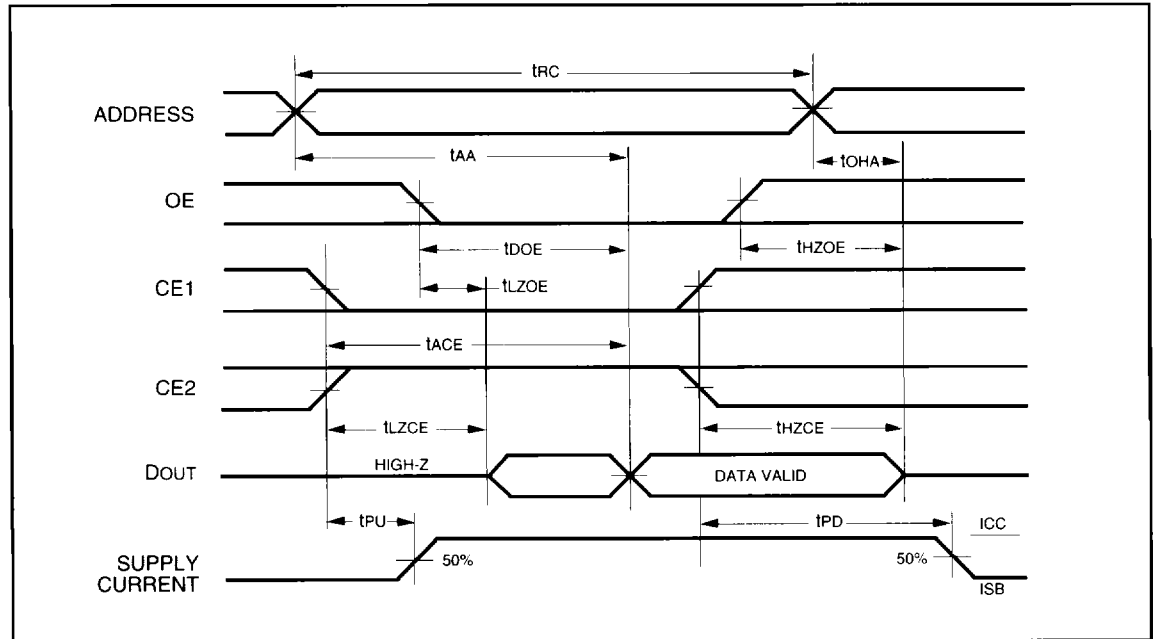
AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



2

READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and $CE2$ HIGH transitions.

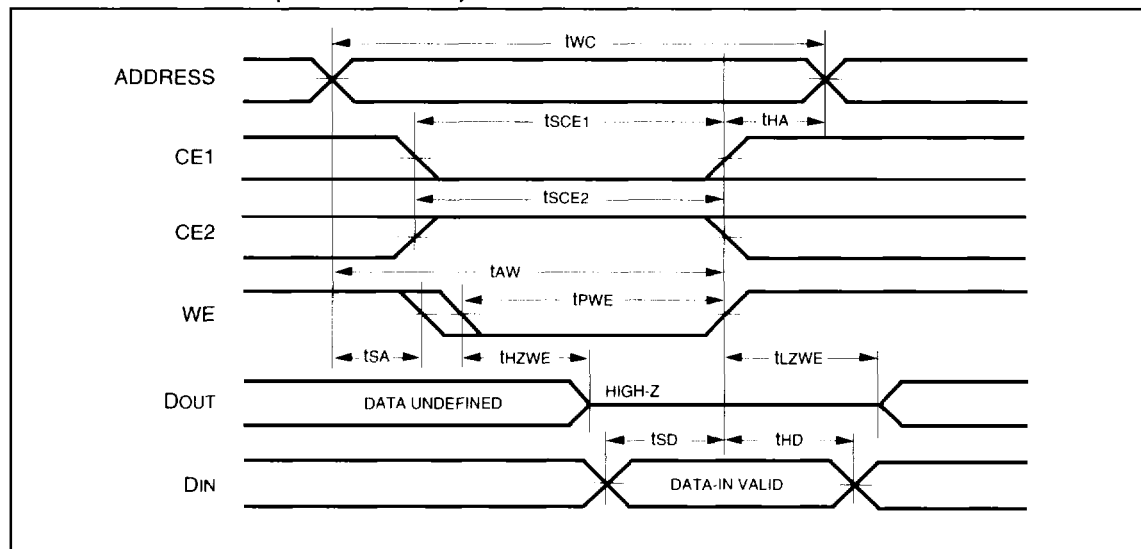
WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

Symbol	Parameter	-12 ns		-15 ns		-20 ns		-25 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t _{SCE1}	$\overline{CE1}$ to Write End	10	—	12	—	17	—	22	—	ns
t _{SCE2}	CE2 to Write End	10	—	12	—	17	—	22	—	ns
t _{AW}	Address Setup Time to Write End	10	—	12	—	15	—	20	—	ns
t _{HA}	Address Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{SA}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t _{PWE} ⁽⁴⁾	\overline{WE} Pulse Width	8	—	10	—	12	—	15	—	ns
t _{SD}	Data Setup to Write End	8	—	9	—	10	—	12	—	ns
t _{HD}	Data Hold from Write End	0	—	0	—	0	—	0	—	ns
t _{HZWE} ⁽²⁾	\overline{WE} LOW to High-Z Output	—	6	—	8	—	10	—	12	ns
t _{LZWE} ⁽²⁾	\overline{WE} HIGH to Low-Z Output	0	—	0	—	0	—	0	—	ns

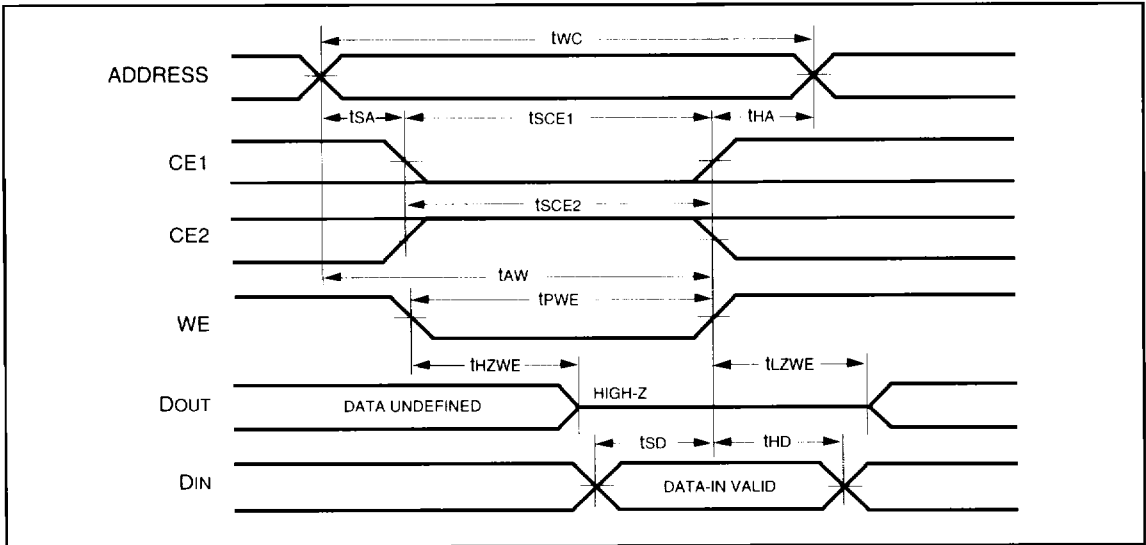
Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.

AC WAVEFORMS

WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)

WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)^(1,2)



2

Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if $\overline{OE} = V_{IH}$.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
12	IS61C64AH-12N	300-mil Plastic DIP
12	IS61C64AH-12J	300-mil Plastic SOJ
15	IS61C64AH-15N	300-mil Plastic DIP
15	IS61C64AH-15J	300-mil Plastic SOJ
20	IS61C64AH-20N	300-mil Plastic DIP
20	IS61C64AH-20J	300-mil Plastic SOJ
25	IS61C64AH-25N	300-mil Plastic DIP
25	IS61C64AH-25J	300-mil Plastic SOJ