

Dual 4 to 1 Multiplexer

The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- Power Dissipation, 305 mW Typical
- Improved Noise Margin 150 mV (over operating voltage and temperature range)
- Voltage Compensated
- MECL 10K-Compatible

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply ($V_{CC} = 0$)	V_{EE}	-8.0 to 0	Vdc
Input Voltage ($V_{CC} = 0$)	V_I	0 to V_{EE}	Vdc
Output Current— Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range— Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS ($V_{EE} = -5.2 V \pm 5\%$) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	80	—	73	—	80	mA
Input Current High Pins 3-7 & 9-13 Pin 14	I_{inH}	—	475	—	300	—	300	μ Adc
		—	670	—	420	—	420	
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μ A
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

AC PARAMETERS

Propagation Delay	t_{pd}	0.7	2.4	0.8	2.5	0.9	2.6	ns
Data								
Select (A, B)		1.0	2.8	1.1	2.9	1.2	3.2	
Enable		0.4	1.45	0.4	1.5	0.5	1.7	
Rise Time	t_r	0.5	1.5	0.5	1.6	0.5	1.7	ns
Fall Time	t_f	0.5	1.5	0.5	1.6	0.5	1.7	ns

NOTE:

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

MC10H174



L SUFFIX
CERAMIC PACKAGE
CASE 620-10



P SUFFIX
PLASTIC PACKAGE
CASE 648-08



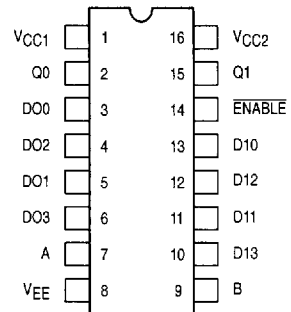
FN SUFFIX
PLCC
CASE 775-02

TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
	B	A	Z	W
H	X	X	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

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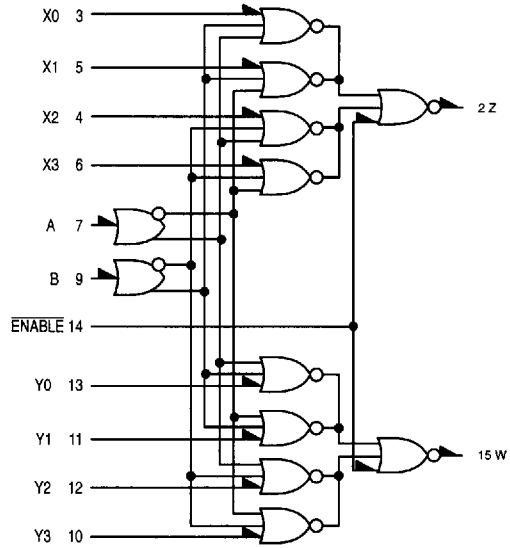
DIP PIN ASSIGNMENT



Pin assignment is for Dual-in-Line Package. For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.



LOGIC DIAGRAM



VCC1 = PIN 1
VCC2 = PIN 16
VEE = PIN 8

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