4Mx18, 2Mx36
72Mb QUAD (Burst 2) Synchronous SRAM

ADVANCED INFORMATION
SEPTEMBER 2010

FEATURES

- 2Mx36 and 4Mx18 configuration available.
- On-chip delay-locked loop (DLL) for wide data valid window.
- Separate read and write ports with concurrent read and write operations.
- Synchronous pipeline read with EARLY write operation.
- Double data rate (DDR) interface for read and write input ports.
- Fixed 2-bit burst for read and write operations.
- Clock stop support.
- Two input clocks (K and K#) for address and control registering at rising edges only.
- Two output clocks (C and C#) for data output control.
- Two echo clocks (CQ and CQ#) that are delivered simultaneously with data.
- +1.8V core power supply and 1.5, 1.8V VDDQ, used with 0.75, 0.9V VREF.
- HSTL input and output levels.
- Registered addresses, write and read controls, byte writes, data in, and data outputs.
- Full data coherency.
- Boundary scan using limited set of JTAG 1149.1 functions.
- Byte write capability.
- Fine ball grid array (FBGA) package:
  13mmx15mm and 15mmx17mm body size
  165-ball (11 x 15) array
- Programmable impedance output drivers via 5x user-supplied precision resistor.

DESCRIPTION

The 72Mb IS61QDB22M36A and IS61QDB24M18A are synchronous, high-performance CMOS static random access memory (SRAM) devices. These SRAMs have separate I/Os, eliminating the need for high-speed bus turnaround. The rising edge of K clock initiates the read/write operation, and all internal operations are self-timed. Refer to the *Timing Reference Diagram for Truth Table* for a description of the basic operations of these QUAD (Burst of 2) SRAMs.

The input address bus operates at double data rate. The following are registered internally on the rising edge of the K clock:

- Read address
- Read enable
- Write enable
- Byte writes
- Data-in for early writes

The following are registered on the rising edge of the K# clock:

- Write address
- Byte writes
- Data-in for second burst addresses

Byte writes can change with the corresponding data-in to enable or disable writes on a per-byte basis. An internal write buffer enables the data-ins to be registered half a cycle earlier than the write address. The first data-in burst is clocked at the same time as the write command signal, and the second burst is timed to the following rising edge of the K# clock.

During the burst read operation, the data-outs from the first bursts are updated from output registers of the second rising edge of the C# clock (starting 1.5 cycles later after read command). The data-outs from the second bursts are updated with the third rising edge of the C clock. The K and K# clocks are used to time the data-outs whenever the C and C# clocks are tied high.

The device is operated with a single +1.8V power supply and is compatible with HSTL I/O interfaces.

Package ballout and description

x36 FBGA Ball Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA[1]	SA	W#	BW_2#	K#	BW_1#	R#	SA	NC/SA[1]	CQ
B	Q27	Q18	D18	SA	BW_3#	K	BW_0#	SA	D17	Q17	Q8
C	D27	Q28	D19	V_{SS}	SA	SA	SA	V_{SS}	D16	Q7	D8
D	D28	D20	Q19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q16	D15	D7
E	Q29	D29	Q20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q13	D13	D5
H	Doff#	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	D31	Q31	D23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D10	Q1	D2
N	D34	D26	Q25	V_{SS}	SA	SA	SA	V_{SS}	Q10	D9	D1
P	Q35	D35	Q26	SA	SA	C	SA	SA	Q9	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

Notes:
1. The following balls are reserved for higher densities: 10A for 144Mb, and 2A for 288Mb.

x18 FBGA Ball Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/SA[1]	SA	W#	BW_1#	K#	NC/SA[1]	R#	SA	SA	CQ
B	NC	Q9	D9	SA	NC	K	BW_0#	SA	NC	NC	Q8
C	NC	NC	D10	V_{SS}	SA	SA	SA	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	Doff#	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	D1
P	NC	NC	Q17	SA	SA	C	SA	SA	NC	D0	Q0
R	TDO	TCK	SA	SA	SA	C#	SA	SA	SA	TMS	TDI

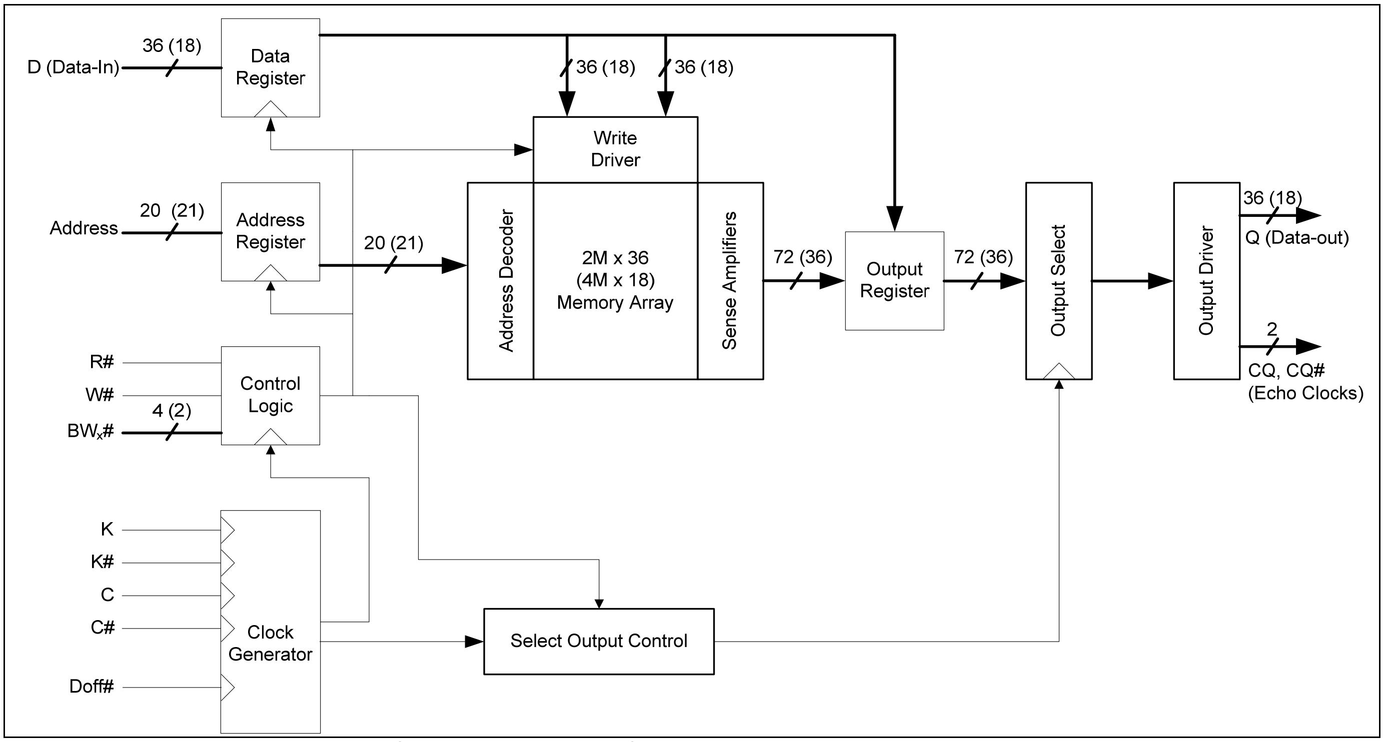
Notes:
1. The following balls are reserved for higher densities: 2A for 144Mb, and 7A for 288Mb.

Ball Descriptions

Symbol	Type	Description
K, K#	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain VREF level.
C, C#	Input	Input clock for output data. C and C# are used to clock out the READ data. They can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
CQ, CQ#	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tri-states.
Doff#	Input	DLL disable and reset input : when low, this input causes the DLL to be bypassed and reset the previous DLL information. When high, DLL will start operating and lock the frequency after tCK lock time. The device behaves in 1.0 read latency mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz.
SA	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. These inputs are ignored when device is deselected.
D0 - Dn	Input	Synchronous data inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See BALL CONFIGURATION figures for ball site location of individual signals. The x18 device uses D0~D17. D18~D35 should be treated as NC pin. The x36 device uses D0~D35.
Q0 - Qn	Output	Synchronous data outputs: Output data is synchronized to the respective C and C#, or to the respective K and K# if C and /C are tied to high. This bus operates in response to R# commands. See BALL CONFIGURATION figures for ball site location of individual signals. The x18 device uses Q0~Q17. Q18~Q35 should be treated as NC pin. The x36 device uses Q0~Q35.
W#	Input	Synchronous write: When low, this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
R#	Input	Synchronous read: When low, this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K.
BW_x#	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and #K for each of the two rising edges comprising the WRITE cycle. See Write Truth Table for signal to data relationship.
V_{REF}	-	HSTL input reference voltage: Nominally VDDQ/2, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.
V_{DD}	supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.
V_{DDQ}	supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.
V_{SS}	supply	Ground
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. Q and CQ output impedance are set to 0.2xRQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to VDDQ, which enables the minimum impedance mode. This ball cannot be connected directly to VSS or left unconnected. In ODT (On Die Termination) enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input.
TMS, TDI, TCK	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.
TDO	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to VSS if the JTAG function is not used in the circuit.
NC	-	No connect: These signals should be left floating or connected to ground to improve package heat dissipation.

SRAM Features description

Block Diagram



Note: Numerical values in parentheses refer to the x18 device configuration.

Read Operations

The SRAM operates continuously in a burst-of-two mode. Read cycles are started by registering R# in active low state at the rising edge of the K clock. A second set of clocks, C and C#, are used to control the timing to the outputs. A set of free-running echo clocks, CQ and CQ#, are produced internally with timings identical to the data-outs. The echo clocks can be used as data capture clocks by the receiver device.

When the C and C# clocks are connected high, then the K and K# clocks assume the function of those clocks. In this case, the data corresponding to the first address is clocked 1.5 cycles later by the rising edge of the K# clock. The data corresponding to the second burst is clocked 2 cycles later by the following rising edge of the K clock.

A NOP operation (R# is high) does not terminate the previous read.

Write Operations

Write operations can also be initiated at every rising edge of the K clock whenever W# is low. The write address is provided 0.5 cycles later, registered by the rising edge of K#. Again, the write always occurs in bursts of two.

The write data is provided in an ‘early write’ mode; that is, the data-in corresponding to the first address of the burst, is presented 0.5 cycles before the rising edge of the following K clock. The data-in corresponding to the second write burst address follows next, registered by the rising edge of K#.

The data-in provided for writing is initially kept in write buffers. The information in these buffers is written into the array on the third write cycle. A read cycle to the last write address produces data from the write buffers. Similarly, a read address followed by the same write address produces the latest write data. The SRAM maintains data coherency.

During a write, the byte writes independently control which byte of any of the four burst addresses is written (see *X18/X36 Write Truth Tables* and *Timing Reference Diagram for Truth Table*).

Whenever a write is disabled (W# is high at the rising edge of K), data is not written into the memory.

RQ Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to enable the SRAM to adjust its output driver impedance. The value of RQ must be 5x the value of the intended line impedance driven by the SRAM. For example, an RQ of 250Ω results in a driver impedance of 50Ω. The allowable range of RQ to guarantee impedance matching is between 175Ω and 350Ω with V_{DDQ}=1.5V. The RQ resistor should be placed less than two inches away from the ZQ ball on the SRAM module. The capacitance of the loaded ZQ trace must be less than 7.5pF.

The ZQ pin can also be directly connected to V_{DDQ} to obtain a minimum impedance setting. ZQ must never be connected to V_{SS}.

PROGRAMMABLE IMPEDANCE AND POWER-UP REQUIREMENTs

Periodic readjustment of the output driver impedance is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. At power-up, the driver impedance is in the middle of allowable impedances values. The final impedance value is achieved within 1024 clock cycles.

Single Clock Mode

This device can be also operated in single-clock mode. In this case, C and C# are both connected high at power-up and must never change. Under this condition, K and K# will control the output timings.

Either clock pair must have both polarities switching and must never connect to V_{REF}, as they are not differential clocks.

Depth Expansion

Separate input and output ports enable easy depth expansion, as each port can be selected and deselected independently. Read and write operations can occur simultaneously without affecting each other. Also, all pending read and write transactions are always completed prior to deselecting the corresponding port.

Delay Lock Loop (DLL)

Delay Lock Loop (DLL) is a new system to align the output data coincident with clock rising or falling edge to enhance the output valid timing characteristics. It is locked to the clock frequency and is constantly adjusted to match the clock frequency. Therefore device can have stable output over the temperature and voltage variation.

DLL has a limitation of locking range and jitter adjustment which are specified as tKHKH and tKCvar respectively in the AC timing characteristics. In order to turn this feature off, applying logic low to the Doff# pin will bypass this. In the DLL off mode, the device behaves with 1.0 cycle latency and a longer access time which is known in DDR-I or old QUAD mode.

The DLL can also be reset without power down by toggling Doff# pin low to high or stopping the input clocks K and K# for a minimum of 30ns.(K and K# must be stayed either at higher than VIH or lower than VIL level. Remaining Vref is not permitted.) DLL reset must be issued when power up or when clock frequency changes abruptly. After DLL being reset, it gets locked after 2048 cycles of stable clock.

Power-Up and Power-Down Sequences

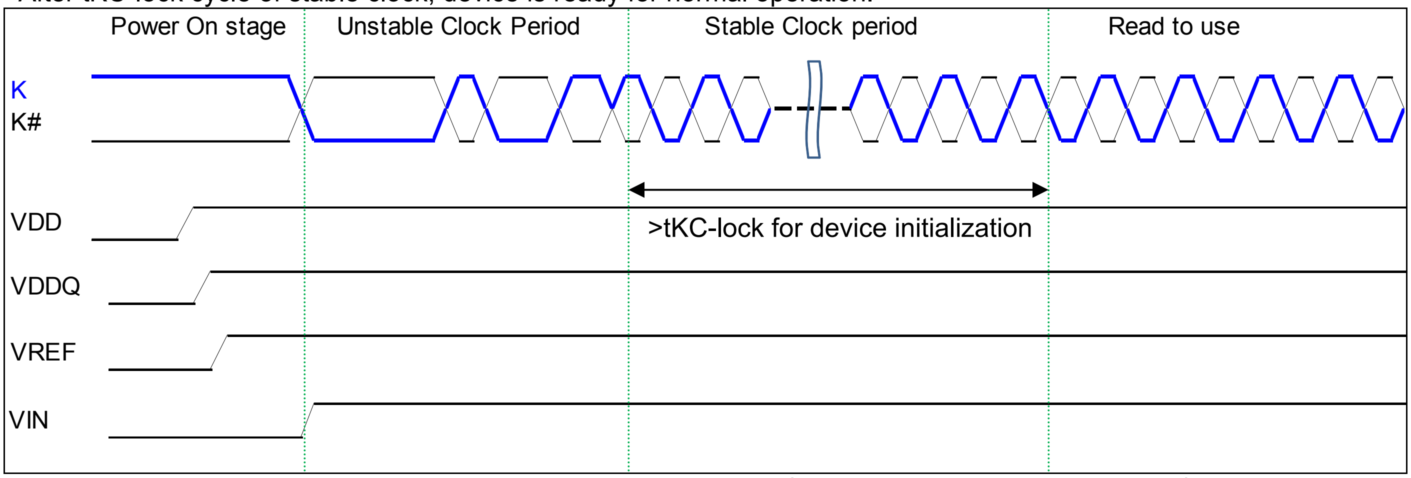
The recommendation of voltage apply sequence is : $V_{DD} \rightarrow V_{DDQ}$ 1) $\rightarrow V_{REF}$ 2) $\rightarrow V_{IN}$

Notes:
V_{DDQ} can be applied concurrently with V_{DD}.
V_{REF} can be applied concurrently with V_{DDQ}.

After power and clock signals are stabilized, device can be ready for normal operation after tKC-Lock cycles. In tKC-lock cycle period, device initializes internal logics and locks DLL. Depending on /Doff status, locking DLL will be skipped. The following timing pictures are possible examples of power up sequence.

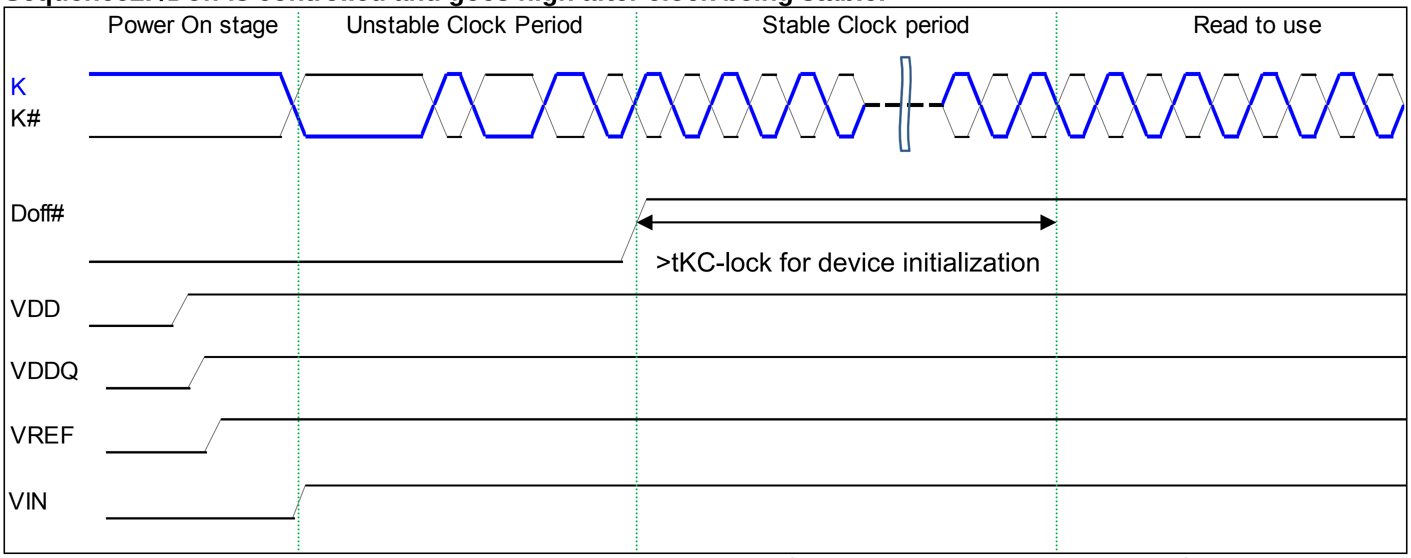
Sequence1. /Doff is fixed low

After tKC-lock cycle of stable clock, device is ready for normal operation.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Sequence2. /Doff is controlled and goes high after clock being stable.

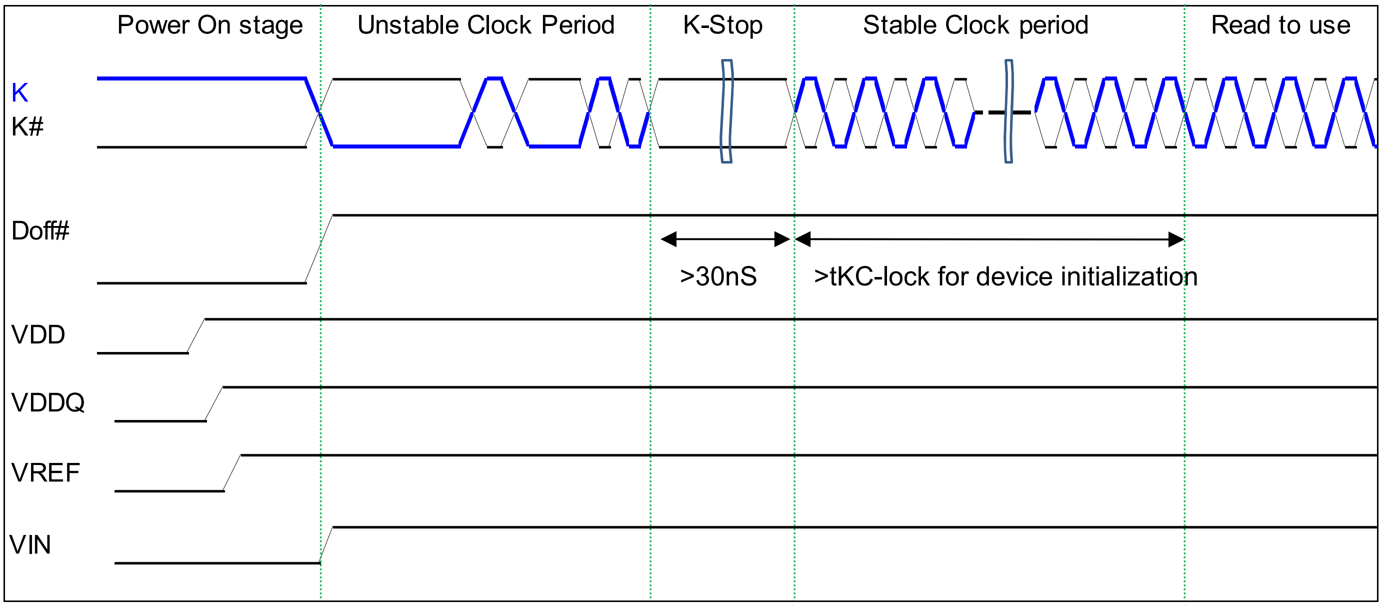


Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Sequence3. /Doff is controlled but goes high before clock being stable.

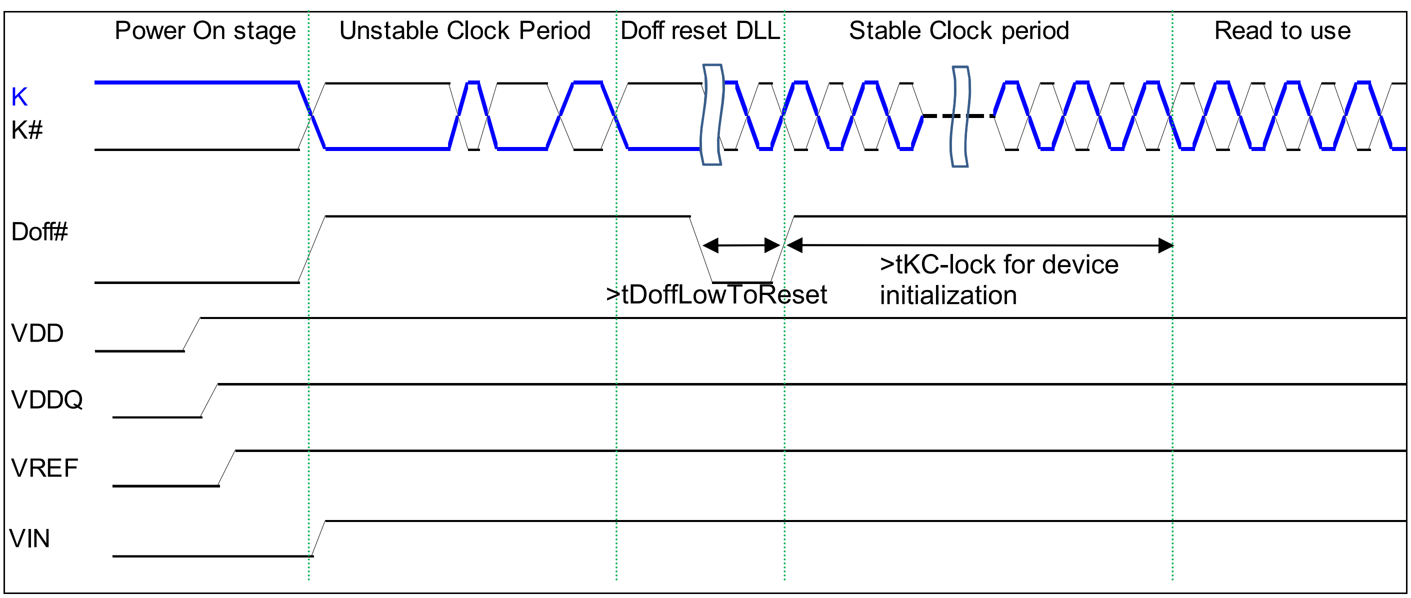
Because DLL has a risk to be locked with the unstable clock, DLL needs to be reset and locked with the stable input.

a) K-stop to reset. If K or K# stays at VIH or VIL for more than 30nS, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

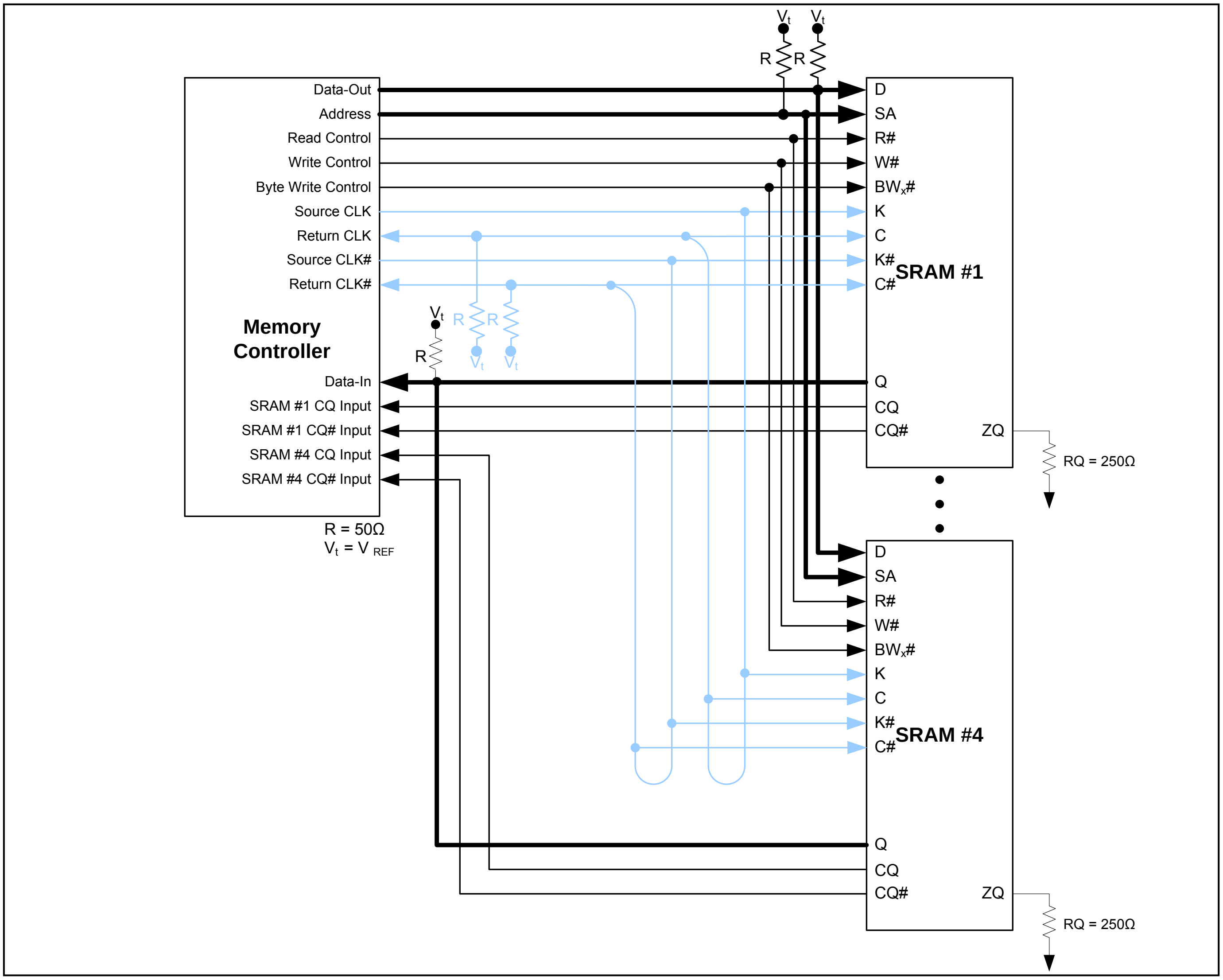
a) /Doff Low to reset. If /Doff toggled low to high, DLL will be reset and ready to re-lock. In tKC-Lock period, DLL will be locked with a new stable value. Device can be ready for normal operation after that.



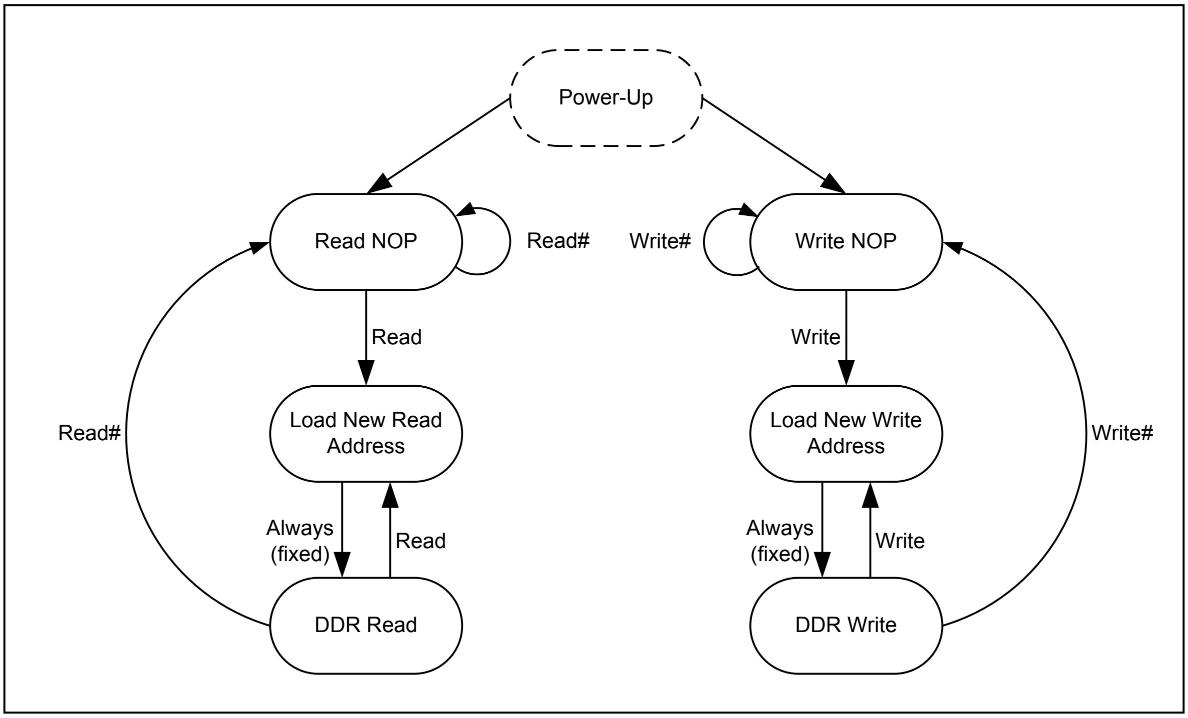
Note) Applying DLL reset sequences (sequence 3a, 3b) are also required when operating frequency is changed without power off.
Note) All inputs including clocks must be either logically High or Low during Power On stage. Timing above shows only one of cases.

Application Example

In the following application example, the second pair of C and C# clocks is delayed such that the return data meets the data setup and hold times at the memory controller.



State Diagram

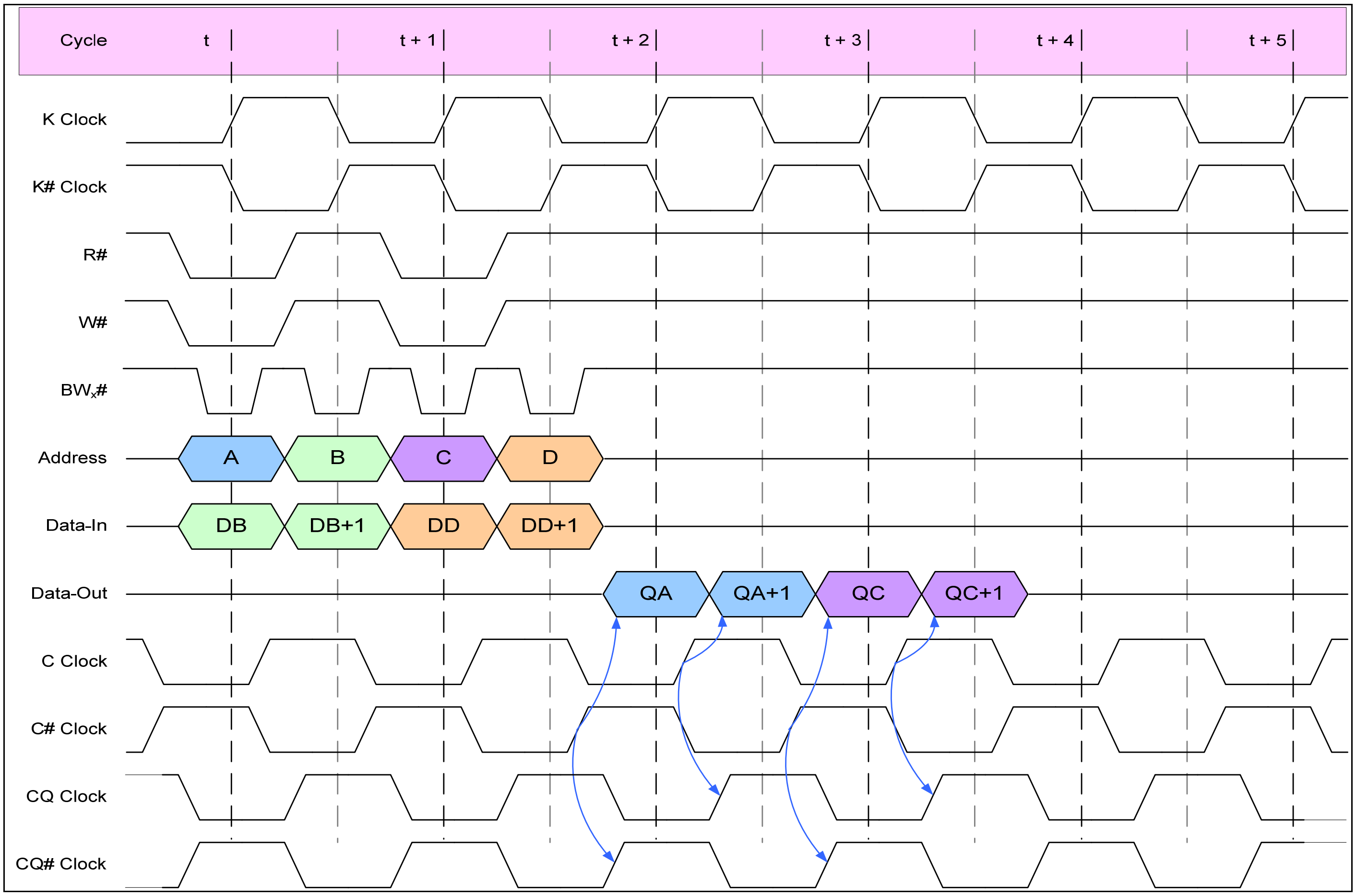


Notes:

1. Internal burst counter is fixed as two-bit linear; that is when first address is A0+0, next internal burst addresses are A0+1.
2. **Read** refers to read active status with R# = LOW. **Read#** refers to read inactive status with R# = HIGH.
3. **Write** refers to write active status with W# = LOW. **Write#** refers to write inactive status with W# = HIGH.
4. The read and write state machines can be active simultaneously.
5. State machine control timing sequence is controlled by K.

Timing Reference Diagram for Truth Table

The *Timing Reference Diagram for Truth Table* is helpful in understanding the *Clock and Write Truth Tables*, as it shows the cycle relationship between clocks, address, data in, data out, and control signals. Read command is issued at the beginning of cycle "t". Write command is issued at the beginning of cycle "t+1".



Clock Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Mode	Clock	Controls		Data In		Data Out	
	K	R#	W#	D_B	D_{B+1}	Q_A	Q_{A+1}
Stop Clock	Stop	X	X	Previous State	Previous State	Previous State	Previous State
No Operation (NOP)	L → H	H	H	X	X	High-Z	High-Z
Read A	L → H	L	X	X	X	D_{OUT} at C# (t+1.5)	D_{OUT} at C (t+2.0)
Write B	L → H	X	L	D_{IN} at K (t)	D_{IN} at K# (t+0.5)	X	X

Notes:
1. Internal burst counter is always fixed as two-bit.
2. X = "don't care"; H = logic "1"; L = logic "0".
3. A read operation is started when control signal R# is active low
4. A write operation is started when control signal W# is active low.
5. For timing definitions, refer to the *AC Timing Characteristics* table. Signals must meet AC specifications at timings indicated in parenthesis with respect to switching clocks K, K#, C and C#.

x18 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Operation	K (t)	K# (t+0.5)	BW_0#	BW_1#	D_B	D_{B+1}
Write Byte 0	L → H		L	H	D0-8 (t)	
Write Byte 1	L → H		H	L	D9-17 (t)	
Write All Bytes	L → H		L	L	D0-17 (t)	
Abort Write	L → H		H	H	Don't Care	
Write Byte 0		L → H	L	H		D0-8 (t+0.5)
Write Byte 1		L → H	H	L		D9-17 (t+0.5)
Write All Bytes		L → H	L	L		D0-17 (t+0.5)
Abort Write		L → H	H	H		Don't Care

Notes:
1. Refer to the *Timing Reference Diagram for Truth Table*. Cycle time starts at n and is referenced to the K clock.
2. For all cases, W# needs to be active low during the rising edge of K occurring at time t.
3. For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

x36 Write Truth Table

(Use the following table with the *Timing Reference Diagram for Truth Table*.)

Operation	K (t)	K# (t+0.5)	BW_0#	BW_1#	BW_2#	BW_3#	D_B	D_{B+1}
Write Byte 0	L → H		L	H	H	H	D0-8 (t)	
Write Byte 1	L → H		H	L	H	H	D9-17 (t)	
Write Byte 2	L → H		H	H	L	H	D18-26 (t)	
Write Byte 3	L → H		H	H	H	L	D27-35 (t)	
Write All Bytes	L → H		L	L	L	L	D0-35 (t)	
Abort Write	L → H		H	H	H	H	Don't Care	
Write Byte 0		L → H	L	H	H	H		D0-8 (t+0.5)
Write Byte 1		L → H	H	L	H	H		D9-17 (t+0.5)
Write Byte 2		L → H	H	H	L	H		D18-26 (t+0.5)
Write Byte 3		L → H	H	H	H	L		D27-35 (t+0.5)
Write All Bytes		L → H	L	L	L	L		D0-35 (t+0.5)
Abort Write		L → H	H	H	H	H		Don't Care

Notes:
1. For all cases, W# needs to be active low during the rising edge of K occurring at time t.
2. For timing definitions refer to the *AC Timing Characteristics* table. Signals must meet AC specifications with respect to switching clocks K and K#.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	–0.5	2.9	V
I/O Power Supply Voltage	V_{DDQ}	–0.5	2.9	V
DC Input Voltage	V_{IN}	–0.5	V_{DD}+0.3	V
Data Out Voltage	V_{DOUT}	–0.5	2.6	°C
Junction Temperature	T_J	-	110	°C
Storage Temperature	T_{STG}	–55	+125	°C

Note:
Stresses greater than those listed in this table can cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Temperature Range

Temperature Range	Symbol	Min	Max	Units
Commercial	T_A	0	+70	°C
Industrial	T_A	–40	+85	°C

DC Electrical Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%)

Parameter	Symbol	Min	Max	Units	Notes
x36 Average Power Supply Operating Current (I_{OUT}=0, V_{IN}=V_{IH} or V_{IL})	I_{DD30} I_{DD33} I_{DD40}	–	1200 1100 1000	mA	1, 2
x18 Average Power Supply Operating Current (I_{OUT}=0, V_{IN}=V_{IH} or V_{IL})	I_{DD30} I_{DD33} I_{DD40}	–	1150 1050 950	mA	1, 2
Power Supply Standby Current (R#=V_{IH}, W#=V_{IH}. All other inputs=V_{IH} or V_{IL}, I_{IH}=0)	I_{SB30} I_{SB33} I_{SB40}	–	290 280 270	mA	1,2
Input leakage current (0 ≤V_{IN}≤V_{DDQ} for all input balls except V_{REF}, ZQ, TCK, TMS, TDI ball)	I_{LI}	–2	+2	μA	3
Output leakage current (0 ≤V_{OUT} ≤V_{DDQ} for all output balls except TDO ball; Output must be disabled.)	I_{LO}	–2	+2	μA	
Output "high" level voltage (I_{OH}=-0.1mA, ZQnorm)	V_{OH}	V_{DDQ}–0.2	V_{DDQ}	V	
Output "low" level voltage (I_{OL}=+0.1mA, ZQnorm)	V_{OL}	V_{SS}	V_{SS}+0.2	V	

Notes:
1. I_{OUT} = chip output current.
2. The numeric suffix indicates the part operating at speed, as indicated in *AC Timing Characteristics table* (that is, I_{DD25} indicates 2.5ns cycle time).
3. DOFF# Ball does not follow this spec, I_{LI} = ±5uA

Recommended DC Operating Conditions

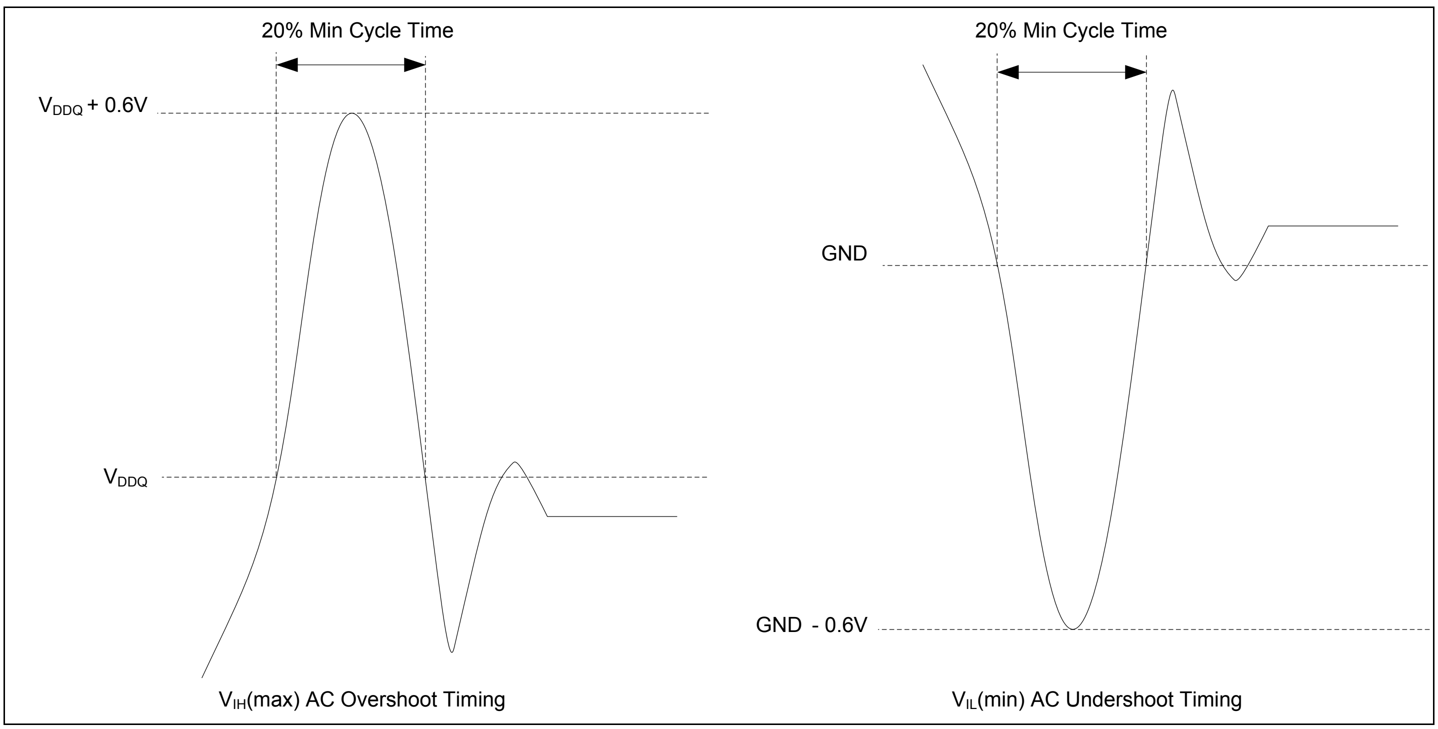
(Over the Operating Temperature Range)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Supply Voltage	V_{DD}	1.8–5%	1.8	1.8+5%	V	1
Output Driver Supply Voltage	V_{DDQ}	1.4	1.5	V_{DD}	V	1
Input High Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.2	V	1, 2
Input Low Voltage	V_{IL}	–0.2	-	V_{REF} –0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.95	V	1, 5
Clock Signal Voltage	V_{IN-CLK}	–0.2	-	V_{DDQ}+0.2	V	1, 4

Notes:

1. All voltages are referenced to V_{SS}. All V_{DD}, V_{DDQ}, and V_{SS} pins must be connected.
2. V_{IH}(Max) AC = See *0vershoot and Undershoot Timings*.
3. V_{IL}(Min) AC = See *0vershoot and Undershoot Timings*.
4. V_{IN-CLK} specifies the maximum allowable DC excursions of each clock (K, K#, C, and C#).
5. Peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

Overshoot and Undershoot Timings

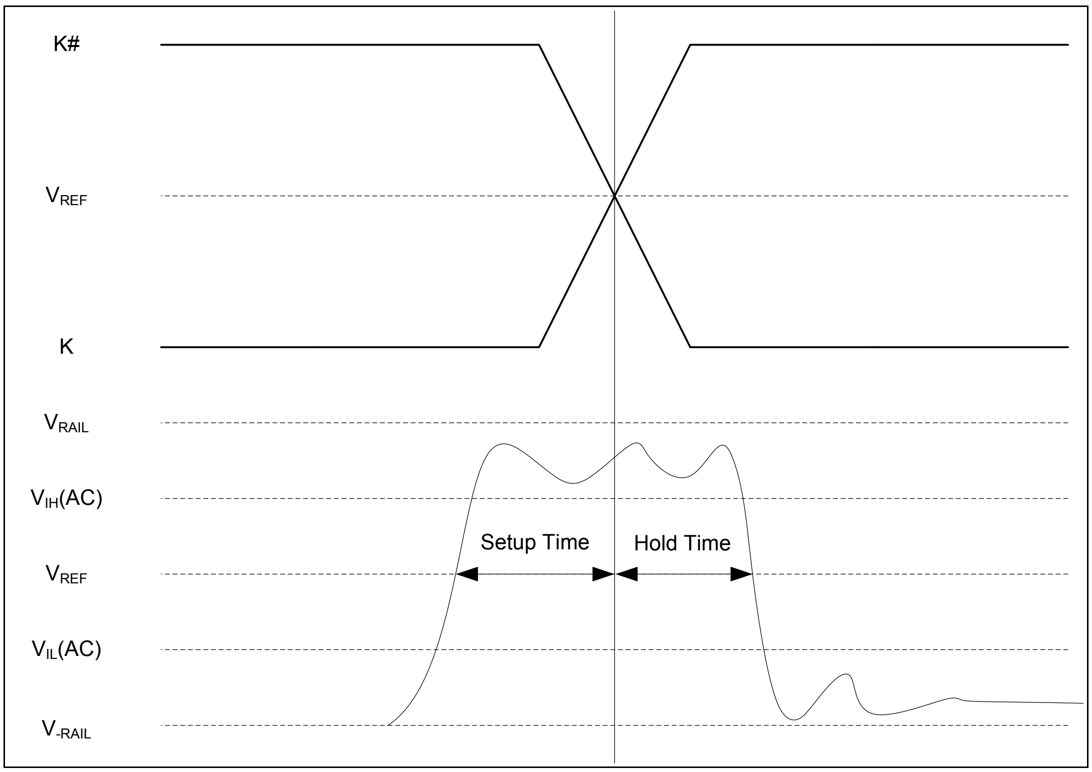


Typical AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic HIGH	V_{IH} (AC)	V_{REF}+0.2		V	1, 2, 3, 4
AC Input Logic LOW	V_{IL} (AC)		V_{REF}–0.2	V	1, 2, 3, 4
Clock Input Logic HIGH	V_{IH-CLK} (AC)	V_{REF}+0.2		V	1, 2, 3
Clock Input Logic LOW	V_{IL-CLK} (AC)		V_{REF}–0.2	V	1, 2, 3

Notes:
1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. Performance is a function of V_{IH} and V_{IL} levels to clock inputs.
3. See the *AC Input Definition* diagram.
4. See the *AC Input Definition* diagram. The signals should swing monotonically with no steps rail-to-rail with input signals never ringing back past V_{IH} (AC) and V_{IL} (AC) during the input setup and input hold window. V_{IH} (AC) and V_{IL} (AC) are used for timing purposes only.

AC Input Definition



PBGA Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal resistance from junction to ambient (airflow = 1m/s)	$R_{\theta JA}$	TBD	°C/W
Thermal resistance from junction to pins	$R_{\theta JB}$	TBD	°C/W
Thermal resistance from junction to case	$R_{\theta JC}$	TBD	°C/W

Note: these parameters are guaranteed by design and tested by a sample basis only.

Pin Capacitance

Parameter	Symbol	Test Condition	Max	Units
Input or output capacitance except D and Q pins	C_{IN} ,C_O	T_A = 25°C, f = 1 MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V	5	pF
D and Q capacitance (D0–Dx, Q0-Qx)	C_{DQ}		6	pF
Clocks Capacitance (K, K, C, C)	C_{CLK}		4	pF

Note: these parameters are guaranteed by design and tested by a sample basis only.

PROGRAMMABLE IMPEDANCE OUTPUT DRIVER DC ELECTRICAL CHARACTERISTICS

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Min	Max	Units	Notes
Output Logic HIGH Voltage	V_{OH}	V_{DDQ}/2 -0.12	V_{DDQ}/2 + 0.12	V	1, 3
Output Logic LOW Voltage	V_{OL}	V_{DDQ}/2 -0.12	V_{DDQ}/2 + 0.12	V	2, 3

Notes:

1. For 175Ω ≤ RQ ≤ 350Ω:

$$|I_{OH}| = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{RQ}{5}\right)}$$

2. For 175Ω ≤ RQ ≤ 350Ω:

$$|I_{OL}| = \frac{\left(\frac{V_{DDQ}}{2}\right)}{\left(\frac{RQ}{5}\right)}$$

3. Parameter Tested with RQ=250Ω and V_{DDQ}=1.5V

AC Test Conditions

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

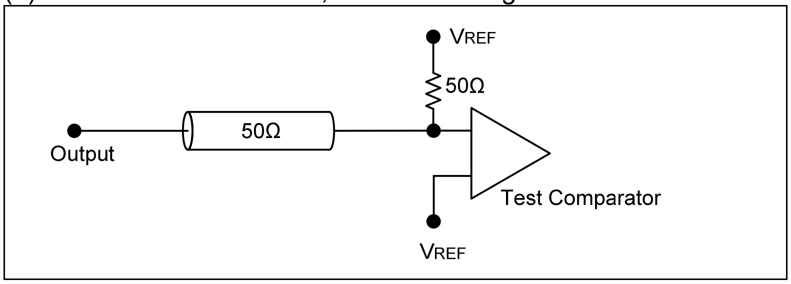
Parameter	Symbol	Conditions	Units	Notes
Output Drive Power Supply Voltage	V_{DDQ}	1.5/1.8	V	
Input Logic HIGH Voltage	V_{IH}	V_{REF}+0.5	V	
Input Logic LOW Voltage	V_{IL}	V_{REF}–0.5	V	
Input Reference Voltage	V_{REF}	0.75/0.9	V	
Input Rise Time	T_R	2.0	V/ns	
Input Fall Time	T_F	2.0	V/ns	
Output Timing Reference Level		V_{REF}	V	
Clock Reference Level		V_{REF}	V	
Output Load Conditions				1, 2

Notes:

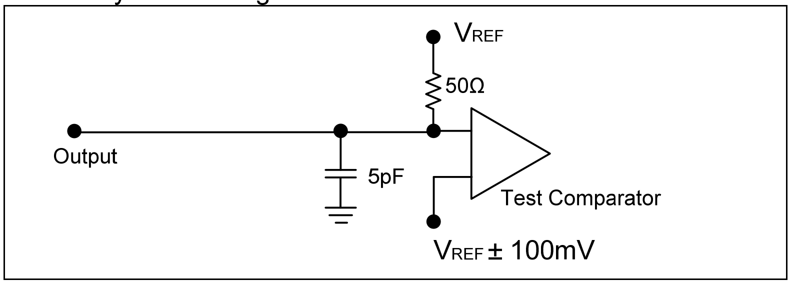
1. See *AC Test Loading.*
2. Parameter Tested with RQ=250Ω and V_{DDQ}=1.5V

AC Test Loading

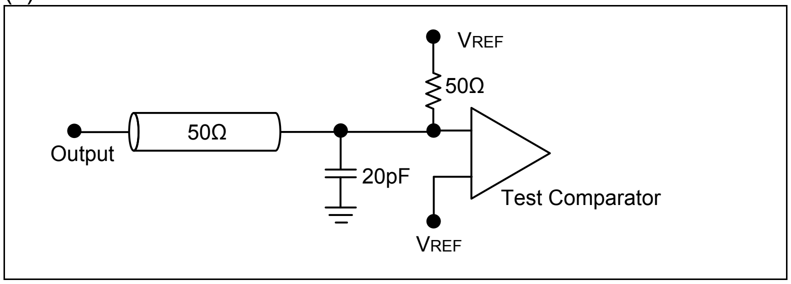
(a) Unless otherwise noted, AC test loading assume this condition.



(b) tCHQZ and tCHQX1 are specified with 5pF load capacitance and measured when transition occurs ±100mV from the steady state voltage.



(c)TDO



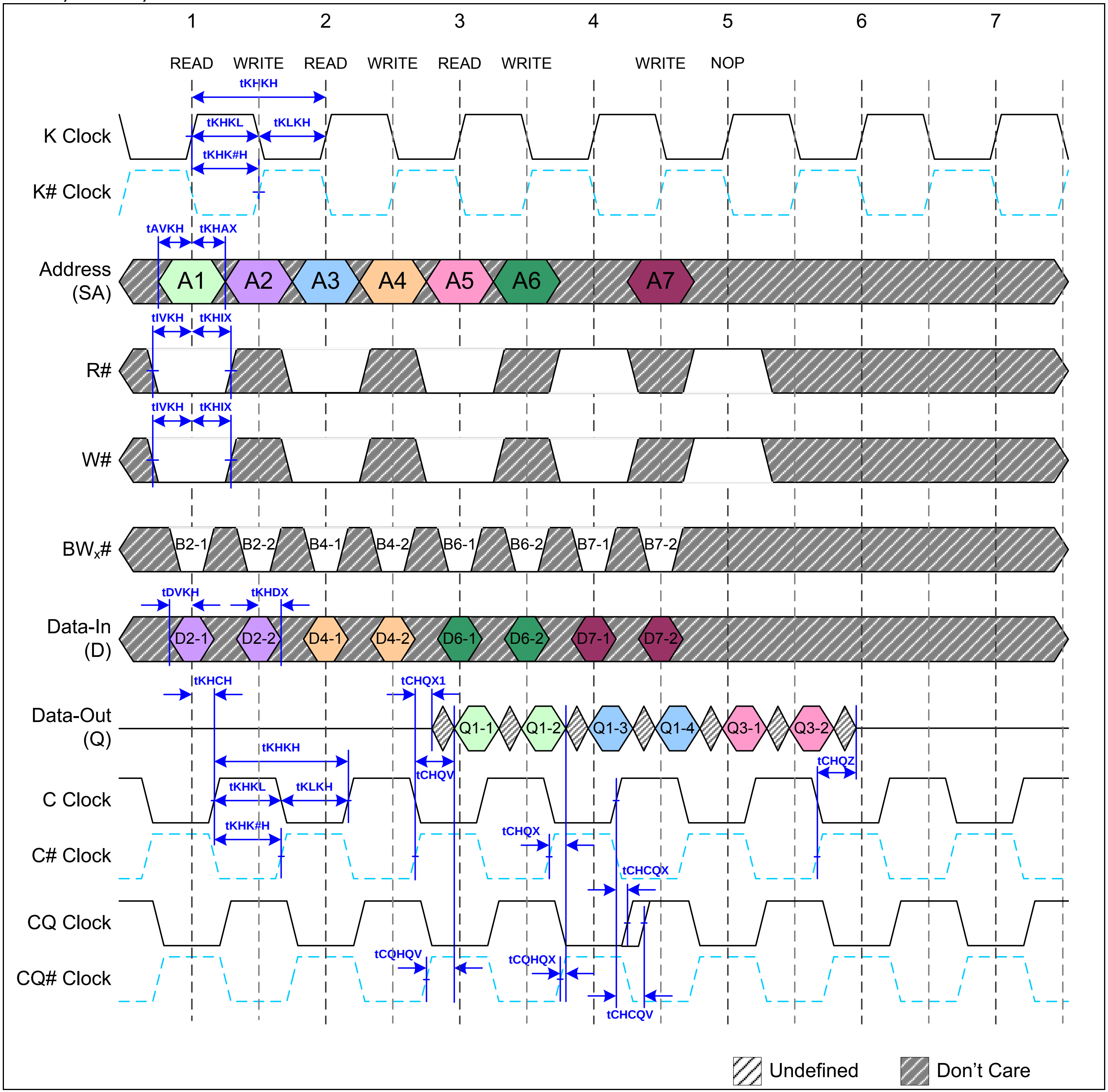
AC Timing Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	30 (333MHz)		33 (300MHz)		40 (250MHz)		unit	notes
		Min	Max	Min	Max	Min	Max		
Clock									
Clock Cycle Time (K, K#,C,C#)	tKHKH	3.00	8.4	3.33	8.4	4.00	8.4	ns	
Clock Phase Jitter (K, K#,C,C#)	tKC var		0.3		0.3		0.3	ns	4
Clock High Time (K, K#,C,C#)	tKHKL	0.4		0.4		0.4		cycle	
Clock Low Time (K, K#,C,C#)	tKLKH	0.4		0.4		0.4		cycle	
Clock to Clock (K_H→ $K\#_H$, C_H→ $C\#_H$)	tKHK#H	1.35		1.50		1.80		ns	
Clock to Data Clock (K > C, K# > C#)	tKHCH	0	1.35	0	1.48	0	1.8	ns	
DLL Lock Time (K,C)	tKC lock	1024		1024		1024		cycles	5
Doff Low period to DLL reset	tDoffLowToReset	5		5		5		ns	
K static to DLL reset	tKCreset	30		30		30		ns	
Output Times									
C,C# High to Output Valid	tCHQV		0.45		0.45		0.45	ns	1,3
C,C# High to Output Hold	tCHQX	-0.45		-0.45		-0.45		ns	1,3
C,C# High to Echo Clock Valid	tCHCQV		0.45		0.45		0.45	ns	1
C,C# High to Echo Clock Hold	tCHCQX	-0.45		-0.45		-0.45		ns	1
CQ, CQ# High to Output Valid	tCQHQV		0.30		0.30		0.30	ns	1,3
CQ, CQ# High to Output Hold	tCQHQX	-0.30		-0.30		-0.30		ns	1,3
C,C# High to Output High-Z	tCHQZ		0.45		0.45		0.45	ns	1,3
C,C# High to Output Low-Z	tCHQX1	-0.45		-0.45		-0.45		ns	1,3
Setup Times									
Address valid to K rising edge	tAVKH	0.40		0.40		0.40		ns	2
R#,W# control inputs valid to K rising edge	tIVKH	0.40		0.40		0.40		ns	2
BW_x# control inputs valid to K rising edge	tIVKH2	0.30		0.30		0.30		ns	2
Data-in valid to K, K# rising edge	tDVKH	0.30		0.30		0.30		ns	2
Hold Times									
K rising edge to address hold	tKHAX	0.40		0.40		0.40		ns	2
K rising edge to R#,W# control inputs hold	tKHIX	0.40		0.40		0.40		ns	2
K rising edge to BW_x# control inputs hold	tKHIX2	0.30		0.30		0.30		ns	2
K, K# rising edge to data-in hold	tKHDX	0.30		0.30		0.30		ns	2

Notes:
1. All address inputs must meet the specified setup and hold times for all latching clock edges.
2. During normal operation, VIH, VIL, TRISE, and TFALL of inputs must be within 20% of VIH, VIL, TRISE, and TFALL of clock.
3. If C, C are tied high, then K, K become the references for C, C timing parameters.
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. V_{DD} slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.
6. The data sheet parameters reflect tester guard bands and test setup variations.
7. To avoid bus contention, at a given voltage and temperature tCHQX1 is bigger than tCHQZ. The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worst case at totally different test conditions (0 C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70 C, 1.7V) It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

READ, WRITE, AND NOP TIMING DIAGRAM



Notes:
1. If address A1 = A2, data Q1-1 = D2-1 and data Q1-2 = D2-2. Write data is forwarded immediately as read results.
2. B2-1 and B2-2 refer to all BWx# byte controls for D2-1 and D2-2 respectively.
3. B4-1 and B4-2 refer to all BWx# byte controls for D4-1 and D4-2 respectively.
4. B6-1 and B6-2 refer to all BWx# byte controls for D6-1 and D6-2 respectively.
5. B7-1 and B7-2 refer to all BWx# byte controls for D7-1 and D7-2 respectively.
6. Outputs are disabled one cycle after a NOP.

IEEE 1149.1 TAP and Boundary Scan

The SRAM provides a limited set of JTAG functions to test the interconnection between SRAM I/Os and printed circuit board traces or other components. There is no multiplexer in the path from I/O pins to the RAM core.

In conformance with IEEE Standard 1149.1, the SRAM contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

The TAP controller has a standard 16-state machine that resets internally on power-up. Therefore, a TRST signal is not required

Disabling the JTAG feature

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (VSS) to prevent clocking of the device. TDI and TMS are internally pulled up and may be left disconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left disconnected. On power-up, the device will come up in a reset state, which will not interfere with device operation.

Test Access Port Signal List:

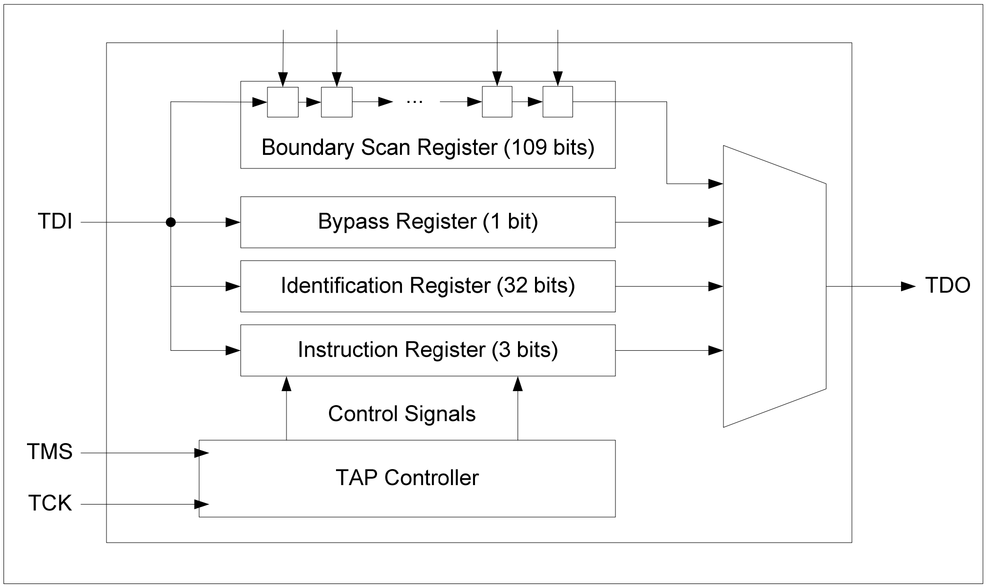
1. Test Clock (TCK)
This signal uses VDD as a power supply. The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

2. Test Mode Select (TMS)
This signal uses VDD as a power supply. The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK.

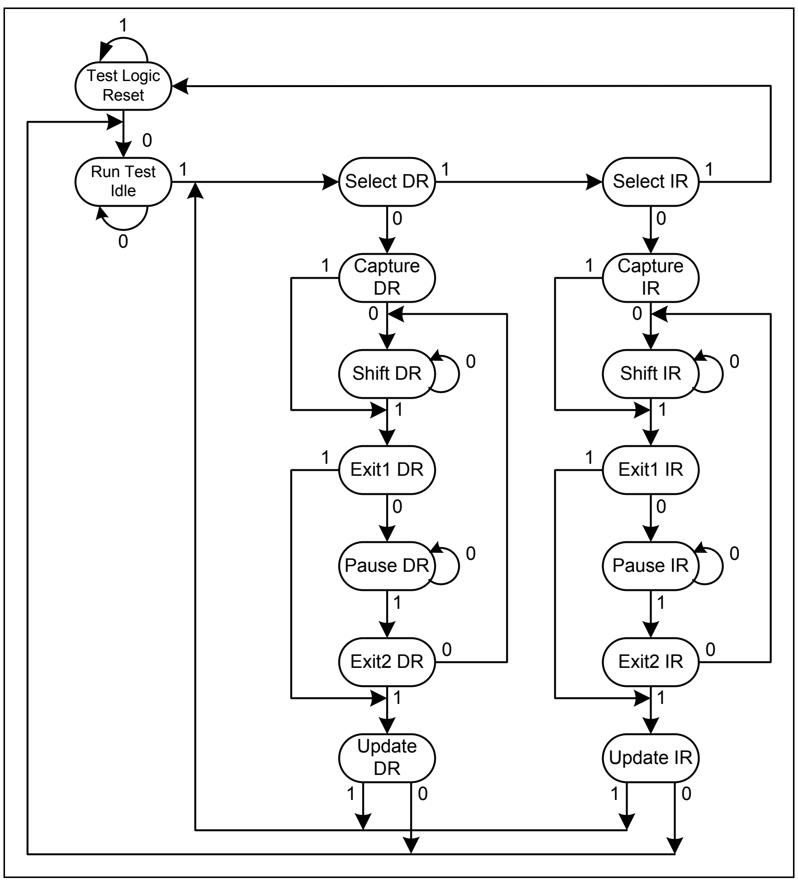
3. Test Data-In (TDI)
This signal uses VDD as a power supply. The TDI input is used to serially input test instructions and information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is connected to the most significant bit (MSB) of any register. For more information regarding instruction register loading, please see the TAP Controller State Diagram.

4. Test Data-Out (TDO)
This signal uses VDDQ as a power supply. The TDO output ball is used to serially clock test instructions and data out from the registers. The TDO output driver is only active during the Shift-IR and Shift-DR TAP controller states. In all other states, the TDO pin is in a High-Z state. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. For more information, please see the TAP Controller State Diagram.

TAP Controller State and Block Diagram



TAP Controller State Machine



Performing a TAP Reset

A Reset is performed by forcing TMS HIGH (VDD) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP Registers

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

1. Instruction Register
This register is loaded during the update-IR state of the TAP controller. At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section. When the TAP controller is in the capture-IR state, the two LSBs are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

2. Bypass Register
The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

3. Boundary Scan Register
The boundary scan register is connected to all the input and bidirectional balls on the SRAM. Several balls are also included in the scan register to reserved balls. The boundary scan register is loaded with the contents of the SRAM Input and Output ring when the TAP controller is in the capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the shift-DR state. Each bit corresponds to one of the balls on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

4. Identification (ID) Register
The ID register is loaded with a vendor-specific, 32-bit code during the capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the shift-DR state.

Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	109

TAP Instruction Set

Many instructions are possible with an eight-bit instruction register and all valid combinations are listed in the TAP Instruction Code Table. All other instruction codes that are not listed on this table are reserved and should not be used. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

1. EXTEST
The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output balls are used to apply a test vector, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD

instruction. Thus, during the update-IR state of EXTEST, the output driver is turned on, and the PRELOAD data is driven onto the output balls.

2. IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and allows the IDCODE to be shifted out of the device when the TAP controller enters the shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

3. SAMPLE Z

If the SAMPLE-Z instruction is loaded in the instruction register, all SRAM outputs are forced to an inactive drive state (high-Z), moving the TAP controller into the capture-DR state loads the data in the SRAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

4. SAMPLE/PRELOAD

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register. The user must be aware that the TAP controller clock can only operate at a frequency up to 50 MHz, while the SRAM clock operates significantly faster. Because there is a large difference between the clock frequencies, it is possible that during the capture-DR state, an input or output will undergo a transition. The TAP may then try to capture a signal while in transition. This will not harm the device, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible. To ensure that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time. The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/ PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register. Once the data is captured, it is possible to shift out the data by putting the TAP into the shift-DR state. This places the boundary scan register between the TDI and TDO balls.

6. BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

7. PRIVATE

Do not use these instructions. They are reserved for future use and engineering mode.

JTAG DC Operating Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%)

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{IH1}	1.3	V_{DD}+0.3	V	
JTAG Input Low Voltage	V_{IL1}	–0.3	0.5	V	
JTAG Output High Voltage	V_{OH1}	1.4	-	V	$\lvert I_{OH1}\rvert$=2mA
JTAG Output Low Voltage	V_{OL1}	-	0.4	V	I_{OL1}=2mA
JTAG Output High Voltage	V_{OH2}	1.6	-	V	$\lvert I_{OH2}\rvert$=100uA
JTAG Output Low Voltage	V_{OL2}	-	0.2	V	I_{OL2}=100uA
JTAG Input Leakage Current	I_{LIJTAG}	-5	+5	μA	0 ≤ Vin ≤ VDD
JTAG Output Leakage Current	I_{LOJTAG}	-5	+5	μA	0 ≤ Vout ≤ VDD

Notes:

1. All voltages referenced to VSS (GND); All JTAG inputs and outputs are LVTTL-compatible.
2. In "EXTEST" mode and "SAMPLE" mode, V_{DDQ} is nominally 1.5 V.

JTAG AC Test Conditions

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Conditions	Units
Input Pulse High Level	V_{IH1}	1.3	V
Input Pulse Low Level	V_{IL1}	0.5	V
Input Rise Time	T_{R1}	1.0	ns
Input Fall Time	T_{F1}	1.0	ns
Input and Output Timing Reference Level		0.9	V

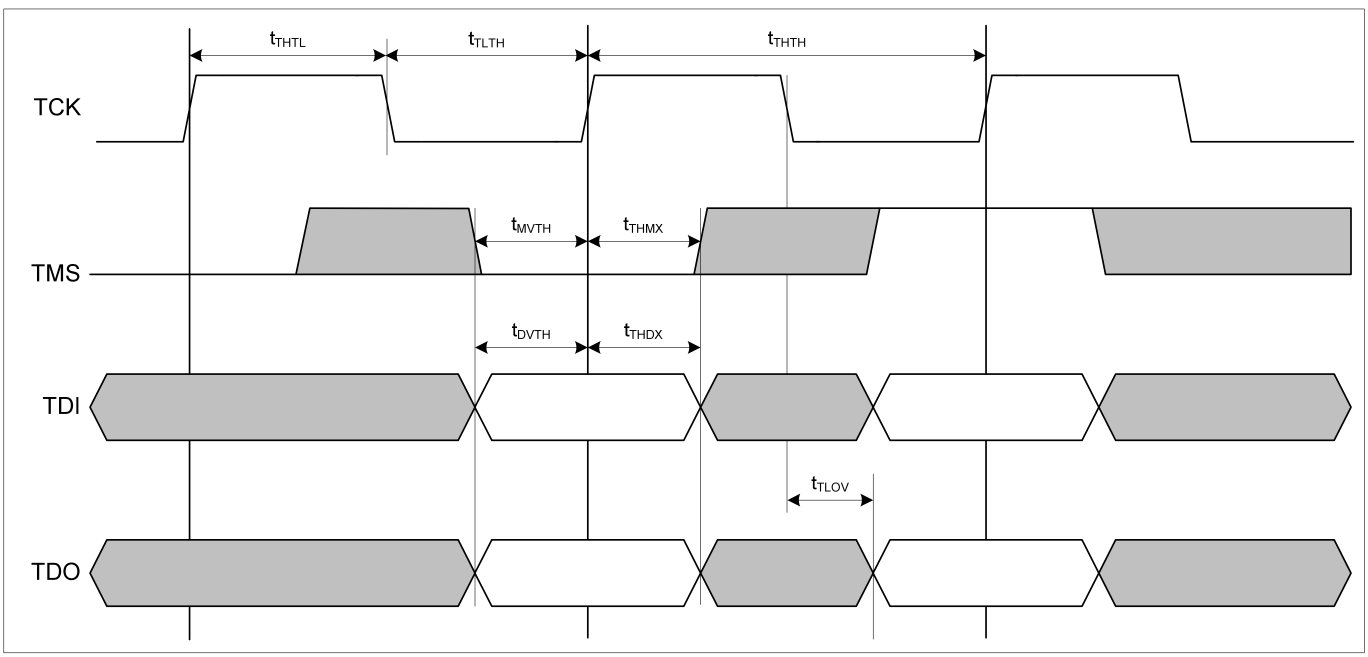
JTAG AC Characteristics

(Over the Operating Temperature Range, V_{DD}=1.8V±5%, V_{DDQ}=1.5V/1.8V)

Parameter	Symbol	Min	Max	Units
TCK cycle time	t_{THTH}	50	–	ns
TCK high pulse width	t_{THTL}	20	–	ns
TCK low pulse width	t_{TLTH}	20	–	ns
TMS Setup	t_{MVTH}	5	–	ns
TMS Hold	t_{THMX}	5	–	ns
TDI Setup	t_{DVTH}	5	–	ns
TDI Hold	t_{THDX}	5	–	ns
TCK Low to Valid Data*	t_{TLOV}	–	10	ns

Note: See *AC Test Loading(c)*

JTAG Timing Diagram



Instruction Set

Code	Instruction	TDO Output	Notes
000	EXTEST	Boundary Scan Register	2, 6
001	IDCODE	32-bit Identification Register	
010	SAMPLE-Z	Boundary Scan Register	1, 2
011	PRIVATE	Do Not Use	5
100	SAMPLE(/PRELOAD)	Boundary Scan Register	4
101	PRIVATE	Do Not Use	5
110	PRIVATE	Do Not Use	5
111	BYPASS	Bypass Register	3

Notes:
1. Places Qs in high-Z in order to sample all input data, regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. BYPASS register is initiated to V_{SS} when BYPASS instruction is invoked. The BYPASS register also holds the last serially loaded TDI when exiting the shift-DR state.
4. SAMPLE instruction does not place Qs in high-Z.
5. This instruction is reserved. Invoking this instruction will cause improper SRAM functionality.
6. This EXTEST is not IEEE 1149.1-compliant. By default, it places Q in high-Z. If the internal register on the scan chain is set high, Q will be updated with information loaded via a previous SAMPLE instruction. The actual transfer occurs during the update IR state after EXTEST is loaded. The value of the internal register can be changed during SAMPLE and EXTEST only.

ID Register Definition

Revision Number (32:29)	Part Configuration (28:12)	JEDEC Code (11:1)	Start Bit (0)
000	00DEF0WX01PQLB0S0	00011010101	1

Part Configuration Definition:
1. DEF = 011 for 72Mb
2. WX = 11 for x36, 10 for x18
3. P = 1 for II+(QUAD-P/DDR-IIP), 0 for II(QUAD/DDR-II)
4. Q = 1 for QUAD, 0 for DDR-II
5. L = 1 for RL=2.5, 0 for RL≠2.5
6. B = 1 for burst of 4, 0 for burst of 2
7. S = 1 for Separate I/O, 0 for Common I/O

LIST OF IEEE 1149.1 STANDARD VIOLATIONS
- 7.2.1.b, e
- 7.7.1.a-f
- 10.1.1.b, e
- 10.7.1.a-d
- 6.1.1.d

Boundary Scan Exit Order

ORDER	Pin ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

ORDER	Pin ID
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	10A
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	2A
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

ORDER	Pin ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1H
85	1J
86	2J
87	3K
88	3J
89	2K
90	1K
91	2L
92	3L
93	1M
94	1L
95	3N
96	3M
97	1N
98	2M
99	3P
100	2N
101	2P
102	1P
103	3R
104	4R
105	4P
106	5P
107	5N
108	5R
109	Internal

Notes:
1. NC pins as defined on the *FBGA Ball Assignments* are read as "Don't Cares".
2. State of internal pin (#109) is loaded via JTAG

Ordering Information

Commercial Range: 0°C to +70°C

Speed	Order Part No.	Organization	Package
333 MHz	IS61QDB22M36A-333M3	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-333M3L	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-333M3	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-333M3L	4Mx18	166 FBGA (15x17 mm), lead free
300 MHz	IS61QDB22M36A-300M3	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-300M3L	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-300M3	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-300M3L	4Mx18	165 FBGA (15x17 mm), lead free
250 MHz	IS61QDB22M36A-250M3	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-250M3L	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-250M3	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-250M3L	4Mx18	165 FBGA (15x17 mm), lead free

Commercial Range: 0°C to +70°C

Speed	Order Part No.	Organization	Package
333 MHz	IS61QDB22M36A-333B3	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-333B3L	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-333B3	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-333B3L	4Mx18	166 FBGA (13x15 mm), lead free
300 MHz	IS61QDB22M36A-300B3	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-300B3L	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-300B3	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-300B3L	4Mx18	165 FBGA (13x15 mm), lead free
250 MHz	IS61QDB22M36A-250B3	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-250B3L	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-250B3	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-250B3L	4Mx18	165 FBGA (13x15 mm), lead free

Note: Please contact SRAM Marketing at SRAM@issi.com for availability of 13x15mm BGA package option.

Industrial Range: -40°C to +85°C

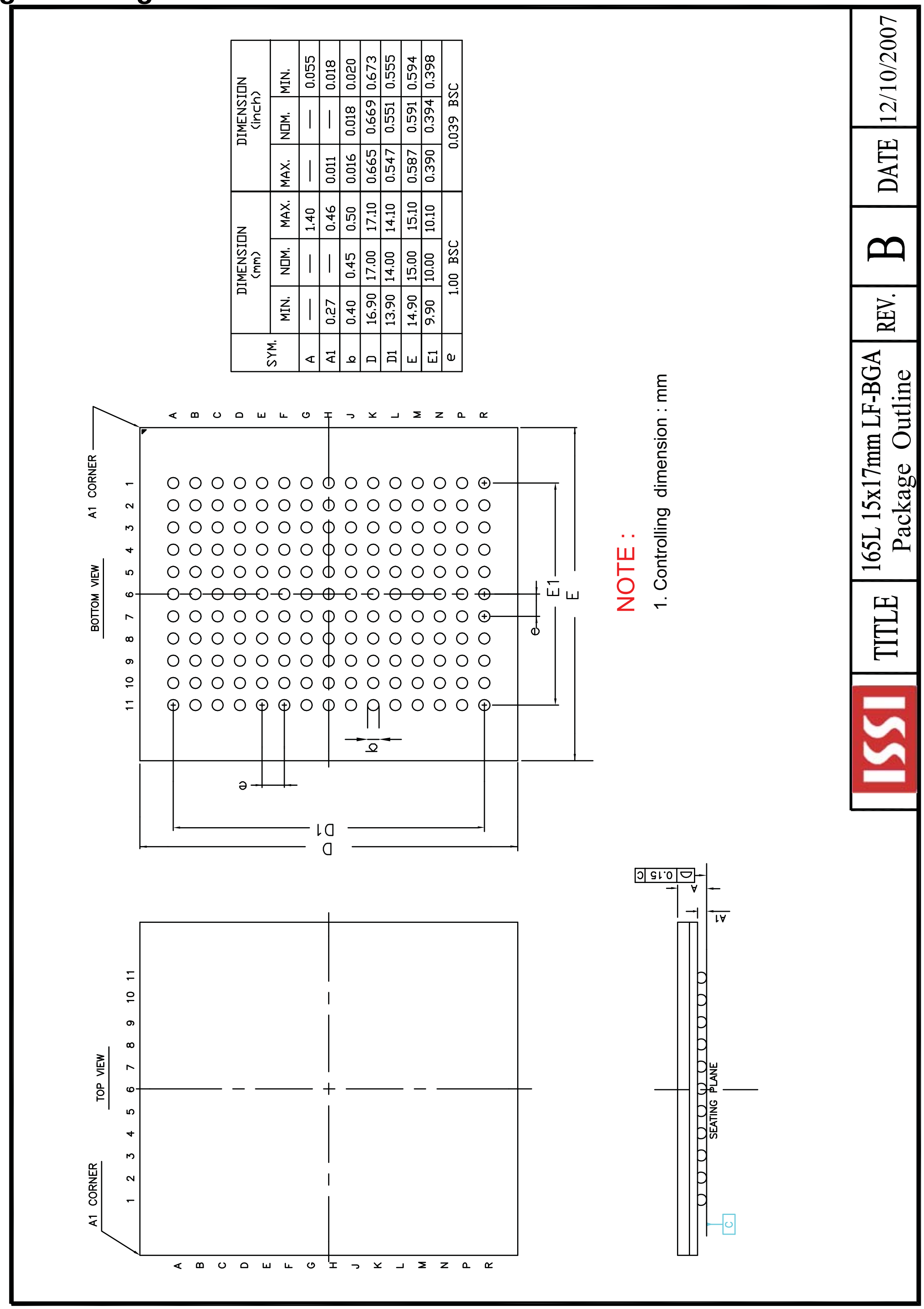
Speed	Order Part No.	Organization	Package
333 MHz	IS61QDB22M36A-333M3I	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-333M3LI	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-333M3I	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-333M3LI	4Mx18	165 FBGA (15x17 mm), lead free
300 MHz	IS61QDB22M36A-300M3I	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-300M3LI	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-300M3I	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-300M3LI	4Mx18	165 FBGA (15x17 mm), lead free
250 MHz	IS61QDB22M36A-250M3I	2Mx36	165 FBGA (15x17 mm)
	IS61QDB22M36A-250M3LI	2Mx36	165 FBGA (15x17 mm), lead free
	IS61QDB24M18A-250M3I	4Mx18	165 FBGA (15x17 mm)
	IS61QDB24M18A-250M3LI	4Mx18	165 FBGA (15x17 mm), lead free

Industrial Range: -40°C to +85°C

Speed	Order Part No.	Organization	Package
333 MHz	IS61QDB22M36A-333B3I	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-333B3LI	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-333B3I	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-333B3LI	4Mx18	165 FBGA (13x15 mm), lead free
300 MHz	IS61QDB22M36A-300B3I	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-300B3LI	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-300B3I	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-300B3LI	4Mx18	165 FBGA (13x15 mm), lead free
250 MHz	IS61QDB22M36A-250B3I	2Mx36	165 FBGA (13x15 mm)
	IS61QDB22M36A-250B3LI	2Mx36	165 FBGA (13x15 mm), lead free
	IS61QDB24M18A-250B3I	4Mx18	165 FBGA (13x15 mm)
	IS61QDB24M18A-250B3LI	4Mx18	165 FBGA (13x15 mm), lead free

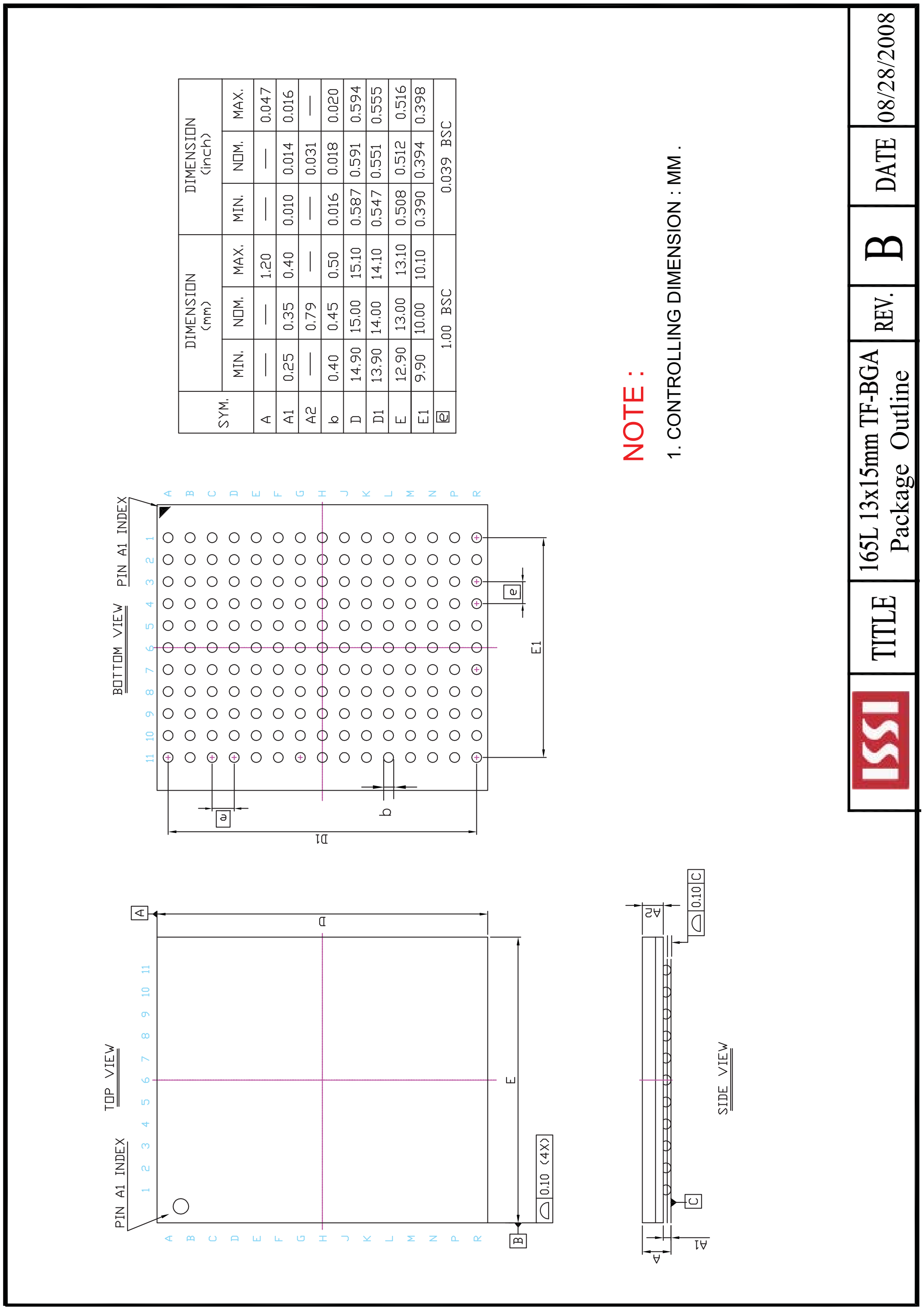
Note: Please contact SRAM Marketing at SRAM@issi.com for availability of 13x15mm BGA package option.

Package drawing – 15x17x1.4 BGA



SYM.	DIMENSION (mm) MIN.	NOM.	MAX.	DIMENSION (inch) MAX.	NOM.	MIN.
A	—	—	1.40	—	—	0.055
A1	0.27	—	0.46	0.011	—	0.018
b	0.40	0.45	0.50	0.016	0.018	0.020
D	16.90	17.00	17.10	0.665	0.669	0.673
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	14.90	15.00	15.10	0.587	0.591	0.594
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

Package drawing – 13x15x1.2 BGA



SYM.	DIMENSION (mm) MIN.	NOM.	MAX.	DIMENSION (inch) MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.35	0.40	0.010	0.014	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
e	1.00 BSC			0.039 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .

TITLE: 165L 13x15mm TF-BGA Package Outline

REV. B

DATE 08/28/2008