ASSP
Dual Serial Input
PLL Frequency Synthesizer

MB15U30SP

➢ DESCRIPTION

The Fujitsu MB15U30SP is a serial input Phase Locked Loop (PLL) frequency synthesizer with 2.5GHz and 510MHz prescalers. A 32/33 or a 64/65 for the 2.5GHz prescaler, and a 8/9 or a 16/17 for the 510MHz prescaler can be selected that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 5.0mA typ. at a supply voltage of 3.0V. A refined charge pump supplies well-balanced output current with 1.0mA and 4mA selected by serial data.

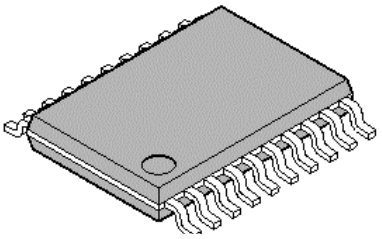
MB15U30SP is ideally suitable for digital mobile communications, such as CATV, PHS(Personal Handy Phone System), and PCS(Personal Communication Service).

➢ FEATURE

-High frequency operation : RF synthesizer: 2.5GHz max.
IF synthesizer: 510MHz max.
-Power supply voltage : Vcc=2.7V to 5.5V
-Very low power supply current : Icc=5.0mA typ. (Vcc=3.0V)
-Power saving function : Ips1=Ips2=10uA max.
-Serial input 15 bit programmable reference divider : R=3 to 32,767
-Serial input 18 bit programmable divider consisting of
Binary 7 bit swallow counter : 0 to 127
Binary 11 bit programmable counter : 3 to 2,047
-On-chip high performance charge pump circuit and phase comparator achieved high speed settling time and low phase noise.
-Wide operating temperature : Ta = -40 to +85°C
-Plastic 20-pin TSSOP package[FPT-20P-M06] / Plastic 20-pad BCC package[LCC-20P-M05]

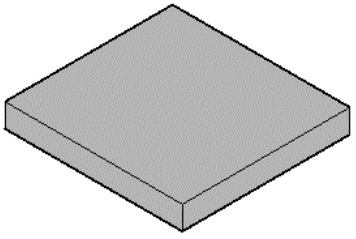
➢ PACKAGE

20-pin Plastic TSSOP



FPT-20P-M06

20-pad Plastic BCC

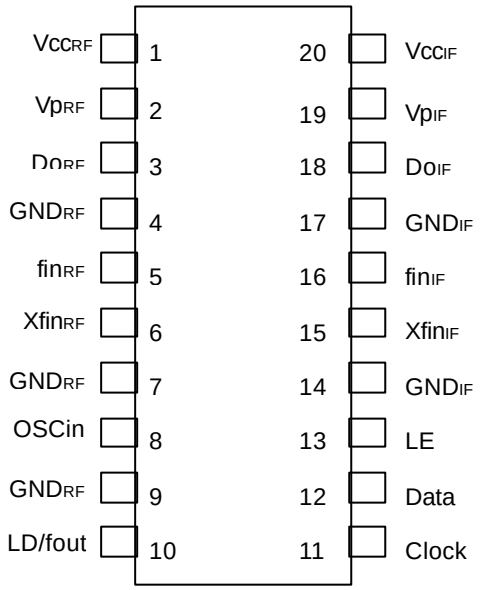


LCC-20P-M05

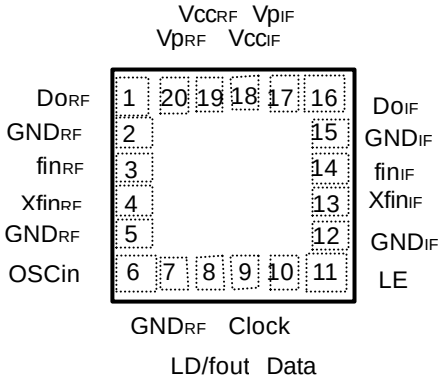
MB15U30SP

➢ PIN ASSIGNMENT

(TSSOP-20)
TOP VIEW



(BCC-20)
TOP VIEW



MB15U30SP

➢ PIN DESCRIPTIONS

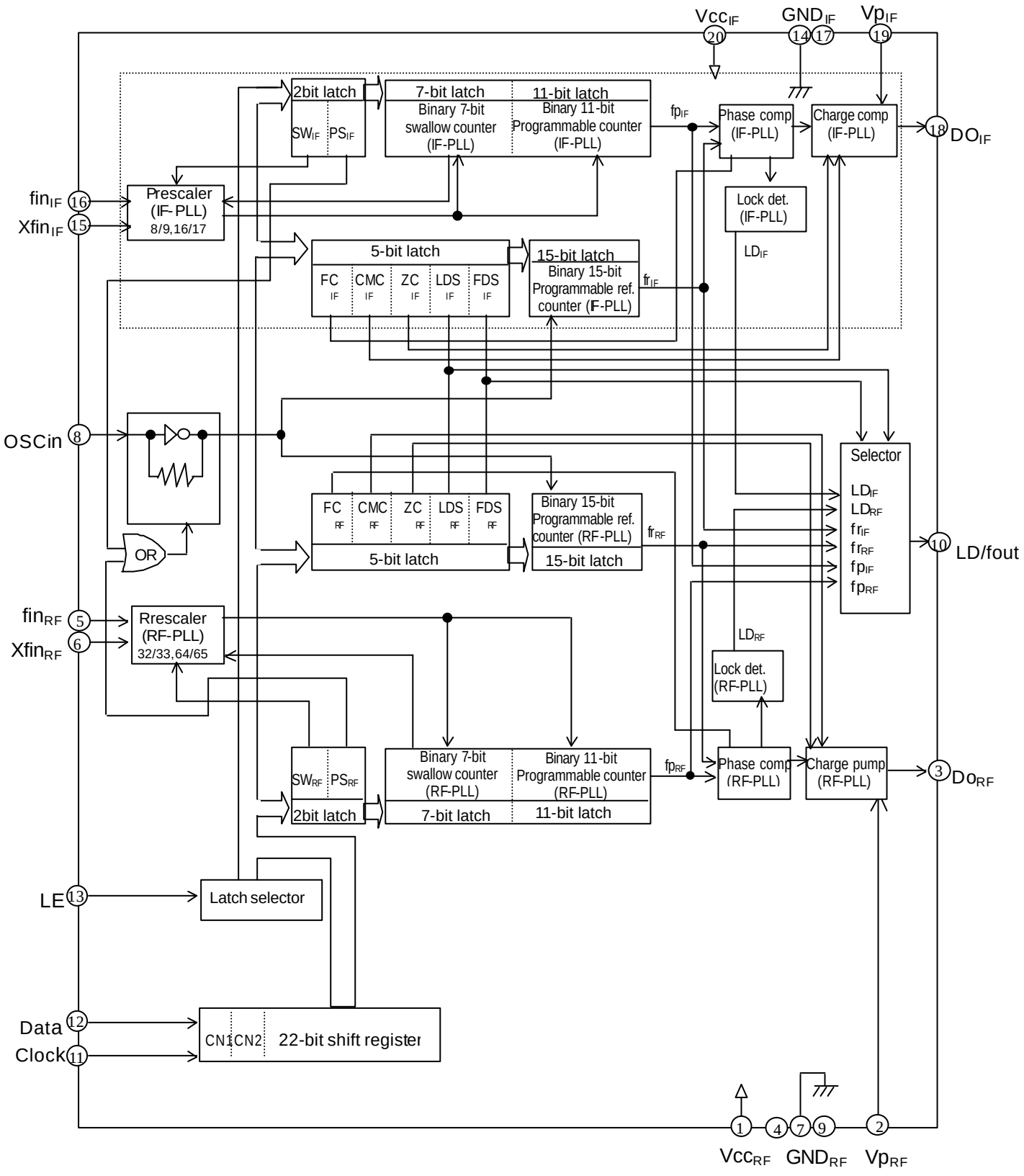
Pin No	Pin name	I/O	Descriptions
1(19)	V_{CCRF}	-	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
2(20)	V_{pRF}	-	Power supply for RF charge pump.(Independent of 19 pin)
3(1)	D_{ORF}	O	Charge pump output for the RF-PLL section. Phase detector characteristics can be reversed using the FC bit.
4(2)	GND_{RF}	-	Ground for the RF-PLL section.
5(3)	fin_{RF}	I	Prescaler input pin for the RF-PLL section. Connection to an external VCO should be via AC coupling.
6(4)	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL. Section. This pin should be grounded via a capacitor.
7(5)	GND_{RF}	-	Ground for the RF-PLL section.
8(6)	OSCin	I	The programmable reference divider input. External TCXO reference oscillator input or connection to crystal. TCXO should be connected with via AC coupling.
9(7)	GND_{RF}	-	Ground for the RF-PLL section.
10(8)	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout). The output signal is selected by the LDS and FDS bits in the serial data.
11(9)	Clock	I	Clock input for the 22 bit shift register. One bit data is shifted into the shift register on a rising edge of the clock.
12(10)	Data	I	Serial data input. Data is transferred to the corresponding latch (RF-ref counter, RF-prog counter, IF-ref counter, IF-prog counter according to the control bits setting in the serial programming data.
13(11)	LE	I	Load enable signal input. When LE is "H", data in the shift register is transferred to the corresponding latch according to the control bits in the serial programming data.
14(12)	GND_{IF}	-	Ground for the IF-PLL section.
15(13)	$Xfin_{IF}$	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
16(14)	fin_{IF}	I	Prescaler input pin for the IF-PLL section. Connection to an external VCO should be via AC coupling.
17(15)	GND_{IF}	-	Ground for the IF-PLL section.
18(16)	D_{OIF}	O	Charge pump output for the IF-PLL section. Phase detector characteristics can be reserved using FC bit.
19(17)	V_{pIF}	-	Power supply voltage for the IF charge pump.(Independent of 2 pin)
20(18)	V_{CCIF}	-	Power supply voltage input pin for the IF-PLL section. When power is OFF, latched data of IF-PLL is cancelled.

(Pin No):BCC20

MB15U30SP

➢ BLOCK DIAGRAM

PKG:TSSOP-20(FPT-20-M06)



➢ ABSOLUTE MAXIMUM

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	Vcc	-0.5 to 6.0	V	
	Vp	-0.5 to 6.0	V	
Input voltage	Vi	-0.5 to 6.0	V	
Output voltage	Vo	-0.5 to 6.0	V	
Storage temperature	T_{STG}	-55 to +125	°C	

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

➢ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	Vcc	2.7	3.0	5.5	V	Vcc_{RF}=Vcc_{IF}
	Vp	Vcc	-	5.5	V	
Input voltage	Vi	GND	-	Vcc	V	
Operating temperature	Ta	-40	-	+85	°C	

Handling Precautions

-This device should be transported and stored in anti-static containers.

-This is a static-sensitive device ; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.

-Always turn the power supply off before inserting or removing the device from its socket.

-Protect leads with a conductive sheet when handling or transporting PC boards with devices

➢ ELECTRICAL CHARACTERISITCS

Parameter		Symbol	Condition		Value			Unit
Power supply current		Icc_{IF}*1			–	1.7	–	mA
		Icc_{RF}*2			–	3.3	–	mA
Power saving current		Ips_{IF}	Vcc_{RF} current at $PSbit_{RF/IF}$="H"		–	0.1*3	10	uA
		Ips_{RF}	Vcc_{IF} current at $PSbit_{RF/IF}$="H"		–	0.1*3	10	uA
Operating frequency		fin_{IF}*4	IF-PLL		45	–	510	MHz
		fin_{RF}*4	RF-PLL		500	–	2500	MHz
		Fosc	Min. 500mVpp		3	–	40	MHz
Input sensitivity		$Pfin_{IF}$	IF-PLL, 50Ω termination		-10	–	+2	dBm
		$Pfin_{RF}$	RF-PLL, 50Ω termination	2.7V≤VCC≤3.0V	-15	–	+2	dBm
				3.0V<VCC≤5.5V	-10	–	+2	dBm
		Vosc			500	–	Vcc	mVp-p
Input voltage	Data, Clock LE	V_{IH}			Vcc×0.8	–	–	V
		V_{IL}			–	–	Vcc×0.2	V
Input current	Data, Clock LE	I_{IH}*5	V_{IH}=Vcc		-1.0	–	+1.0	uA
		I_{IL}*5	V_{IH}=0V		-1.0	–	+1.0	uA
	OSCin	I_{IH}	V_{IH}=Vcc		0	–	+100	uA
		I_{IL}*5	V_{IH}=0V		-100	–	0	uA
Output voltage	LD/fout	V_{OH}	I_{OH}=-1mA,Vcc=3.0V		Vcc-0.4	–	–	V
		V_{OL}	I_{OL}=1mA,Vcc=3.0V		–	–	0.4	V
	Do_{RF} Do_{IF}	V_{DOH}	I_{DOH}=-0.5mA,Vcc=Vp=3.0V		Vp-0.4	–	–	nA
		V_{DOL}	I_{DOL}=0.5mA,Vcc=Vp=3.0V		–	–	0.4	mA
High impedance cutoff current	Do_{RF} Do_{IF}	I_{OFF}	Vcc=Vp=3.0V 0.5V≤V_{DO}≤Vp-0.5V		–	–	3.0	nA
Output current	LD/fout	I_{OH}*5	Vcc=3.0V		–	–	-1.0	mA
		I_{OL}	Vcc=3.0V		+1.0	–	–	mA

➢ ELECTRICAL CHARACTERISITCS (Continued)

Parameter		Symbol	Condition	Value			Unit
				MIN	TYP	MAX	
Output current	DO_{IF} DO_{RF}	I_{DOH}*5	Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="L", Ta=25°C	–	-1.00	–	mA
		I_{DOL}	Vcc=Vp=3.0V, V_{DOL}=Vp/2 CMCbit="L", Ta=25°C	–	1.00	–	mA
		I_{DOH}*5	Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	-4.00	–	mA
		I_{DOL}	Vcc=Vp=3.0V, V_{DOH}=Vp/2 CMCbit="H", Ta=25°C	–	4.00	–	mA
Cp current change ratio	I_{DOL}/I_{DOH}	I_{DOMT}*6	V_{DO}=Vp/2, Ta=25°C	–	3	–	%
	I_{DO} vs V_{DO}	I_{DOVD}*7	0.5V≤V_{DO}≤Vp-0.5V Ta=25°C	–	10	–	%
	I_{DO} vs Ta	I_{DOTA}*8	V_{DO}=Vp/2 -40°C ≤Ta≤+85°C	–	10	–	%

∗1:Conditions: Vcc_{IF}=3.0V, Ta=25°C, $fvco_{IF}$=233.15MHz, fosc=19.2MHz, P=16 in locking state

∗2:Conditions: Vcc_{RF}=3.0V, Ta=25°C, $fvco_{RF}$=1651.20MHz, fosc=19.2MHz, P=64 in locking state

∗3:Conditions: Vcc=3.0V, Ta=25°C, fosc=19.2MHz(-2dBm)

∗4:AC coupling. The minimum frequency is specified with a connecting coupling capacitor of 1000pF.

∗5:The symbol "-" means direction of current flow.

∗6:Conditions: Vcc=Vp=3.0V, Ta=25°C

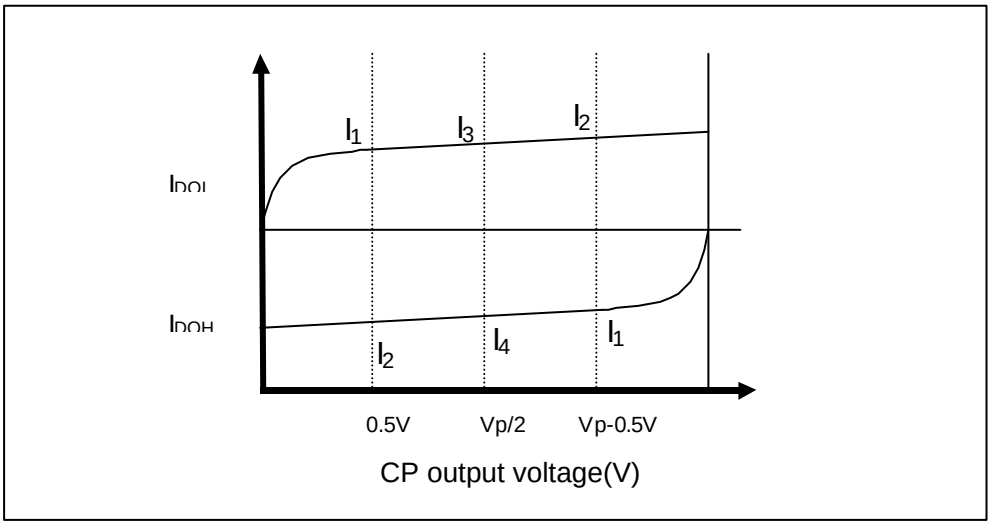
$(| | I_3 | - | I_4 | |)/ [(| I_3 | + | I_4 |)/2] \times 100\%$

∗7:Conditions: Vcc=Vp=3.0V, Ta=25°C

$[(| | I_2 | - | I_1 | |) /2] /[(| I_1 | + | I_2 |)/2] \times 100\%$ (Applied to each I_{DOL}, I_{DOH})

∗8:Conditions: Vcc=Vp=3.0V

$[(| | I_{DO(85°c)} | - | I_{DO(-40°c)} | |) /2] /[(| I_{DO(85°c)} | + | I_{DO(-40°c)} |)/2] \times 100\%$(Applied to each I_{DOL}, I_{DOH})



➢ FUNCTIONAL DESCRIPTION

The divide ratio can be calculated using the following equation:
fvco = [(P × N) + A] × fosc / R (A<N)
fvco : Output frequency of external voltage controlled oscillator (VCO)
P : Preset divide ratio of dual modulus prescaler (8 or 16 for IF-PLL, 32 or 64 for RF-PLL)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter (0≤A≤127)
fosc: Output frequency of the reference frequency oscillator
R : Preset divide ratio of binary 15-bit programmable reference counter (3 to 32,767)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually. Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch them depending upon the control bit data setting.

Table1. control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the IF-PLL
L	H	The programmable reference counter for the RF-PLL
H	L	The programmable counter and the swallow counter for the IF-PLL
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	FC	CMC	ZC	LDS	FDS

CN1,2 :Control bit [Table.1]
R1 to R15 :Divide ratio setting bits for the programmable reference counter(3 to 32,767) [Table.2]
FC :Phase control bit for the phase detector [Table.3]
CMC :Charge pump output current control bit [Table.4]
ZC :Forced high-impedance control bit for the charge pump [Table.5]
LDS/FDS :LD/fout signal select bit [Table.6]
Note: Start data input with MSB first

Programmable Counter

LSB ↓ Data Flow ⟶ MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
CN1	CN2	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	SW	PS

CN1 :Control bit [Table.1]
N1 to N11 :Divide ratio setting bits for the programmable counter(3 to 2,047) [Table.7]
A1 to A7 :Divide ratio setting bits for the swallow counter(0 to 127) [Table.8]
SW :Divide ratio setting bit for the prescaler [Table.9]
(8/9 or 16/17 for IF-PLL, 32/33 or 64/65 for the RF-PLL)
PS :Power saving mode control bit [Table.10,11]
Note: Start data input with MSB first
Note: For the IF swallow counter bits 5,6 and 7 are don't care bits.(See Table.8)

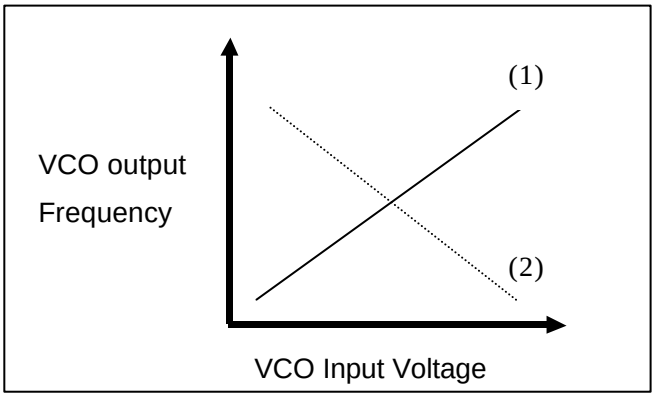
Table.2 Binary 15 bit programmable reference counter data setting

Divide ratio (R)	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less then 3 is prohibited.

Tabale.3 Phase comparator phase switching data setting

	FC="H"	FC="L"
fr > fp	H	L
fr < fp	L	H
fr = fp	Z	Z
VCO polarity	(1)	(2)



NOTE: Z= High impedance

When the LPF and VCO characteristics are similar to (1), set FC bit high

When the VCO characteristics are similar to (2), set FC bit low.

Table.4 Charge pump output current selection

CMC	Charge pump output current
0	1×IDO
1	4×IDO

Table.5 Forced high impedance control for the charge pump

ZC	Charge pump output
0	Normal output
1	High impedance

Table.6 LD/fout output select data setting

LDS_{RF}	LDS_{IF}	FDS_{RF}	FDS_{IF}	LD/fout output signal
0	0	0	0	Disabled
0	1	0	0	LD signal (IF lock detect)
1	0	0	0	LD signal (RF lock detect)
1	1	0	0	LD signal (RF/IF lock detecy)
×	0	0	1	fout (output fr_{IF})
×	0	1	0	fout (output fr_{RF})
×	1	0	1	fout (output fp_{IF})
×	1	1	0	fout (output fp_{RF})
0	0	1	1	Fast lock
0	1	1	1	IF counter reset
1	0	1	1	RF counter reset
1	1	1	1	RF/IF Counter reset

Note : ×=don't care

The Fast lock mode utilizes the LD/fout output pin. While Fast lock mode, whenever RF Charge pump output current select bit(CMC_{RF} bit) is selected "H", LD/fout output pin (open drain output) is "L". When CMC_{RF} bit is selected"L", LD/fout output pin(open drain output) is "Z".(See Fast lock circuit example)

Table.7 Binary 11 bit Programmable counter data setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio less than 3 is prohibited.

Table.8 Binary 7 bit swallow counter data setting

RF

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Note: Divide ratio (A) range=0 to 127

IF

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	x	x	x	0	0	0	0
1	x	x	x	0	0	0	1
•	•	•	•	•	•	•	•
15	x	x	x	1	1	1	1

Note: x=don't care

Table.9 Prescaler data setting

		SW="L"	SW="H"
Prescaler divide ratio	IF-PLL	8/9	16/17
	RF-PLL	32/33	64/65

Table.10 Power saving mode setting(1)

PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
H	H	OFF	OFF	OFF
L	H	ON	OFF	ON
H	L	OFF	ON	ON
L	L	ON	ON	ON

Setting a $PS_{IF/RF}$ bit to high, IF-PLL/RF-PLL enters into power saving mode resultant current consumption can be limited to 10uA max.. Setting PS bit to low, power saving mode is released so that the device works normally. Allow 1us after frequency stabilization on power-up for exiting the power saving mode.(PS: "H" to "L)
Serial data can be entered during the power saving mode.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10uA per one PLL section.
At that time, the DO become the same state as when a loop is locking. That is, the DO becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a time constant of LPF. As a result, VCO's frequency is kept at the locking frequency.

Table.11 POWER SAVING MODE Setting(2)

ZC	PS	Status
H	H	Asynchronous power saving mode
L	H	Synchronous power saving mode
H	L	Charge pump high impedance only
L	L	Normal operation

Asynchronous power saving mode

The PLL can be asynchronously powered down either by setting the PS bit to HIGH.
The power saving function is NOT gated by the charge pump. Once the PS bit are loaded, the part will go into power saving mode immediately.

Synchronous power saving mode

The PLL can be synchronously powered down by setting PS bit to HIGH.
The power saving function is gated by the charge pump. Once the PS bit are loaded the part will go into power saving mode upon the charge pump becomes tri-state.

Serial data input timing

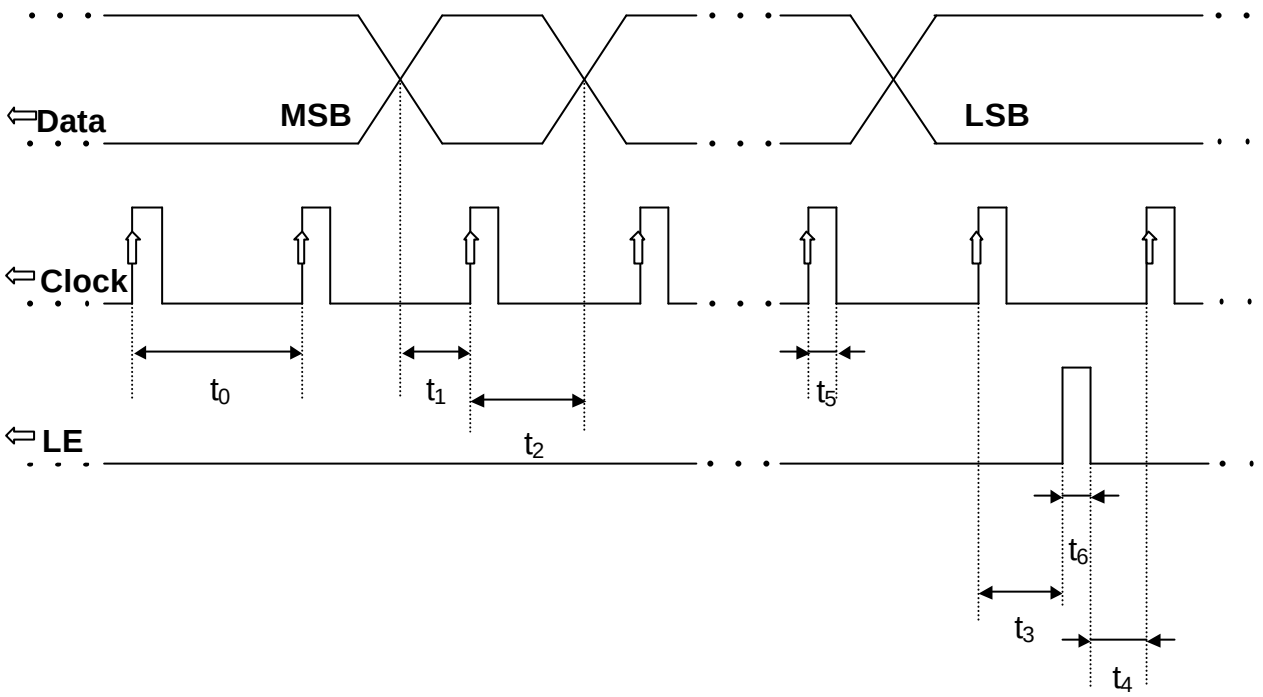
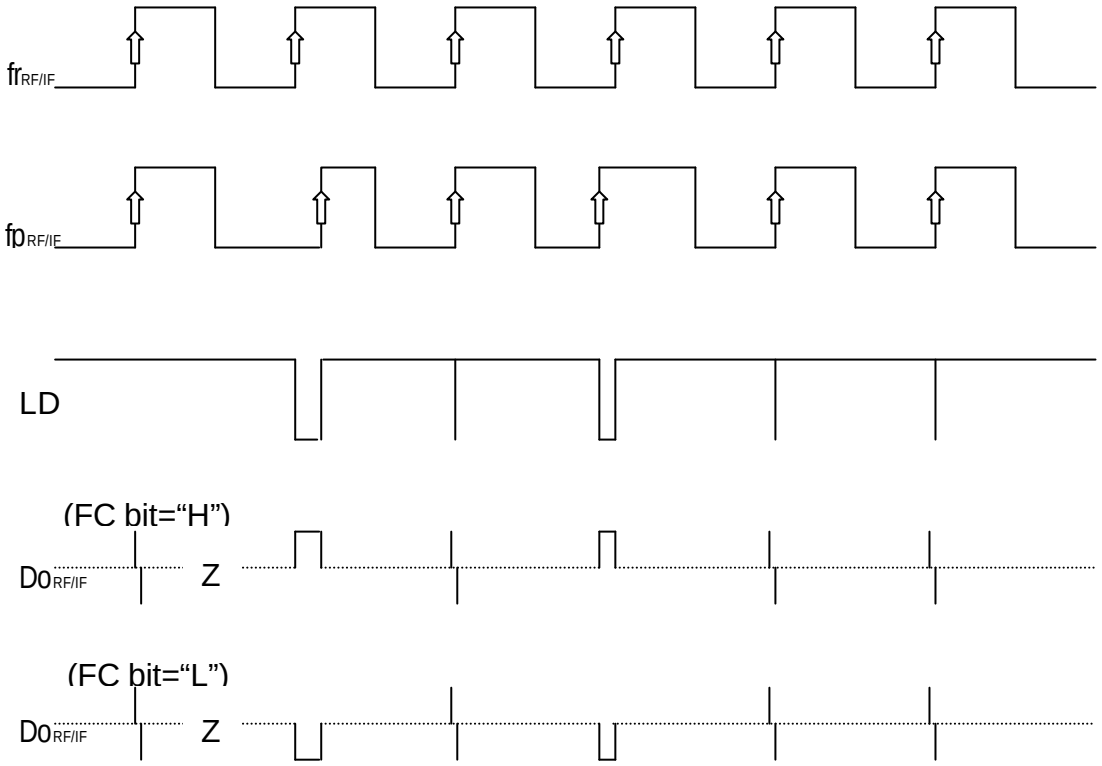


Table11.Timing parameters

Parameter	MIN.	TYP.	MAX.	Unit	Note
t0	100	–	–	ns	CK Rate
t1	20	–	–	ns	tsu CK→Data
t2	20	–	–	ns	th CK→ Data
t3	30	–	–	ns	tsu LE
t4	20	–	–	ns	tsu inactive
t5	30	–	–	ns	tw CK
t6	100	–	–	ns	tw LE

On rising edge of the clock, one bit of the data is transferred into the shift register.

➢ Phase detector output waveform

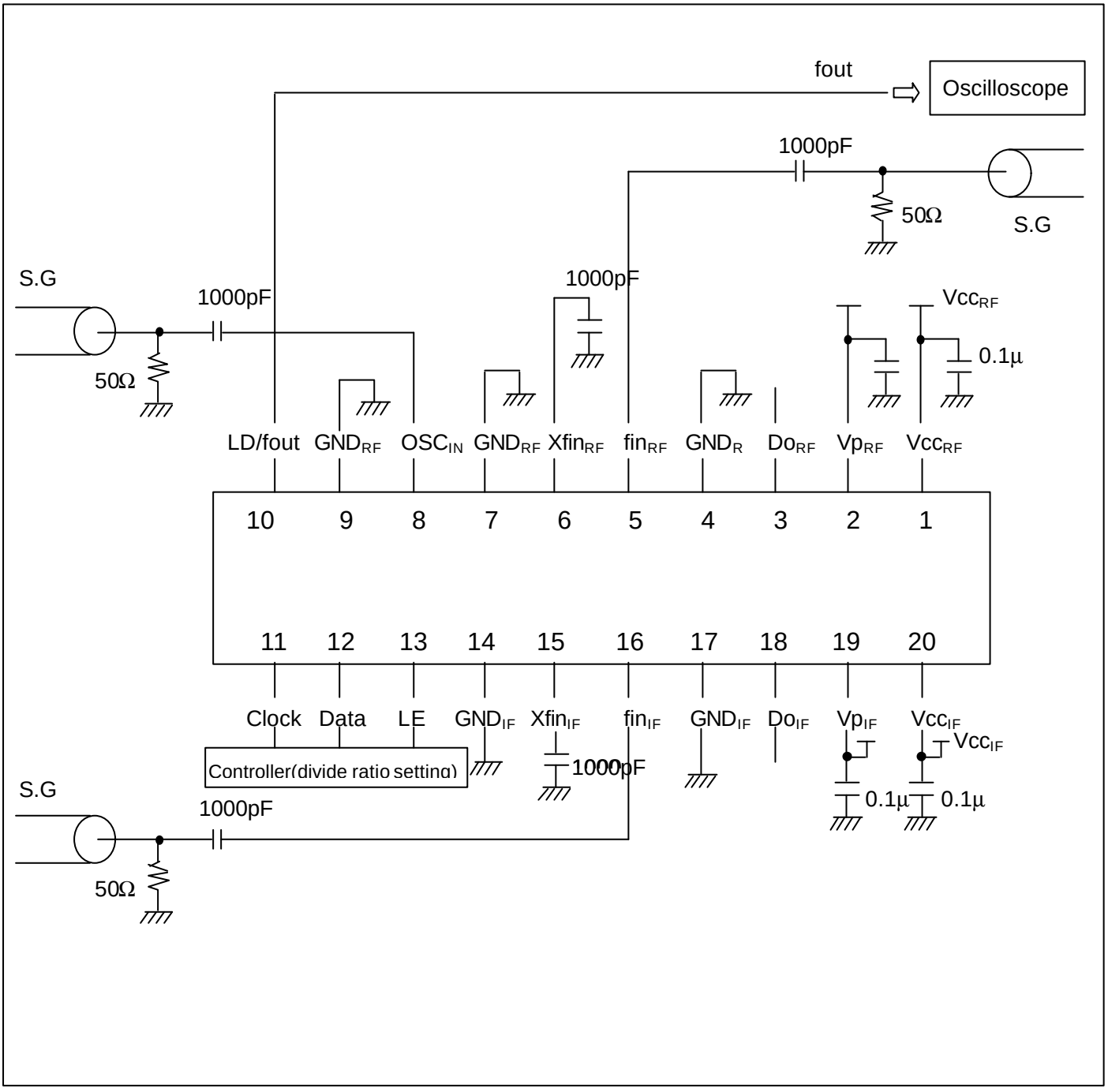


Note: Phase error detection range = -2π to +2π

Pulse on $Do_{RF/IF}$ signals are output to prevent dead zone.

MB15U30SP

➢ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)

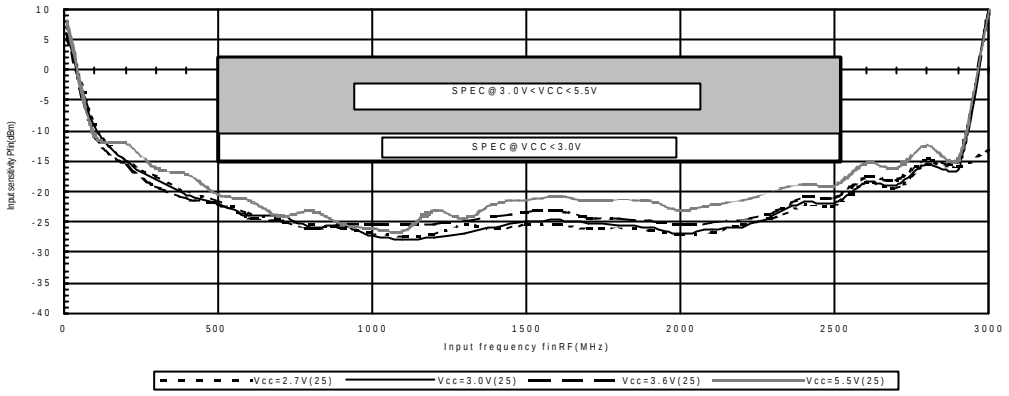


MB15U30SP

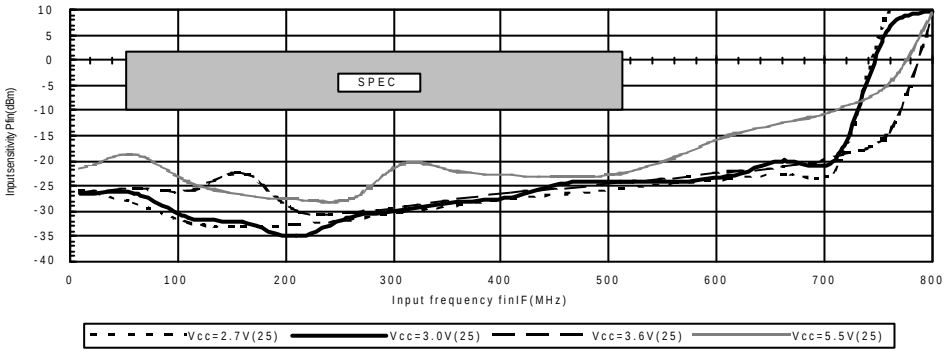
➢ TYPICAL CHARACTERISTICS

1.fin input sensitivity

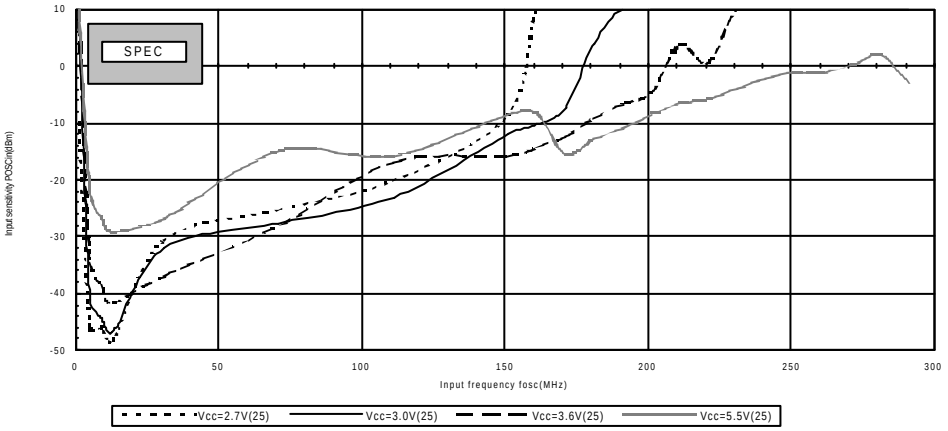
Input sensitivity of fin (RF) versus Input frequency



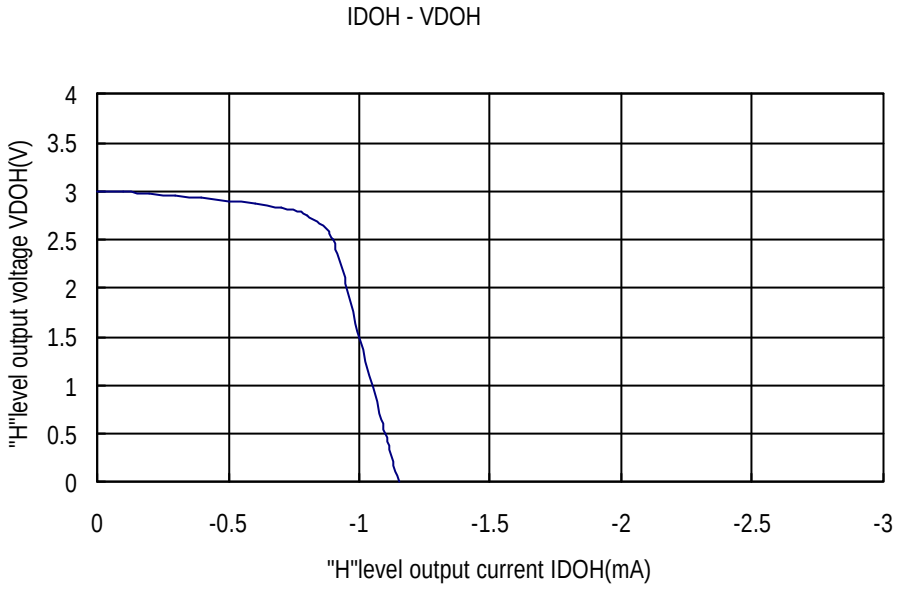
Input sensitivity of fin (IF) versus Input frequency

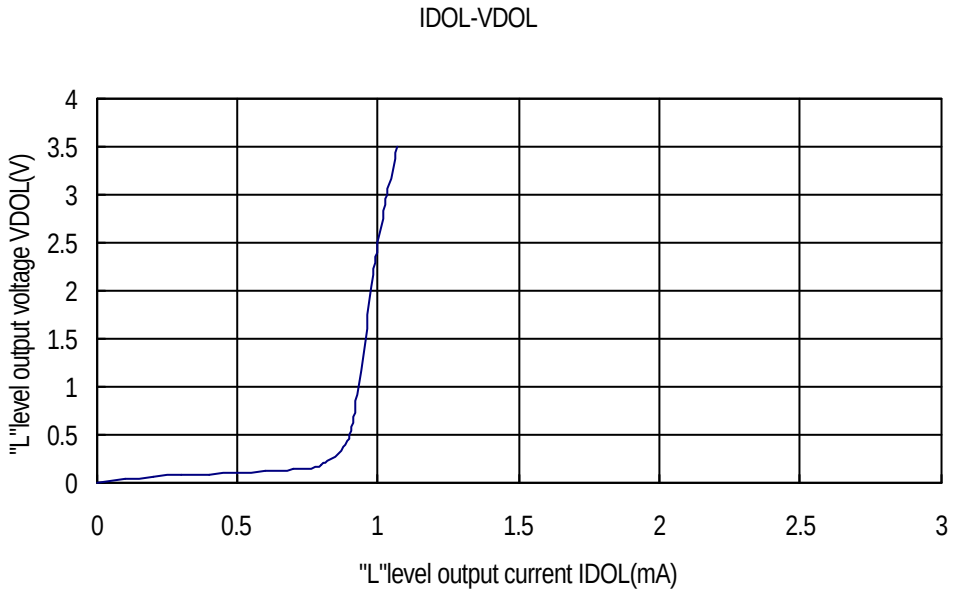


2.OSCin Input se nsitivity

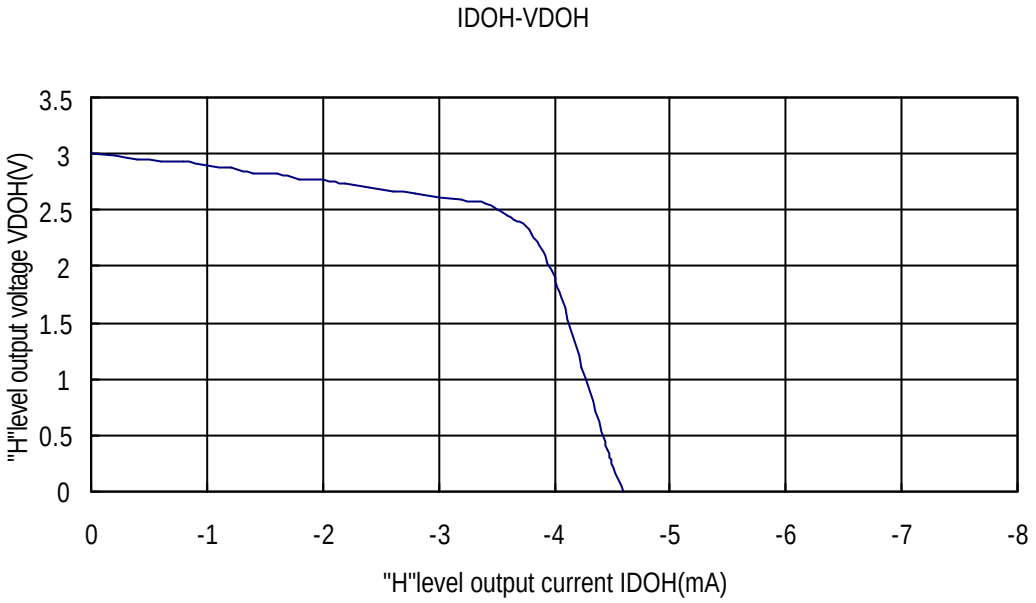


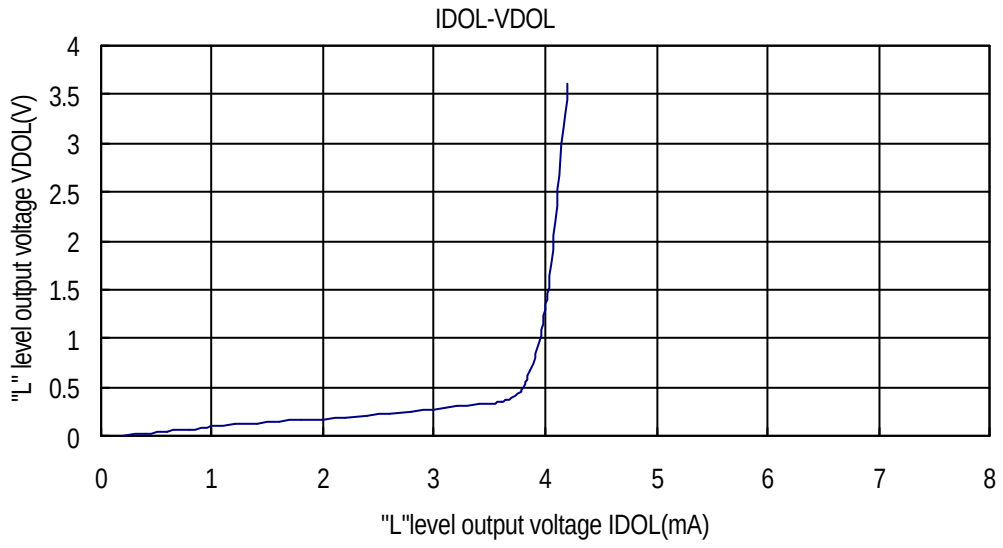
3.Do output current (1´ Do mode)





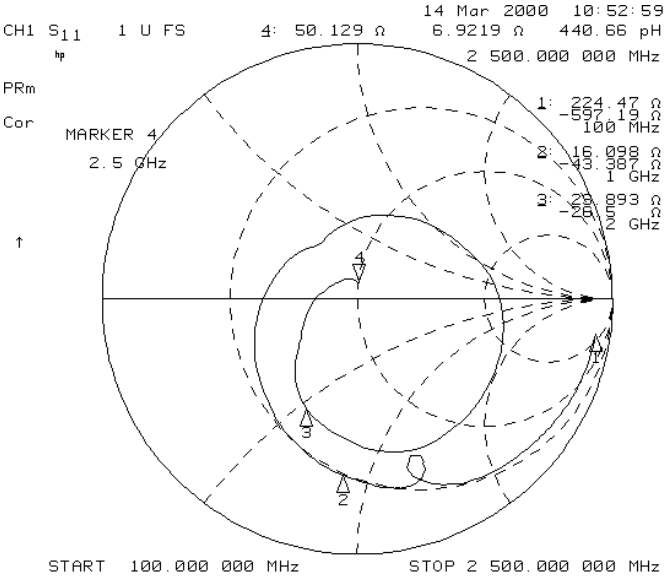
4.Do output current (4xDo mode)



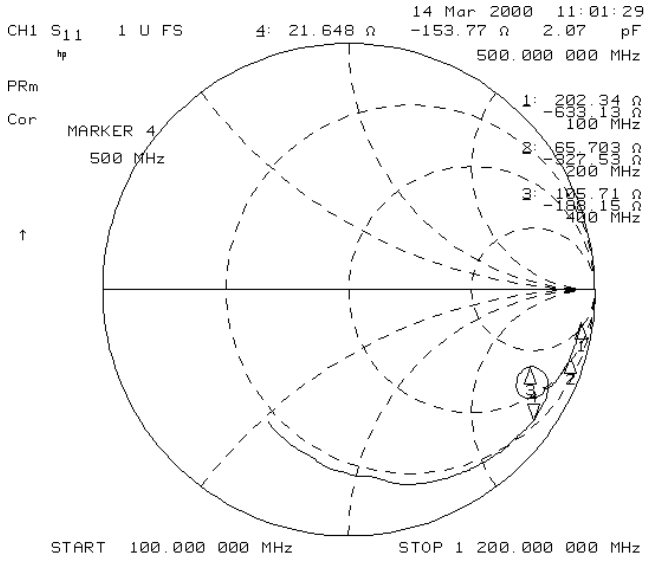


5.Input impedance

Input impedance of fin (RF)

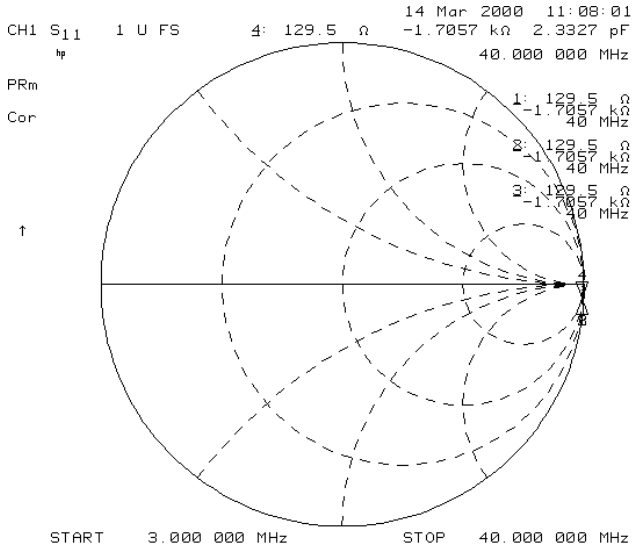


Input impedance of fin (IF)

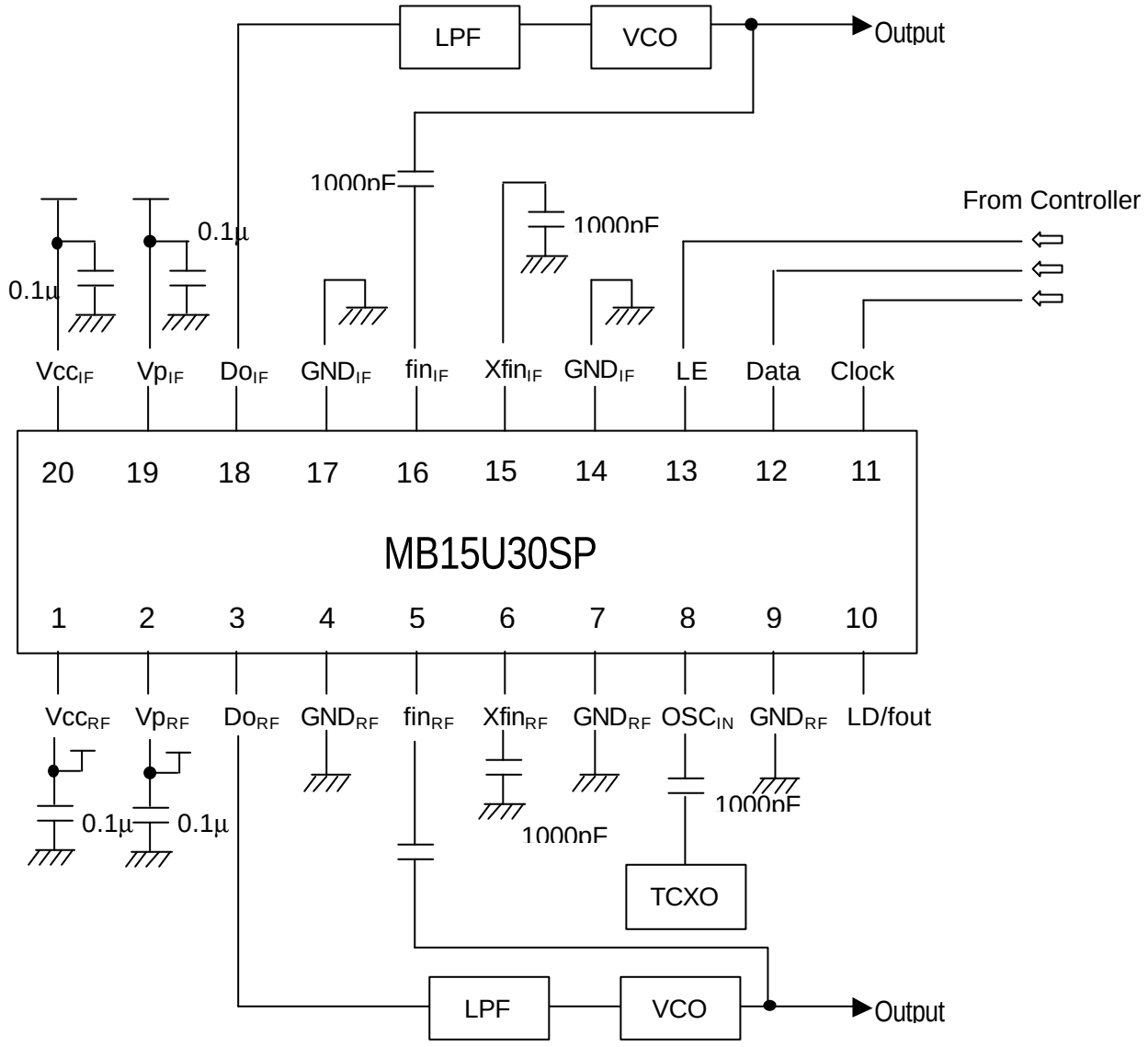


5.Input impedance

Input impedance of fin (OSCin)

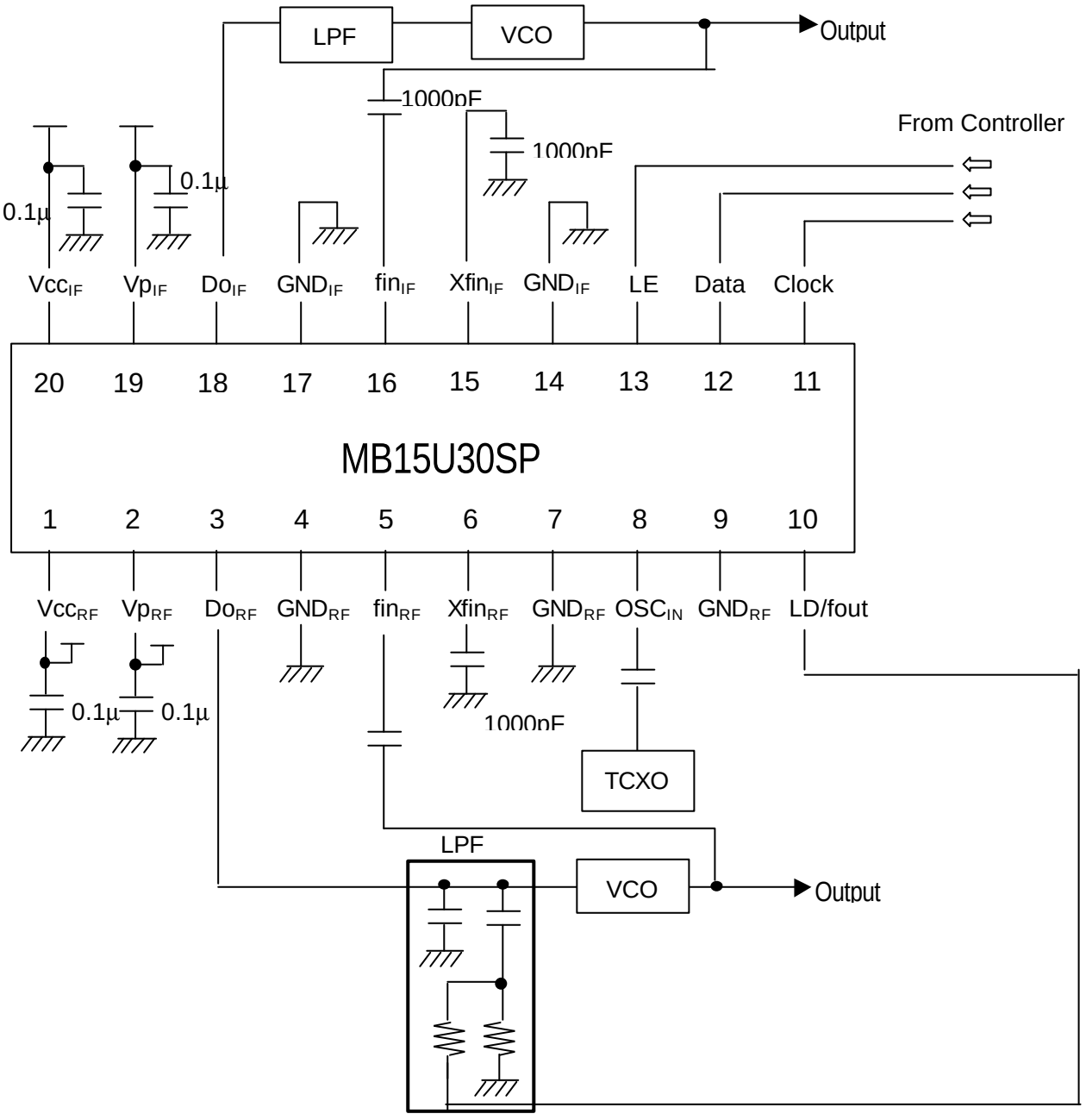


➢ APPLICATION EXAMPLE



Clock, Data, LE : Insert a pull-down or pull-up resister as needed to prevent oscillation when the terminals are left open.

➢ APPLICATION EXAMPLE : Fast lock mode



Clock, Data, LE : Insert a pull-down or pull-up resister as needed to prevent oscillation when the terminals are left open.

The Fastlock mode is controlled by the LDS/FDS bits and the CMC_{RF} bit. When the CMC_{RF} bit is set to "H" (the RF charge pump current is increased 4x normal mode), the LD/fout pin (open drain output) is "L", enabling the parallel resistor in the loop filter. This effectively increases the LPF bandwidth, allowing the loop to lock faster. After the loop has locked onto a new frequency, the CMC_{RF} bit is set to "L", forcing the LD/fout output pin into a high impedance state and returning the LPF bandwidth back to its original value.

➢ ORDERING INFORMATION

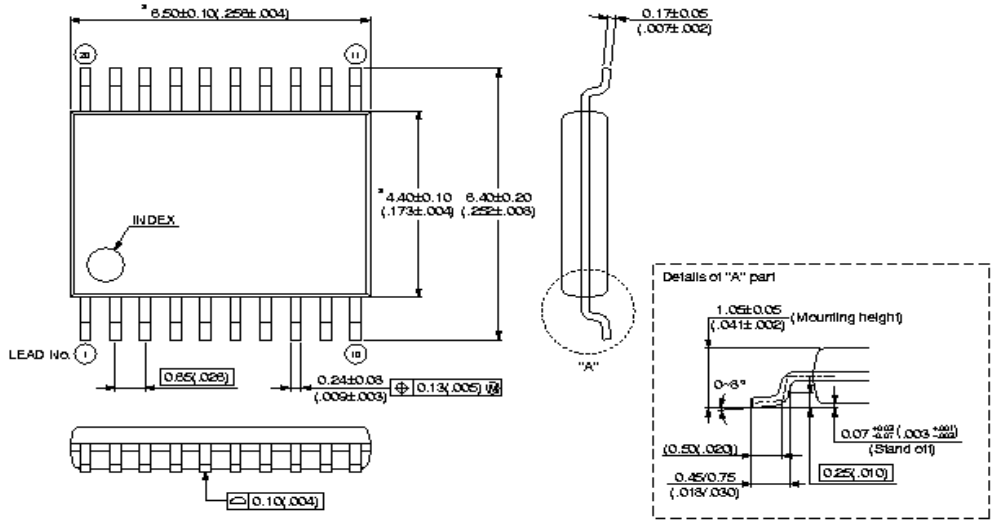
Part number	Package	Remarks
MB15U30SPPFV	20-pin Plastic TSSOP (FPT-20P-M06)	-
MB15U30SPPVA	20-pad Plastic BCC (LCC-20P-M05)	-

MB15U30SP

➢ PACKAGE DIMENSION

20pins, Plastic TSSOP

(FPT-20P-M06)



20pins, Plastic BCC

(LCC-20P-M05)