

# CD74FCT16652T, CD74FCT162652T

August 1996

## Fast CMOS 16-Bit Registered Transceivers

### Features

- These Devices are High-speed, Low Power Devices with High Current Drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on All Inputs
- CD74FCT16652T
  - High Output Drive:  $I_{OH} = -32mA$ ;  $I_{OL} = 64mA$
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical  $V_{OLP}$  (Output Ground Bounce)  $< 1.0V$  at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$
- CD74FCT162652T
  - Balanced Output Drivers:  $\pm 24mA$
  - Reduced System Switching Noise
  - Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.6V$  at  $V_{CC} = 5V$ ,  $T_A = 25^\circ C$

### Description

Harris' CD74FCT16652T and CD74FCT162652T are produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

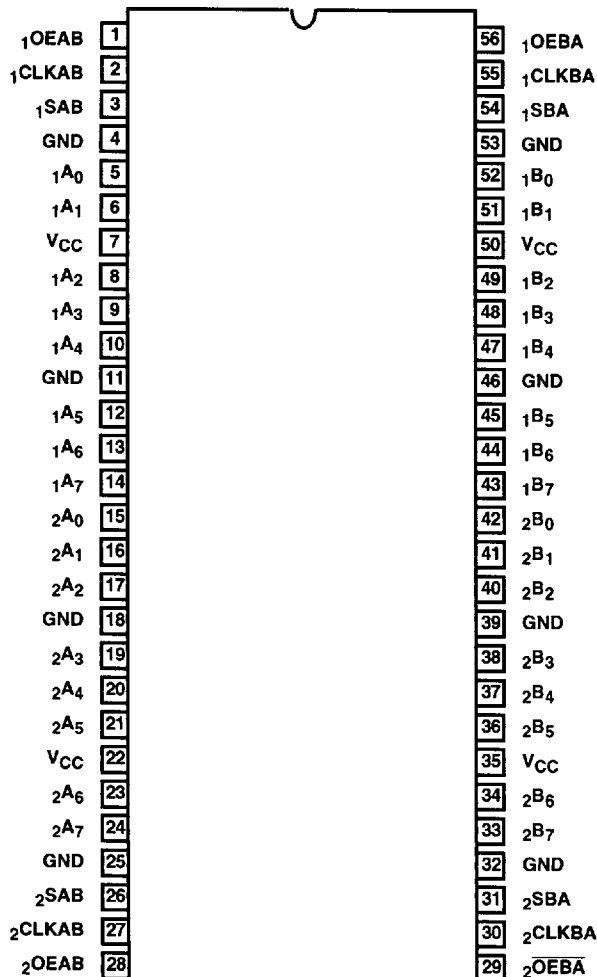
These devices are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ( $\chi OEAB$  and  $\chi OEBA$ ) to control the transceiver functions. The Select ( $\chi SAB$  and  $\chi SBA$ ) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT16652T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162652T has  $\pm 24mA$  balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

### Pinout

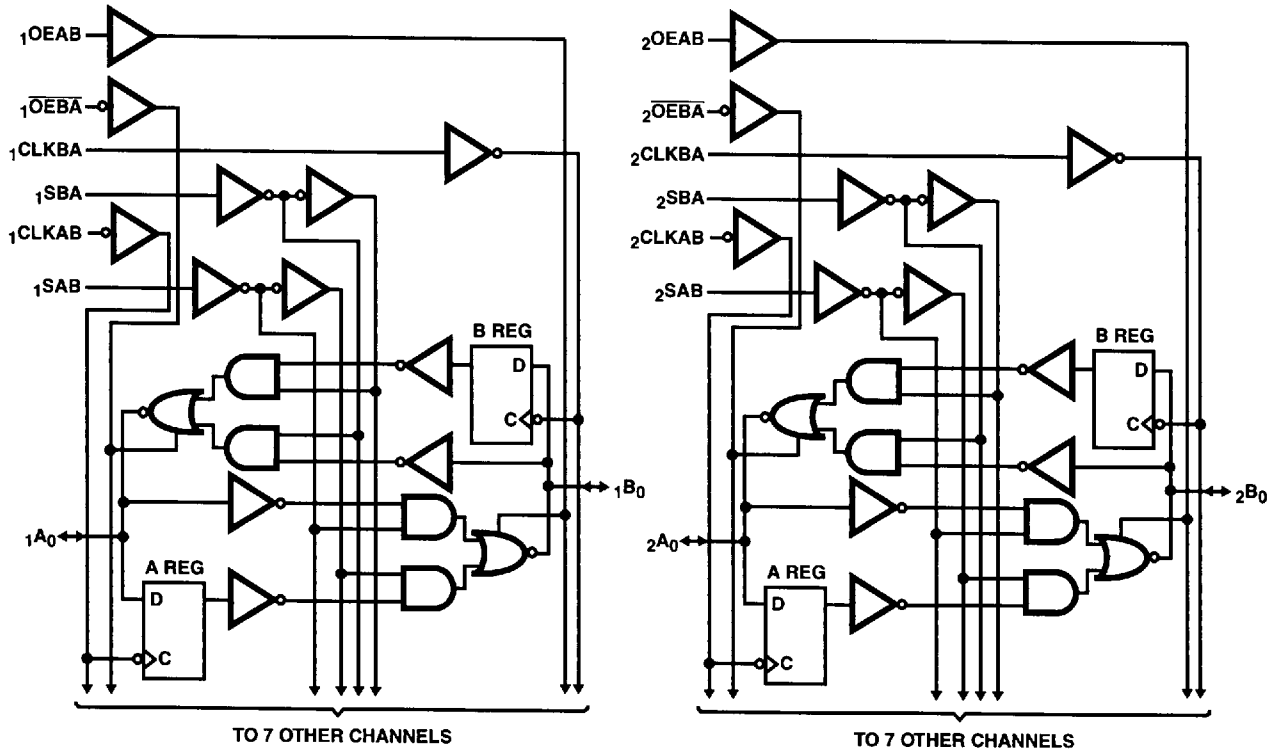
CD74FCT16652T, CD74FCT162652T  
(SSOP, TSSOP)  
TOP VIEW



### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652TSM	-40 to 85	56 Ld SSOP	M56.300-P

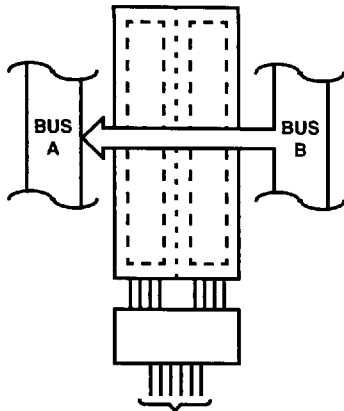
**Functional Block Diagram**



**TRUTH TABLE**

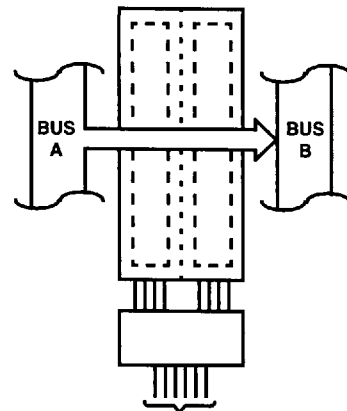
FUNCTION/OPERATION	INPUTS						DATA I/O	
	xOEAB	xOEBA	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X	Input	Input
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 1)
Store A in Both Registers	H	H	↑	↑	X (Note 2)	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 1)	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 2)	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H	Output	Input
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X	Input	Output
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

- The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
- Select control = L: clocks can occur simultaneously.  
 Select control = H: clocks must be staggered in order to load both registers.  
 H = High Voltage Level  
 L = Low Voltage Level  
 X = Don't Care  
 ↑ = LOW-to-HIGH transition



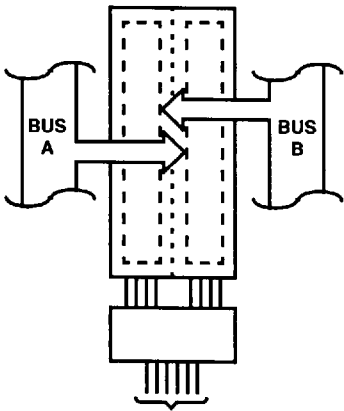
$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 L L X X X L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A

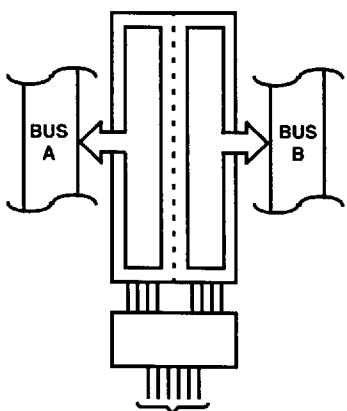


$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 H H X X L X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 X H ↑ X X X  
 L X X ↑ X X  
 L H ↑ ↑ X X  
 FIGURE 3. STORAGE FROM A AND/OR B



$\overline{xOEAB}$   $\overline{xOEBA}$   $xCLKAB$   $xCLKBA$   $xSAB$   $xSBA$   
 H L H or L H or L H H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

**Pin Descriptions**

PIN NAME	DESCRIPTION
$xAx$	Data Register A Inputs Data Register B Outputs
$xBx$	Data Register B Inputs Data Register A Outputs
$xCLKAB, xCLKBA$	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
$\overline{xOEAB}, \overline{xOEBA}$	Output Enable Inputs
GND	Ground
VCC	Power

## CD74FCT16652T, CD74FCT162652T

### Absolute Maximum Ratings

DC Input Voltage .....	-0.5V to 7.0V
DC Output Current .....	120mA

### Operating Conditions

Operating Temperature Range .....	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V <sub>CC</sub> Only .....	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only .....	-0.5V to 7.0V

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
TSSOP Package .....	85
SSOP Package .....	70
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C
(Lead Tips Only)	

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### Electrical Specifications

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 5.0V ±10%							
Input HIGH Voltage	V <sub>IH</sub>	Guaranteed Logic HIGH Level	2.0	-	-	V	
Input LOW Voltage	V <sub>IL</sub>	Guaranteed Logic LOW Level	-	-	0.8	V	
Input HIGH Current	I <sub>IH</sub>	V <sub>CC</sub> = Max      V <sub>IN</sub> = V <sub>CC</sub>	-	-	1	μA	
Input LOW Current	I <sub>IL</sub>	V <sub>CC</sub> = Max      V <sub>IN</sub> = GND	-	-	-1	μA	
High Impedance Output Current	I <sub>OZH</sub>	V <sub>CC</sub> = Max      V <sub>OUT</sub> = 2.7V	-	-	1	μA	
	I <sub>OZL</sub>	V <sub>CC</sub> = Max      V <sub>OUT</sub> = 0.5V	-	-	-1	μA	
Clamp Diode Voltage	V <sub>IK</sub>	V <sub>CC</sub> = Min, I <sub>IN</sub> = -18mA	-	-0.7	-1.2	V	
Short Circuit Current	I <sub>OS</sub>	V <sub>CC</sub> = Max (Note 6), V <sub>OUT</sub> = GND	-80	-140	-200	mA	
Output Drive Current	I <sub>O</sub>	V <sub>CC</sub> = Max (Note 6), V <sub>OUT</sub> = 2.5	-50	-	-180	mA	
Input Hysteresis	V <sub>H</sub>		-	100	-	mV	
<b>CD74FCT16652T OUTPUT DRIVE SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 5.0V ±10%							
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3.0mA	2.5	3.5	-	V
			I <sub>OH</sub> = -15.0mA	2.4	3.5	-	V
			I <sub>OH</sub> = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 64mA	-	0.2	0.55	V
Power Down Disable	I <sub>OFF</sub>	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>OUT</sub> ≤ 4.5V	-	-	±100	μA	
<b>CD74FCT162652T OUTPUT DRIVE SPECIFICATIONS</b> Over the Operating Range, T <sub>A</sub> = -40°C to 85°C, V <sub>CC</sub> = 5.0V ±10%							
Output HIGH Voltage	V <sub>OH</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V <sub>OL</sub>	V <sub>CC</sub> = Min, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 24mA	-	0.3	0.55	V
Output LOW Current	I <sub>ODL</sub>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V (Note 6)	60	115	150	mA	
Output HIGH Current	I <sub>ODH</sub>	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> = 1.5V (Note 6)	-60	-115	-150	mA	

**CD74FCT16652T, CD74FCT162652T**

**Electrical Specifications (Continued)**

PARAMETERS	SYMBOL	(NOTE 4) TEST CONDITIONS	MIN	(NOTE 5) TYP	MAX	UNITS	
<b>CAPACITANCE</b> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$							
Input Capacitance (Note 7)	$C_{IN}$	$V_{IN} = 0\text{V}$	-	4.5	6	pF	
Output Capacitance (Note 7)	$C_{OUT}$	$V_{OUT} = 0\text{V}$	-	5.5	8	pF	
<b>POWER SUPPLY SPECIFICATIONS</b>							
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	500	$\mu\text{A}$	
Supply Current per Input at TTL HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$ $V_{IN} = 3.4\text{V}$ (Note 8)	-	0.5	1.5	mA	
Supply Current per Input per MHz (Note 9)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open $\overline{XOEAB} = \overline{XOEBA} = \text{GND}$ One Bit Toggling 50% Duty Cycle	-	75	120	$\mu\text{A}/\text{MHz}$	
Total Power Supply Current (Note 11)	$I_C$	$V_{CC} = \text{Max}$ , Outputs Open $f_{CP} = 10\text{MHz}$ ( $\overline{XCLKBA}$ ) 50% Duty Cycle $\overline{XOEAB} = \overline{XOEBA} = \text{GND}$ One Bit Toggling $f_I = 5\text{MHz}$ , 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.8	1.7 (Note 10)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	1.3	3.2 (Note 10)	mA
		$V_{CC} = \text{Max}$ , Outputs Open $f_{CP} = 10\text{MHz}$ ( $\overline{XCLKBA}$ ) 50% Duty Cycle $\overline{XOEAB} = \overline{XOEBA} = \text{GND}$ 16 Bits Toggling $f_I = 2.5\text{MHz}$ , 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.8	6.5 (Note 10)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	8.3	22.0 (Note 10)	mA

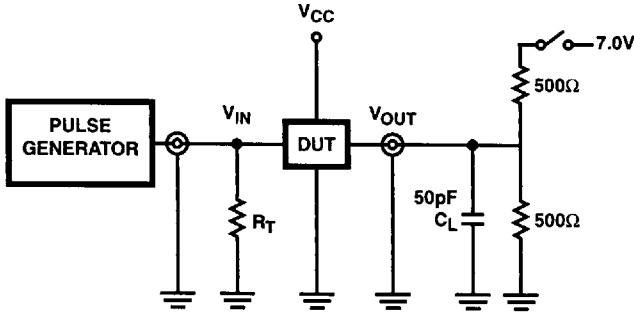
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Propagation Delay Bus to Bus	$t_{PLH}$ , $t_{PHL}$	$C_L = 50pF$ $R_L = 500\Omega$	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	ns
Output Enable Time $\chi OEAB$ or $\chi OE\bar{B}\bar{A}$ to Bus	$t_{PZH}$ , $t_{PZL}$		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	ns
Output Disable Time (Note 14) $\chi OEAB$ or $\chi OE\bar{B}\bar{A}$ to Bus	$t_{PHZ}$ , $t_{PLZ}$		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	ns
Propagation Delay Clock to Bus	$t_{PLH}$ , $t_{PHL}$		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	ns
Propagation Delay $\chi SBA$ or $\chi SAB$ to Bus	$t_{PLH}$ , $t_{PHL}$		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	ns
Setup Time HIGH or LOW, Bus to Clock	$t_{SU}$		4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	$t_H$		2.0	-	1.5	-	1.5	-	1.0	-	ns
Clock Pulse Width HIGH or LOW (Note 14)	$t_W$		6.0	-	5.0	-	5.0	-	3.0	-	ns
Output Skew (Note 15)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
5. Typical values are at  $V_{CC} = 5.0V$ ,  $25^\circ C$  ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
11.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Input Frequency  
 $N_i$  = Number of Inputs at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.
15. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.  
 $R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate  $\leq 1.0\text{MHz}$ ;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_f, t_r \leq 2.5\text{ns}$ .

FIGURE 5. TEST CIRCUIT

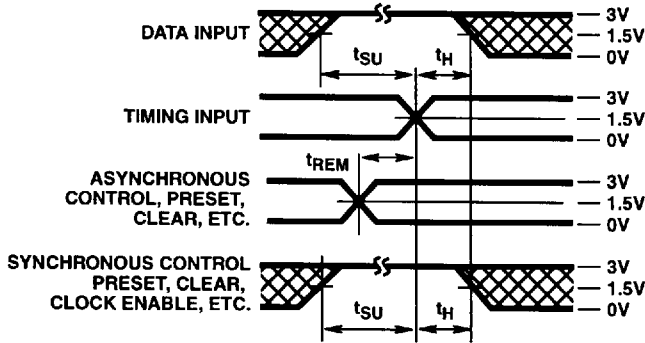


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

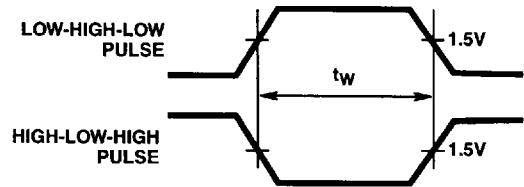


FIGURE 7. PULSE WIDTH

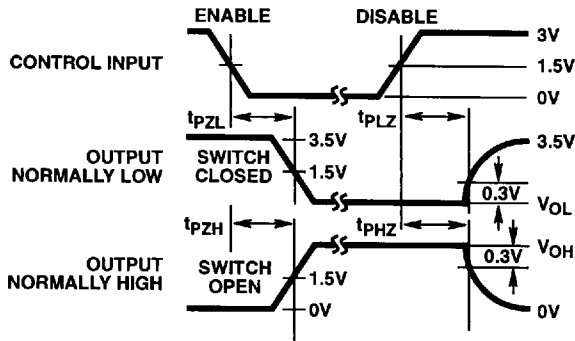


FIGURE 8. ENABLE AND DISABLE TIMING

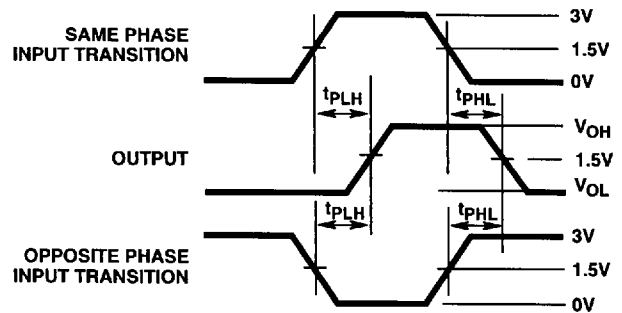
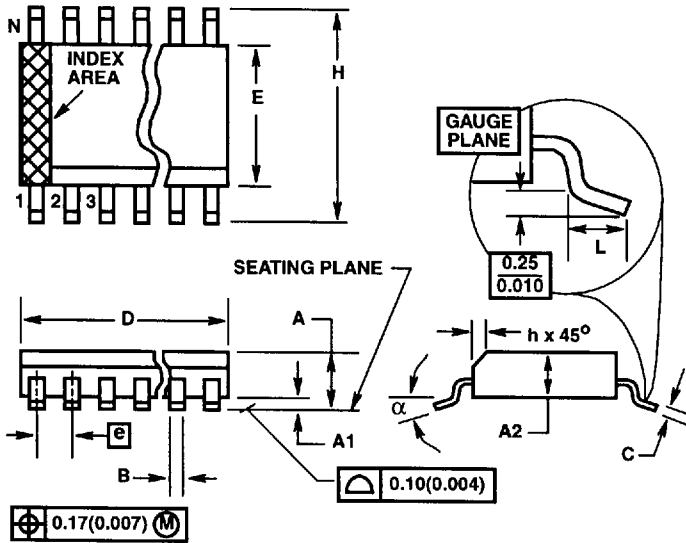


FIGURE 9. PROPAGATION DELAY

Shrink Small Outline Plastic Packages (SSOP)



M56.300-P  
56 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.720	0.730	18.29	18.54	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	56		56		5
$\alpha$	0°	8°	0°	8°	-

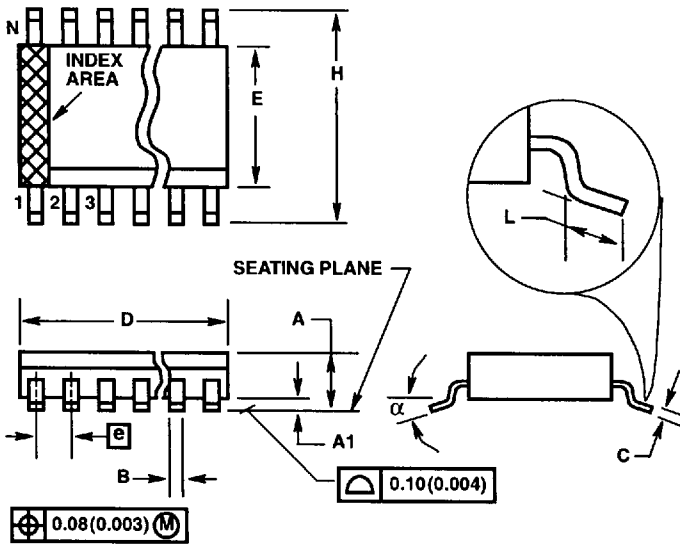
Rev. 0 5/96

NOTES:

1. These package dimensions are within allowable dimensions of JECEC MO-118-AB, Issue B.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
3. Dimension "E" does not include interlead flash or protrusions.
4. "L" is the length of terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.



Thin Shrink Small Outline Plastic Packages (TSSOP)



M56.240-P  
56 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.547	0.555	13.90	14.09	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	56		56		4
alpha	0°	8°	0°	8°	-

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NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
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