ISI IDEAL SEMICONDUCTOR INC.
"Your Best Defense Against Obsolescence"

51 58

54HCTLS 54HCTLS
74HCTLS 74HCTLS

OBJECTIVE SPECIFICATIONS

Dual AND-OR-Invert Gates and Dual AND-OR Gates

Features

- *Function, pin-out, speed and drive compatability with 54/74LS logic family*
- *Low power consumption characteristic of CMOS*
- *High-Drive-Current outputs: I_{OL} = 8 mA @ V_{OL} = 0.5V*
- *Inputs and outputs interface directly with TTL, NMOS and CMOS devices*
- *Wide operating voltage range: 4.5V to 5.5V*
- *Characterized for operation over industial and military temperature ranges:*

  74HCTLS: -40°C to +85°C
  54HCTLS: -55°C to +125°C

Description

The '51 performs the following Boolean functions:

$$1Y = \overline{(1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)}$$
$$2Y = \overline{(2A \bullet 2B) + (2C \bullet 2D)}$$

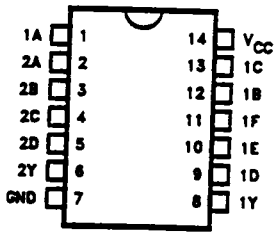
The '58 performs:

$$1Y = (1A \bullet 1B \bullet 1C) + (1D \bullet 1E \bullet 1F)$$
$$2Y = (2A \bullet 2B) + (2C \bullet 2D)$$

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



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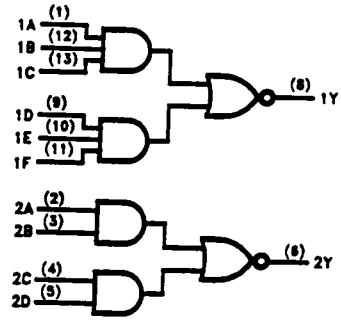
Function Table

Inputs						Output 1Y	
1A	1B	1C	1D	1E	1F	'51	'58
H	H	H	X	X	X	L	H
X	X	X	H	H	H	L	H
Any Other Combination						H	L

Inputs				Output 2Y	
2A	2B	2C	2D	'51	'58
H	H	X	X	L	H
X	X	H	H	L	H
Any Other Combination				H	L

Logic Diagrams

'51



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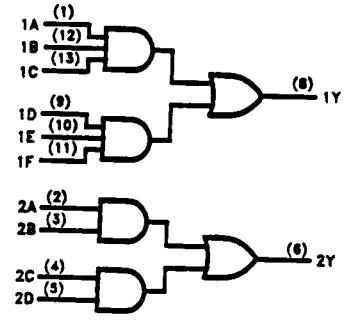
'58



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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} .....-0.5V to 7V
DC Input Diode Current, I_{IK}
(V_I <-0.5V or V_I >V_{CC} + 0.5V).....±20 mA
DC Output Diode Current, I_{OK}
(V_O <-0.5V or V_O >V_{CC} + 0.5V).....±20 mA
Continuous Output Current Per Pin, I_O
(-0.5V < V_O < V_{CC} + 0.5V).....±35 mA
Continuous Current Through
V_{CC} or GND pins.....±125 mA
Storage Temperature Range, T_{STG} .....-65°C to +150°C
Power Dissipation Per Package, P_D •.....500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

•Power Dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} .....4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} .....0V to V_{CC}

Operating Temperature

Range 74HCTLS: -40°C to +85°C
54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r, t_f .....Max 500 ns

*Unused inputs must always to tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ±10% Unless Otherwise Specified)

Sym	Parameter	Test Conditions	T_A = 25°C	74HCTLS T_A = -40°C to +85°C	54HCTLS T_A = -55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = -20 µA	V_{CC}	V_{CC} -0.1	V_{CC} -0.1	V_{CC} -0.1	V
		I_O = -4 mA	4.2	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = 20 µA	0	0.1	0.1	0.1	V
		I_O = 4 mA		0.26	0.33	0.4	
		I_O = 8 mA		0.39	0.5		
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA		2.0	20.0	40.0	µA

AC Electrical Characteristics (Input t_r, $t_f \leq 6$ ns), HCTLS51, HCTLS58

Sym	Parameter	Conditions •	T_A = 25°C VCC - 5.0V	74HCTLS T_A = -40°C to +85°C V_{CC} = 5.0V ±10%	54HCTLS T_A = -55°C to +125°C V_{CC} = 5.0V ±10%	Unit
			Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	15	20	25	30	ns
t_{PHL}			15	20	25	30	
C_{IN}	Maximum Input Capacitance						pF
C_{PD}	Power Dissipation Capacitance*	(per gate)					pF

*C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$
• For AC switching test circuits and timing waveforms see section 2.