

MITSUBISHI LSI

M5M82C55AP-2/FP-2/J-2

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

DESCRIPTION

The M5M82C55AP-2 is a family of general-purpose programmable input/output devices designed for use with the 8/16-bit parallel CPU as input/output ports.

This device is fabricated using silicon-gate CMOS technology for a single supply voltage. This LSI is having 24 input/output pins which correspond to three 8-bit input/output ports. It is housed in a 40-pin plastic molded DIP.

And preparatory for surface equipment M5M82C55AP-2 (SOP) and M5M82C55AJ-2 (PLCC).

FEATURES

- 120nsec access time
- Having internal anti-noise circuit on RESET, $\overline{\text{ACK}}$ and STB pins
- Single 5 V supply voltage
- TTL compatible
- Improved DC driving capability
- Improved timing characteristics
- 24 programmable I/O pins
- Direct bit set/reset capability

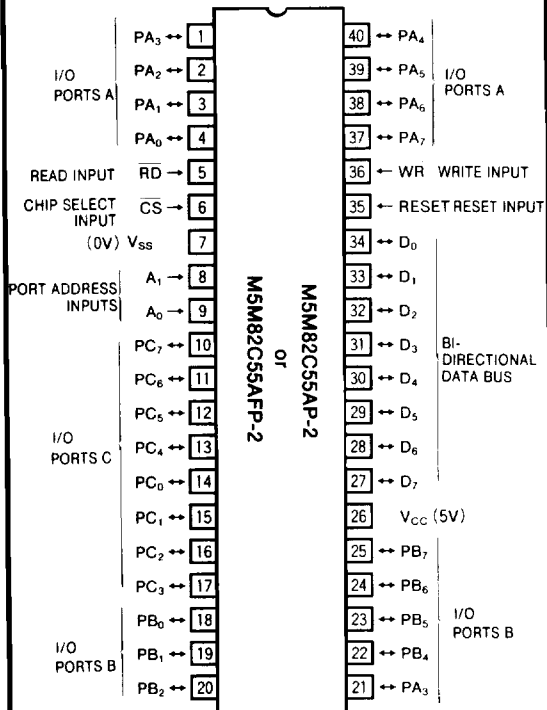
APPLICATION

Input/output ports for microprocessor

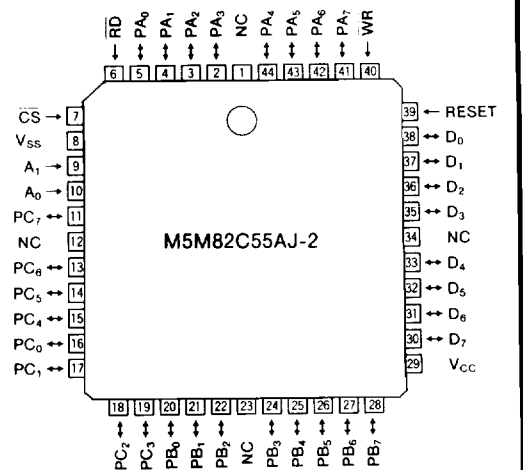
FUNCTION

These PPIs have 24 input/output pins which may be individually programmed in two 12-bit groups A and B with mode control commands from a CPU. They are used in three major modes of operation, mode 0, mode 1 and mode 2. Operating in mode 0, each group of 12 pins may be programmed in sets of 4 to be inputs or outputs. In mode 1, the 24 I/O terminals may be programmed in two 12-bit groups, group A and group B. Each group contains one 8-bit data port, which may be programmed to serve as input or output, and one 4-bit control port used for handshaking and interrupt control signals. Mode 2 is used with group A only, as one 8-bit bidirectional bus port and one 5-bit control port. Bit set/reset is controlled by CPU. A high-level reset input (RESET) clears control register, and all ports are set to the input mode (high-impedance state).

PIN CONFIGURATION (TOP VIEW)



Outline 40P4 (M5M82C55AP-2) Outline 40P2R (M5M82C55AFP-2)

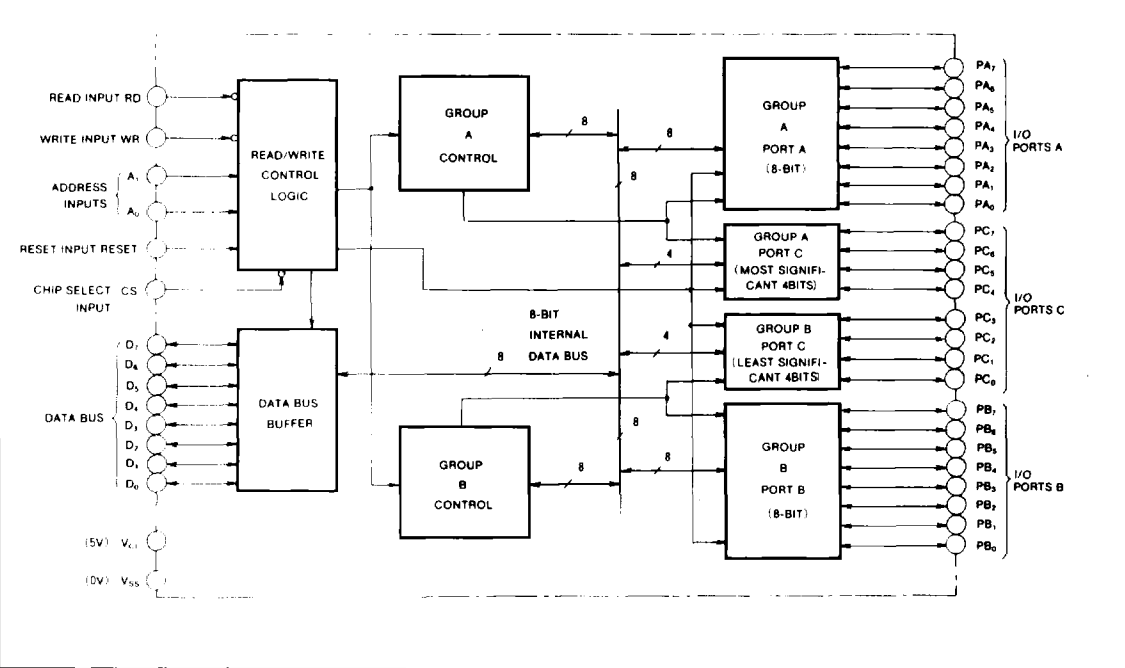


Outline 44P0

NC : NO CONNECTION

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BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

RD (Read) Input

At low-level, the status or the data at the port is transferred to the CPU from the PPI. In essence, it allows the CPU to read data from the PPI.

WR (Write) Input

At low-level, the data or control words are transferred from the CPU and written in the PPI.

A₀, A₁ (Port address) Input

These input signals are used to select one of the three ports: port A, port B, and port C, or the control register. They are normally connected to the least significant 2 bits of the address bus.

RESET (Reset) Input

At high-level, the control register is cleared. Then all ports are set to the input mode (high-impedance state).

CS (Chip-Select) Input

At low-level, the communication between the PPI and the CPU is enabled. While at high-level, the data bus is kept in the high-impedance state, so that commands from the CPU are ignored. Then the previous data is kept at the output port.

Read/Write Control Logic

The function of this block is to control transfers of both data and control words. It accepts the address signals (A₀, A₁, CS), I/O control signals (RD, WR) and RESET signal, and then issues commands to both of the control groups in the PPI.

Data Bus Buffer

This three-state, bidirectional, 8-bit buffer is used to transfer the data when an input or output instruction is executed by the CPU. Control words and status information are also transferred through the data bus buffer.

Group A and Group B Control

Accepting commands from the read/write control logic, the control blocks (Group A, Group B) receive 8-bit control words from the internal data bus and issue the proper commands for the associated ports. Control group A is associated with port A and the 4 high-order bits of port C. Control group B is associated with port B and the 4 low-order bits of port C. The control register, which stores control words, can only be written into.

Port A, Port B and Port C

The PPI contains three 8-bit ports whose modes and input/output settings are programmed by the system software.

Port A has an output latch/buffer and an input latch/buffer. Port B has an input-output latch/buffer. Port C has an output latch/buffer and an input buffer. Port C can be divided into two 4-bit ports which can be used as ports for control signals for port A and port B.

The basic operations are shown in Table 1.

Table 1 Basic Operations

A ₁	A ₀	CS	RD	WR	Operation
0	0	L	L	H	Data bus ← Port A
0	1	L	L	H	Data bus ← Port B
1	0	L	L	H	Data bus ← Port C
0	0	L	H	L	Port A ← Data bus
0	1	L	H	L	Port B ← Data bus
1	0	L	H	L	Port C ← Data bus
1	1	L	H	L	Control register ← Data bus
X	X	H	X	X	Data bus is in high-impedance state
1	1	L	L	H	Illegal condition

Bit Set/Reset

When port C is used as an output port, any 1bit of the 8-bit can be set (high) or reset (low) by a control word from the CPU. This bit set/reset can be operated in the same way as the mode set, but the control word format is different. This operation is also used for INTE (interrupt enable flag) set/reset in mode 1 and mode 2.

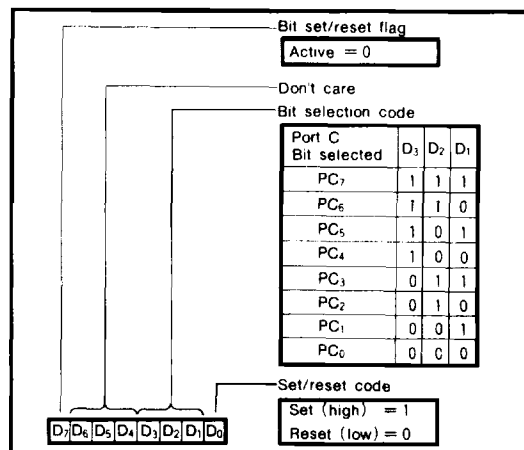


Fig. 1 Control word format for port C set/reset

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BASIC OPERATING MODES

The PPI can operate in any one of three selected basic modes.

Mode 0: Basic input/output (group A, group B)

Mode 1: Strobed input/output (group A, group B)

Mode 2: Bidirectional bus (group A only)

The mode of both group A and group B can be selected independently. The control word format for mode set is shown in Fig. 2.

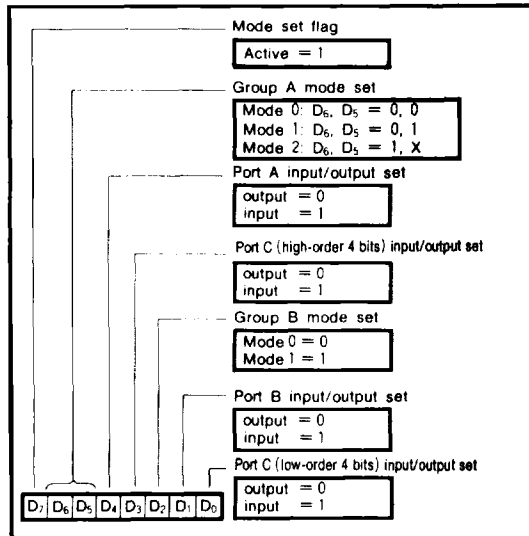
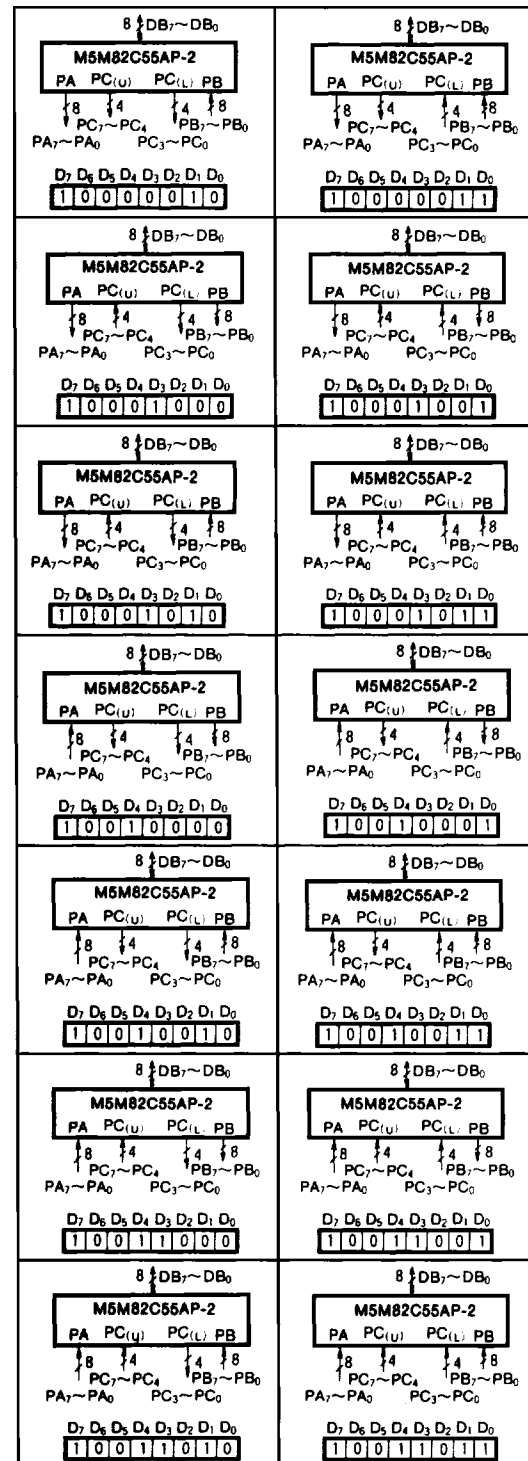
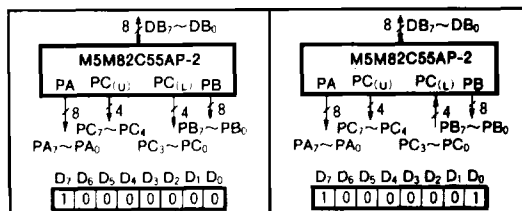


Fig. 2 Control word format for mode set.

1. Mode 0 (Basic Input/Output)

This functional configuration provides simple input and output operations for each of the 3 ports. No "handshaking" is required; data is simply written in, or read from, the specified port. Output data from the CPU to the port can be held, but input data from the port to the CPU cannot be held. Any one of the 8-bit ports and 4-bit ports can be used as an input port or an output port. The diagrams following show the basic input/output operating modes.



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2. Mode 1 (Strobed Input/Output)

This function can be set in both group A and B. Both groups are composed of one 8-bit data port and one 4-bit control data port. The 8-bit port can be used as an input port or an output port. The 4-bit port is used for control and status signals affecting the 8-bit data port. The following shows operations in mode 1 for using input ports.

STB (Strobe Input)

A low-level on this input latches the output data from the terminal units into the input register of the port. In short, this is a clock for data latching. The data from the terminal units can be latched by the PPI independent of the control signal from the CPU. This data is not sent to the data bus until the instruction IN is executed.

IBF (Input Buffer Full Flag Output)

A high-level on this output indicates that the data from the terminal units has been latched into the input register. IBF is set to high-level by the falling edge of the STB input, and is reset to low-level by the rising edge of the RD input.

INTR (Interrupt Request Output)

This can be used to interrupt the CPU when an input device is requesting service. When INTE (interrupt enable flag) of the PPI is high-level, INTR is set to high-level by the rising edge of the STB input and is reset to low-level by the falling edge of RD input.

INTE_A of group A is controlled by bit setting of PC₄. INTE_B of group B is controlled by bit setting of PC₂.

Mode 1 input state is shown in Fig. 3, and the timing diagram is shown in Fig. 4.

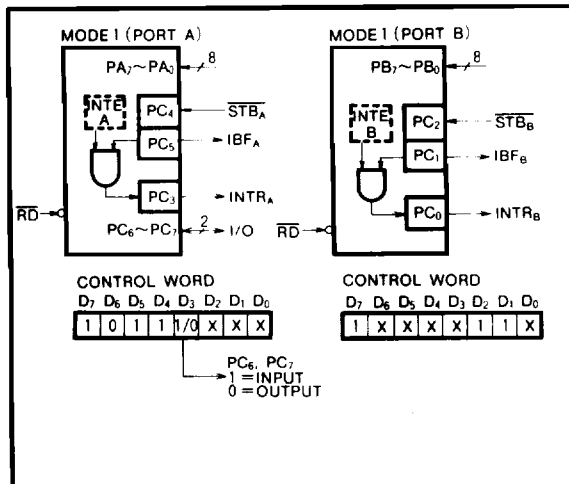


Fig. 3 An example of mode 1 input state

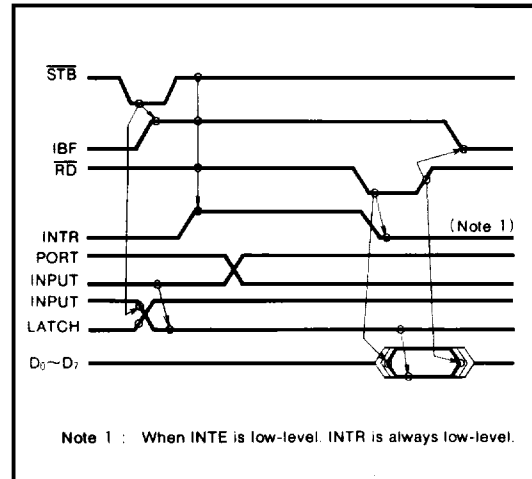


Fig. 4 Timing diagram

The following shows operations using mode 1 for output ports.

OBF (Output Buffer Full Flag Output)

This is reset to low-level by the rising edge of the WR signal and is set to high-level by the falling edge of the ACK (acknowledge input). In essence, the PPI indicates to the terminal units by the OBF signal that the CPU has sent data to the port.

ACK (Acknowledge Input)

Receiving this signal from a terminal unit can indicate to the PPI that the terminal unit has accepted data from a port.

INTR (Interrupt Request)

When a peripheral unit is accepting data from the CPU, setting INTR to high-level can be used to interrupt the CPU. When INTE (interrupt enable flag) is high-level and OBF is set to high-level by the rising edge of an ACK signal, then INTR will also be set to high-level by the rising edge of the ACK signal. Also, INTR is reset to low-level by the falling edge of the WR signal when the PPI has been receiving data from the CPU.

INTE_A of group A is controlled by bit setting of PC₆. INTE_B of group B is controlled by bit setting of PC₂.

Mode 1 output state is shown in Fig. 5, and the timing diagram is shown in Fig. 6.

Combinations for using port A and port B as input or output in mode 1 are shown in Fig. 7 and Fig. 8.

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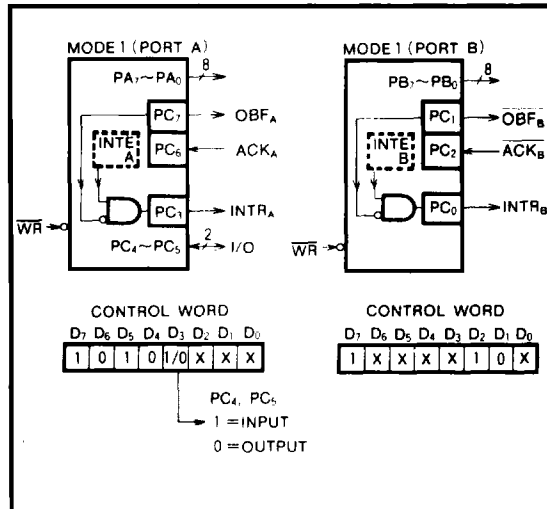


Fig. 5 An example of mode 1 output state

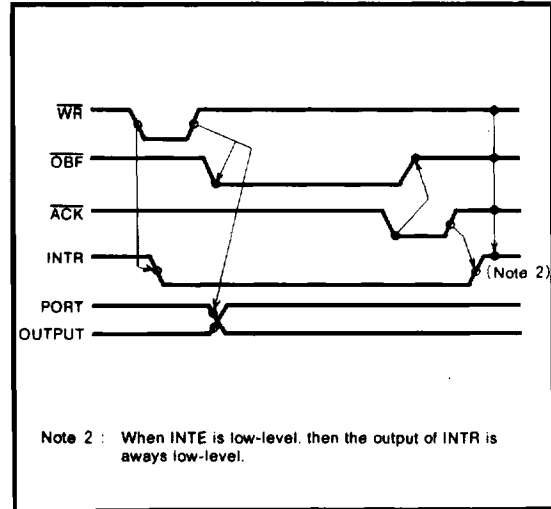


Fig. 6 Timing diagram

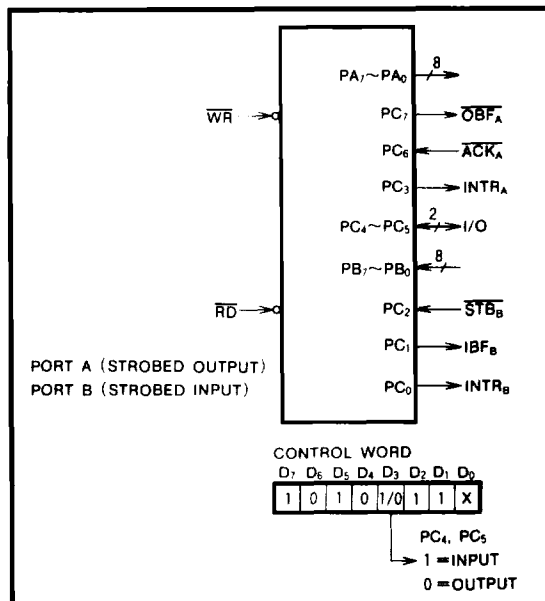


Fig. 7 Mode 1 port A and port B I/O example

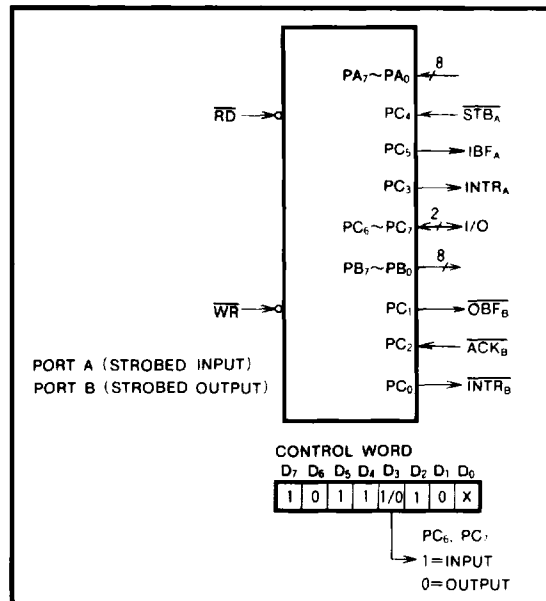


Fig. 8 Mode 1 port A and port B I/O example

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3. Mode 2 (Strobed Bidirectional Bus Input/Output)

Mode 2 can provide bidirectional operations, using one 8-bit bus for communicating with terminal units. Mode 2 is only valid with group A and uses one 8-bit bidirectional bus port (port A) and a 5-bit control port (high-order 5 bits of port C). The bus port (port A) has two internal registers, one for input and the other for output. On the other hand, the control port (port C) is used for communicating control signals and bus-status signals. These control signals are similar to mode 1 and can also be used to control interruption of the CPU. When group A is programmed as mode 2, group B can be programmed independently as mode 0 or mode 1. When group A is in mode 2, the following 5 control signals can be used.

OBF (Output Buffer Full Flag Output)

The OBF output will go low-level to indicate that the CPU has sent data to the internal register of port A. This signal lets the terminal units know that the data is ready for transfer from the CPU. When this occurs, port A remains in the floating (high-impedance) state.

ACK (Acknowledge Input)

A low-level ACK input will cause the data of the internal register to be transferred to port A. For a high-level ACK input, the output buffer will be in the floating (high-impedance) state.

STB (Strobe Input)

When the STB input is low-level, the data from terminal units will be held in the internal register, and the data will be sent to the system data bus with an RD signal to the PPI.

IBF (Input Buffer Full Flag Output)

When data from terminal units is held on the internal register, IBF will be high-level.

INTR (Interrupt Request Output)

This output is used to interrupt the CPU and its operations the same as in mode 1. There are two interrupt enable flags that correspond to INTE_A for mode 1 output and mode 1 input.

INTE₁ is used in generating INTR signals in combination with OBF and ACK. INTE₁ is controlled by bit setting of PC₆.

INTE₂ is used in generating INTR signals in combination with IBF and STB. INTE₂ is controlled by bit setting of PC₄.

Fig. 9 shows the timing diagram of mode 2, and Fig. 10 is an example of mode 2 operation.

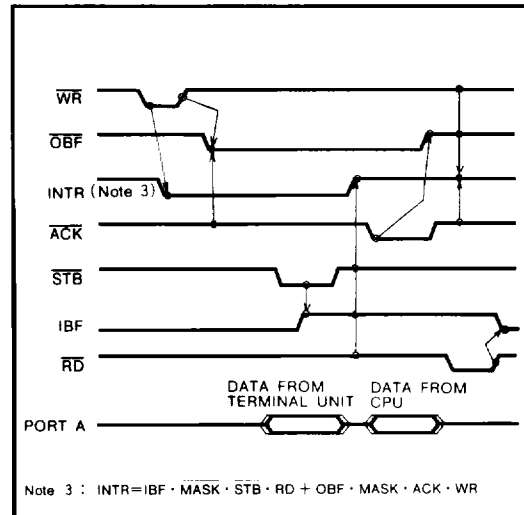


Fig. 9 Mode 2 timing diagram

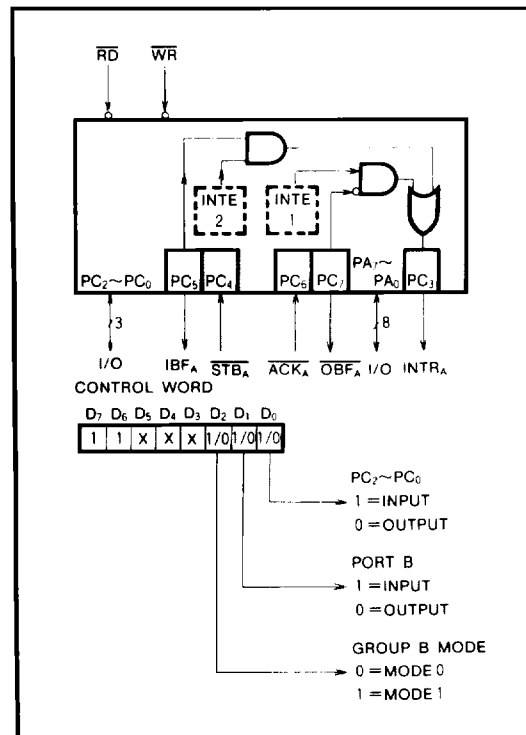


Fig. 10 An example of mode 2 operation

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4. Control Signal Read

In mode 1 or mode 2 when using port C as a control port, by CPU execution of an IN instruction, each control signal and bus status from port C can be read.

5. Control Word Tables

Control word formats and operation details for mode 0, mode 1, mode 2 and set/reset control of port C are given in Tables 3, 4, 5 and 6, respectively.

Table 2 Read-out control signals

Data Mode	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Mode 1, input	I/O	I/O	IBF _A	INTE _A	INTR _A	INTE _B	IBF _B	INTR _B
Mode 1, output	OBF _A	INTE _A	I/O	I/O	INTR _A	INTE _B	OBF _B	INTR _B
Mode 2	OBF _A	INTE _A	IBF _A	INTE ₂	INTR _A	By group B mode		

Table 3 Mode 0 control words

Control words								Hexadecimal	Group A		Group B	
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		Port A	Port C (high-order 4 bits)	Port C (low-order 4 bits)	Port B
1	0	0	0	0	0	0	0	80	OUT	OUT	OUT	OUT
1	0	0	0	0	0	0	1	81	OUT	OUT	IN	OUT
1	0	0	0	0	0	1	0	82	OUT	OUT	OUT	IN
1	0	0	0	0	0	1	1	83	OUT	OUT	IN	IN
1	0	0	0	1	0	0	0	88	OUT	IN	OUT	OUT
1	0	0	0	1	0	0	1	89	OUT	IN	IN	OUT
1	0	0	0	1	0	1	0	8A	OUT	IN	OUT	IN
1	0	0	0	1	0	1	1	8B	OUT	IN	IN	IN
1	0	0	1	0	0	0	0	90	IN	OUT	OUT	OUT
1	0	0	1	0	0	0	1	91	IN	OUT	IN	OUT
1	0	0	1	0	0	1	0	92	IN	OUT	OUT	IN
1	0	0	1	0	0	1	1	93	IN	OUT	IN	IN
1	0	0	1	1	0	0	0	98	IN	IN	OUT	OUT
1	0	0	1	1	0	0	1	99	IN	IN	IN	OUT
1	0	0	1	1	0	1	0	9A	IN	IN	OUT	IN
1	0	0	1	1	0	1	1	9B	IN	IN	IN	IN

Note 4 : OUT indicates output port, and IN indicates input port.

Table 4 Mode 1 control words

Control words								Hexadecimal	Group A					Group B			
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		Port A	Port C				Port C			Port B
										PC ₇	PC ₆	PC ₅	PC ₄	PC ₃	PC ₂	PC ₁	PC ₀
1	0	1	0	0	1	0	X	A4	OUT	OBF _A	ACK _A	OUT	INTR _A	ACK _B	OBF _B	INTR _B	OUT
1	0	1	0	0	1	1	X	A5									
1	0	1	0	0	1	1	X	A6	OUT	OBF _A	ACK _A	OUT	INTR _A	STB _B	IBF _B	INTR _B	IN
1	0	1	0	1	1	0	X	AC	OUT	OBF _A	ACK _A	IN	INTR _A	ACK _B	OBF _B	INTR _B	OUT
1	0	1	0	1	1	1	X	AD									
1	0	1	0	1	1	1	X	AE	OUT	OBF _A	ACK _A	IN	INTR _A	STB _B	IBF _B	INTR _B	IN
1	0	1	1	0	1	0	X	AF									
1	0	1	1	0	1	0	X	B4	IN	OUT	IBF _A	STB _A	INTR _A	ACK _B	OBF _B	INTR _B	OUT
1	0	1	1	0	1	1	X	B5									
1	0	1	1	0	1	1	X	B6	IN	OUT	IBF _A	STB _A	INTR _A	STB _B	IBF _B	INTR _B	IN
1	0	1	1	1	1	0	X	B7									
1	0	1	1	1	1	0	X	BC	IN	IN	IBF _A	STB _A	INTR _A	ACK _B	OBF _B	INTR _B	OUT
1	0	1	1	1	1	1	X	BD									
1	0	1	1	1	1	1	X	BE	IN	IN	IBF _A	STB _A	INTR _A	STB _B	IBF _B	INTR _B	IN
								BF									

Note 5 : Mode of group A and group B can be programmed independently.

Note 6 : It is not necessary for both group A and group B to be in mode 1.

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Table 5 Mode 2 control words

Control words								Hexa-decimal (Ex)	Group A						Group B			
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		Port A	Port C				PortC		Port B		
									PC ₇	PC ₆	PC ₅	PC ₄	PC ₃	PC ₂	PC ₁	PC ₀		
1	1	X	X	X	0	0	0	C0	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	OUT			
1	1	X	X	X	0	0	1	C1	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	IN			
1	1	X	X	X	0	1	0	C2	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	OUT			
1	1	X	X	X	0	1	1	C3	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	IN			
1	1	X	X	X	1	0	X	C4	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	<u>ACK_B</u>	<u>OBF_B</u>	<u>INTR_B</u>	
1	1	X	X	X	1	1	X	C6	Bidirectional bus	<u>OBF_A</u>	<u>ACK_A</u>	<u>IBF_A</u>	<u>STB_A</u>	<u>INTR_A</u>	<u>STB_B</u>	<u>IBF_B</u>	<u>INTR_B</u>	

Table 6 Port C bit set/reset control words

Control words								Hexa-decimal	Port C								Remarks
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		PC ₇	PC ₆	PC ₅	PC ₄	PC ₃	PC ₂	PC ₁	PC ₀	
0	X	X	X	0	0	0	0	00								0	
0	X	X	X	0	0	0	1	01								1	
0	X	X	X	0	0	1	0	02							0		
0	X	X	X	0	0	1	1	03							1		
0	X	X	X	0	1	0	0	04						0			INTE _B set/reset for mode 1 input
0	X	X	X	0	1	0	1	05						1			INTE _B set/reset for mode 1 output
0	X	X	X	0	1	1	0	06					0				
0	X	X	X	0	1	1	1	07					1				
0	X	X	X	1	0	0	0	08				0					INTE _A set/reset for mode 1 input
0	X	X	X	1	0	0	1	09				1					INTE ₂ set/reset for mode 2
0	X	X	X	1	0	1	0	0A			0						
0	X	X	X	1	0	1	1	0B			1						
0	X	X	X	1	1	0	0	0C		0							INTE _A set/reset for mode 1 output
0	X	X	X	1	1	0	1	0D		1							INTE ₁ set/reset for mode 2
0	X	X	X	1	1	1	0	0E	0								
0	X	X	X	1	1	1	1	0F	1								

Note 7 : The terminals of port C should be programmed for the output mode, before the bit set/reset operation is executed.
8 : Also used for controlling the interrupt enable flag (INTE).

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings		Unit
V_{CC}	Supply voltage		-0.3~7		V
V_I	Input voltage	With respect to V_{SS}	-0.3~ $V_{CC}+0.3$		V
V_O	Output voltage		-0.3~ $V_{CC}+0.3$		V
I_{OHMAX}	MAX "H" Output current	All output and I/O pins output "H" level and force same current.	Port	-4	mA
			Data bus	-500	μ A
I_{OLMAX}	MAX "L" Output current	All output and I/O pins output "L" level and force same current.2	Port	4	mA
			Data bus	2.5	
T_{opr}	Operating free-air temperature range		-20~75		°C
T_{stg}	Storage temperature range		-65~150		°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage (GND)		0		V

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim 75^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage		-0.3		0.8	V
V_{OH}	Output high voltage (Note10)	$I_{OH} = -400\mu\text{A}$	2.4			V
		$I_{OH} = -20\mu\text{A}$	4.4			
V_{OL}	Output low voltage (Note10)	$I_{OL} = 2.5\text{mA}$			0.4	V
I_{CC}	Supply current from V_{CC}	All input mode. RESET=0V. Other pins= V_{CC} .			10	μ A
I_{IL}	Input leak current	$V_I = 0V$, V_{CC}			± 10	μ A
I_{OZ}	Off-state output current	$V_O = 0V \sim V_{CC}$			± 10	μ A
C_i	Input terminal capacitance	$f = 1\text{MHz}$			10	pF
$C_{i/O}$	Input/output terminal capacitance	Unmeasured pins=0V			20	pF

Note 9 : Current flowing into an IC is positive, out is negative.
10 : Output current must be less than $\pm 4\text{mA}$ for each Port pin.

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TIMING REQUIREMENTS ($T_a = -20 \sim 75^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(R)}$	Read pulse width		160			ns
$t_{SU(PE-R)}$	Peripheral setup time before read		0			ns
$t_{H(R-PE)}$	Peripheral hold time after read		0			ns
$t_{SU(A-R)}$	Address setup time before read		0			ns
$t_{H(R-A)}$	Address hold time after read		0			ns
$t_{W(W)}$	Write pulse width		120			ns
$t_{SU(DQ-W)}$	Data setup time before write		100			ns
$t_{H(W-DQ)}$	Data hold time after write		0			ns
$t_{SU(A-W)}$	Address setup time before write		0			ns
$t_{H(W-A)}$	Address hold time after write		0			ns
$t_{W(ACK)}$	Acknowledge pulse width		300			ns
$t_{W(STB)}$	Strobe pulse width		350			ns
$t_{SU(PE-STB)}$	Peripheral setup time before strobe		0			ns
$t_{H(STB-PE)}$	Peripheral hold time after strobe		150			ns
$t_{C(RW)}$	Read/write cycle time		200			ns

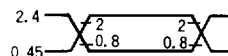
SWITCHING CHARACTERISTICS ($T_a = -20 \sim 75^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{PVZ(R-DQ)}$	Propagation time from read to data output				120	ns
$t_{PZV(R-DQ)}$	Propagation time from read to data floating (Note11)		10		85	ns
$t_{PHL(W-PE)}$	Propagation time from write to output				350	ns
$t_{PLH(W-PE)}$	Propagation time from write to output				350	ns
$t_{PLH(STB-IBF)}$	Propagation time from strobe to IBF flag				300	ns
$t_{PLH(STB-INTR)}$	Propagation time from strobe to interrupt				300	ns
$t_{PHL(R-INTR)}$	Propagation time from read to interrupt				400	ns
$t_{PHL(R-IBF)}$	Propagation time from read to IBF flag				300	ns
$t_{PHL(W-INTR)}$	Propagation time from write to interrupt				450	ns
$t_{PHL(W-OBF)}$	Propagation time from write to OBF flag				300	ns
$t_{PLH(ACK-OBF)}$	Propagation time from acknowledge to OBF flag				350	ns
$t_{PLH(ACK-INTR)}$	Propagation time from acknowledge to interrupt				350	ns
$t_{PVZ(ACK-PE)}$	Propagation time from acknowledge to data output				300	ns
$t_{PZV(ACK-PE)}$	Propagation time from acknowledge to data floating (Note11)		20		250	ns

Note 11 : Test conditions are not applied.

Note 12 : A.C Testing waveform

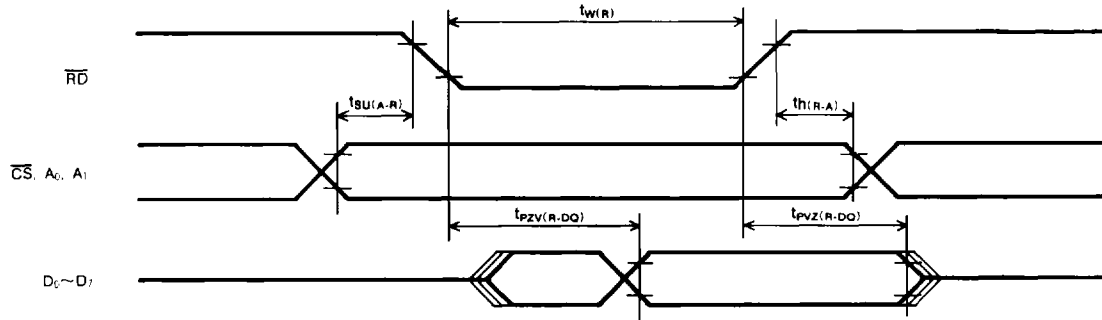
Input pulse level 0.45~2.4V
 Input pulse rise time 10ns
 Input pulse fall time 10ns
 Reference level input $V_{IH} = 2V$, $V_{IL} = 0.8V$
 output $V_{OH} = 2V$, $V_{OL} = 0.8V$



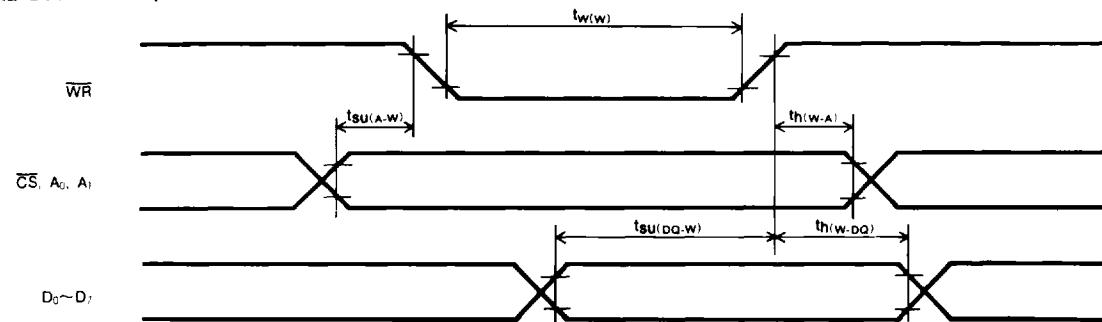
CMOS PROGRAMMABLE PERIPHERAL INTERFACE

TIMING DIAGRAM

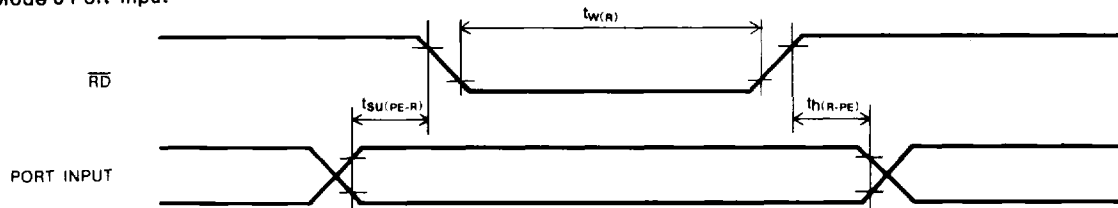
Data Bus Read Operation



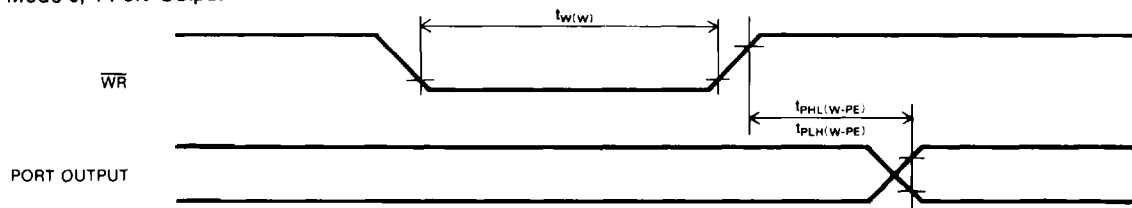
Data Bus Write Operation



Mode 0 Port Input

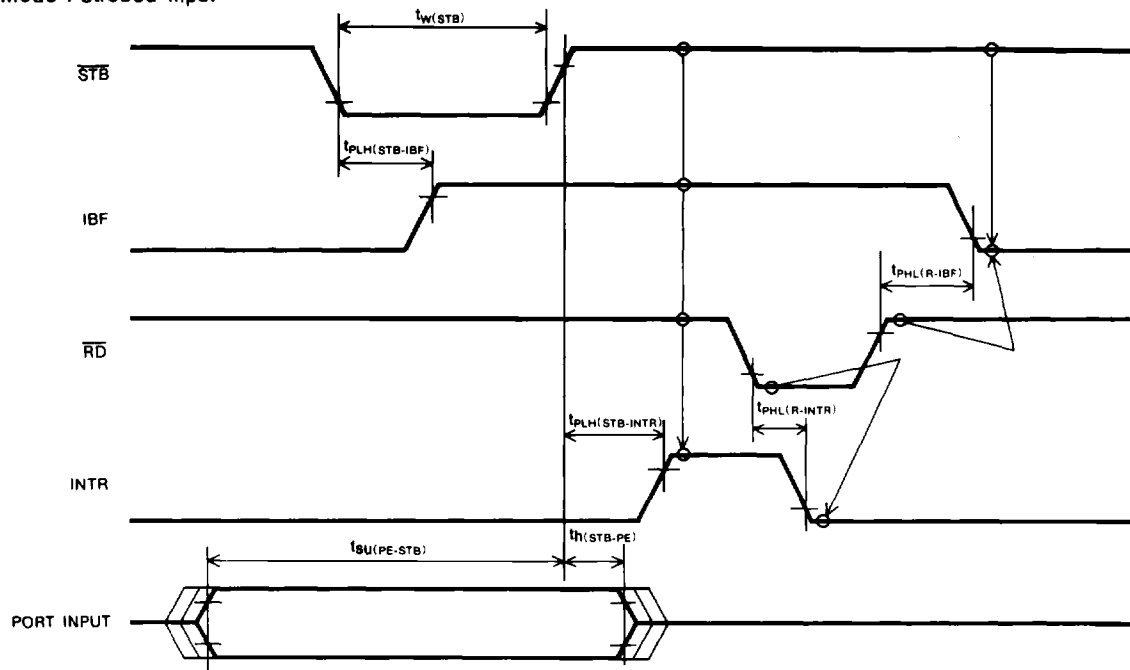


Mode 0, 1 Port Output

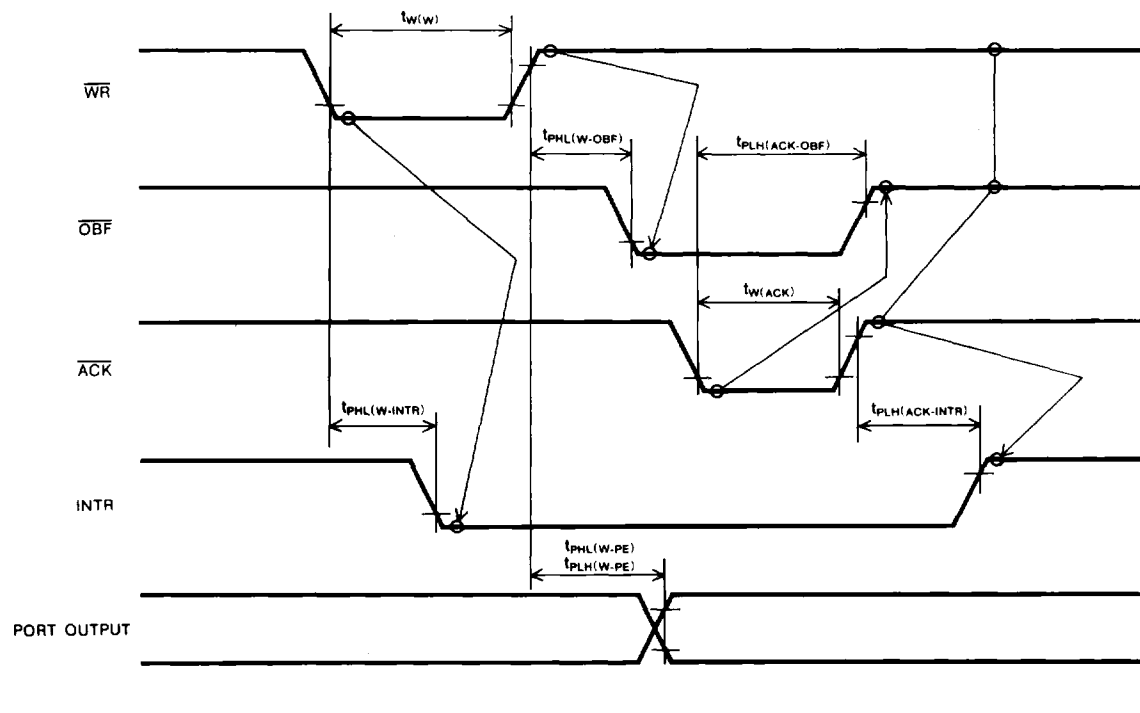


CMOS PROGRAMMABLE PERIPHERAL INTERFACE

Mode 1 Strobed Input

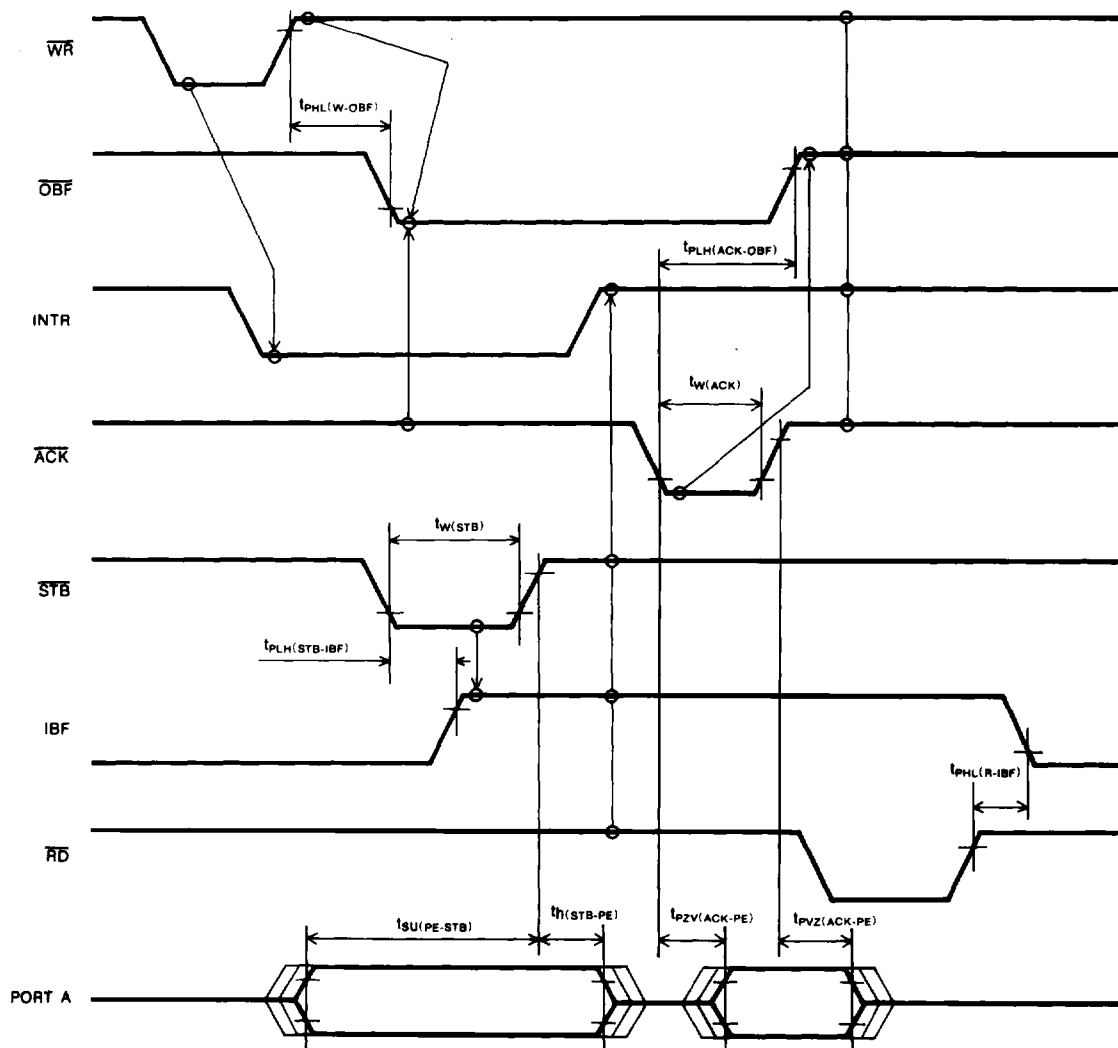


Mode 1 Strobed Output



CMOS PROGRAMMABLE PERIPHERAL INTERFACE

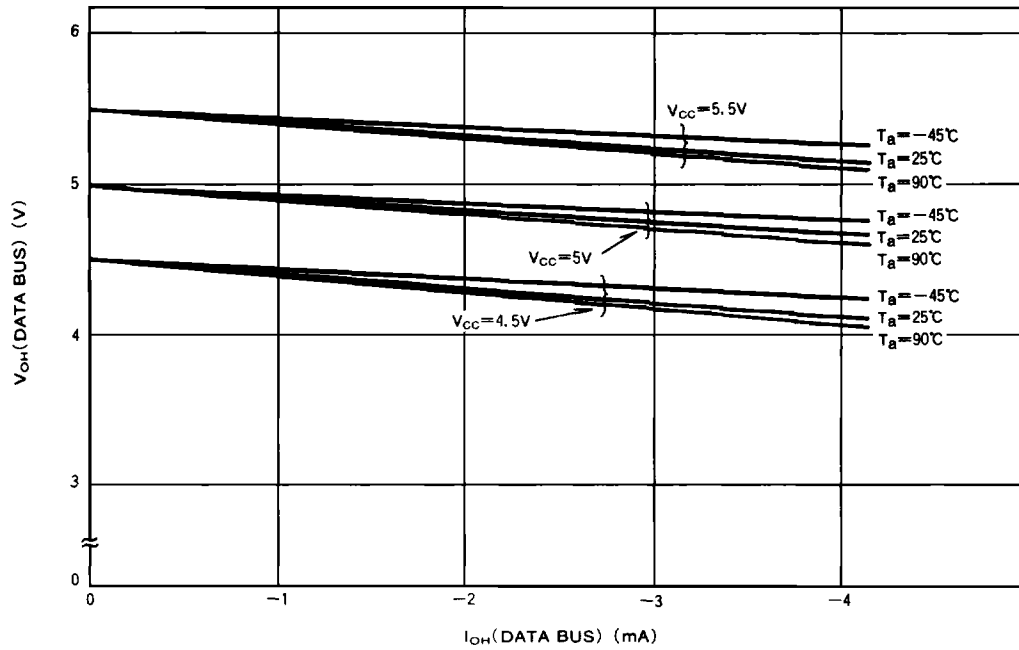
Mode 2 Bidirectional



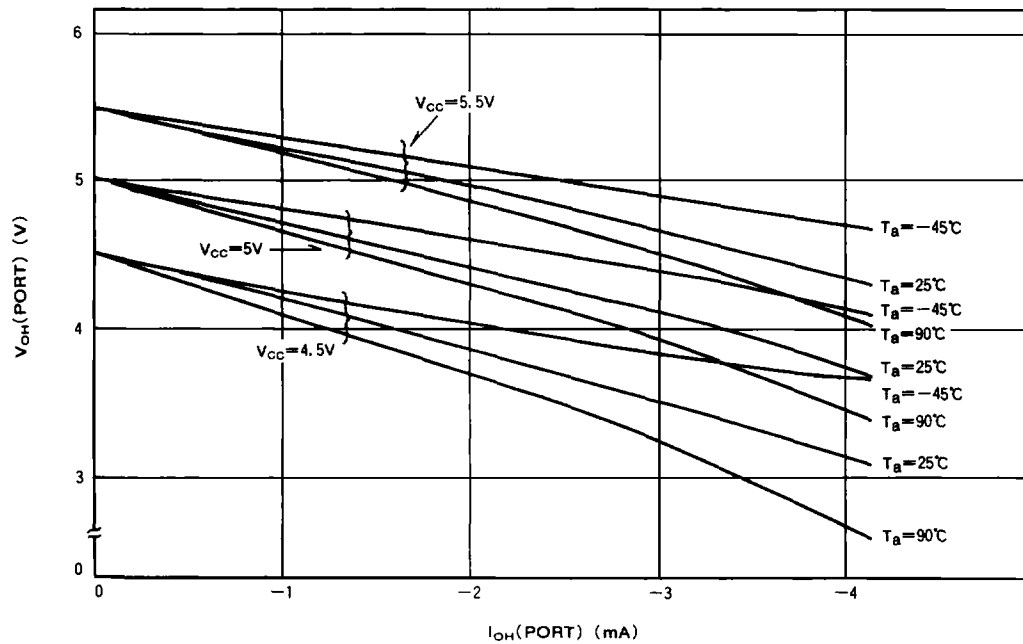
Note 13: $INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$

CMOS PROGRAMMABLE PERIPHERAL INTERFACE

$V_{OH}-I_{OH}$ CHARACTERISTICS (DATA BUS)

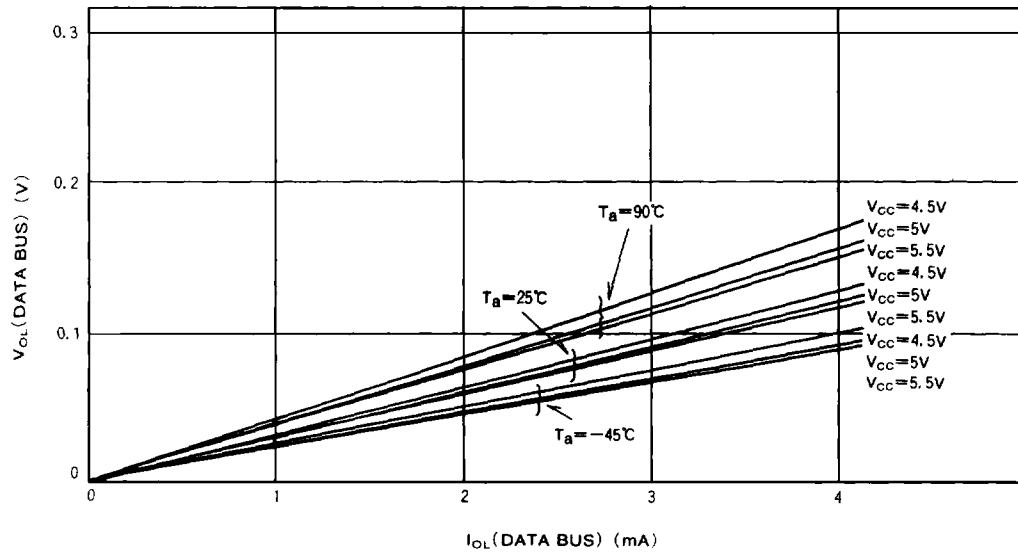


$V_{OH}-I_{OH}$ CHARACTERISTICS (PORT)



CMOS PROGRAMMABLE PERIPHERAL INTERFACE

$V_{OL}-I_{OL}$ CHARACTERISTICS (DATA BUS)



$V_{OL}-I_{OL}$ CHARACTERISTICS (PORT)

