



Integrated Device Technology, Inc.

# HIGH-PERFORMANCE CMOS BUS INTERFACE LATCHES

**IDT54/74FCT841A/B-  
IDT54/74FCT846A/B**  
(Replaces 39C841-46)

## FEATURES:

- Equivalent to AMD's Am29841-46 bipolar registers in pinout/function, speeds and output drive over full temperature and voltage supply extremes
- High-speed parallel latches
  - Non-inverting transparent  $t_{PD} = 5.5\text{ns typ.}$
  - Inverting transparent  $t_{PD} = 6.0\text{ns typ.}$
- Buffered common latch enable, clear and preset input
- $I_{OL} = 48\text{mA (commercial)}$  and  $32\text{mA (military)}$
- Clamp diodes on all inputs for ringing suppression
- CMOS power levels ( $5\mu\text{W typ. static}$ )
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 Series ( $5\mu\text{A max.}$ )
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

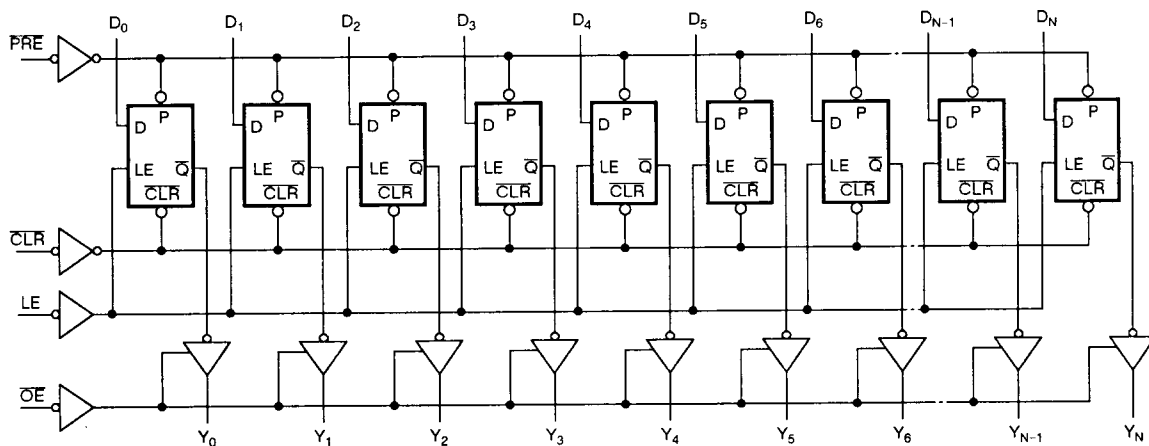
## DESCRIPTION:

The IDT54/74FCT800 Series is built using advanced CEMOS™, a dual metal CMOS technology.

The IDT54/74FCT800 Series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The IDT54/74FCT841 and IDT54/74FCT842 are buffered, 10-bit wide versions of the popular '373 function. The IDT54/74FCT843 and IDT54/74FCT844 are 9-bit wide buffered latches with Preset (PRE) and Clear (CLR) — ideal for parity bus interfacing in high-performance systems. The IDT54/74FCT845 and IDT54/74FCT846 are 8-bit buffered latches with all the '843/4 controls plus multiple enables ( $\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$ ) to allow multiuser control of the interface, e.g., CS, DMA and RD/WR. They are ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

All of the IDT54/74FCT800 high-performance interface family are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

## FUNCTIONAL BLOCK DIAGRAM



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## PRODUCT SELECTOR GUIDE

	DEVICE		
	10-BIT	9-BIT	8-BIT
Non-inverting	54/74FCT841A/B	54/74FCT843A/B	54/74FCT845A/B
Inverting	54/74FCT842A/B	54/74FCT844A/B	54/74FCT846A/B

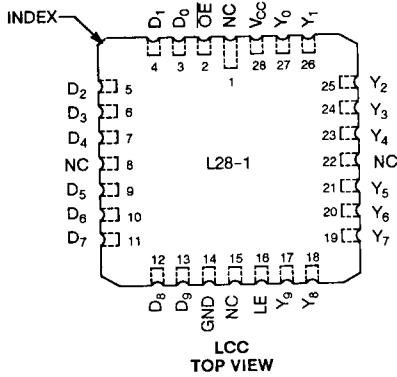
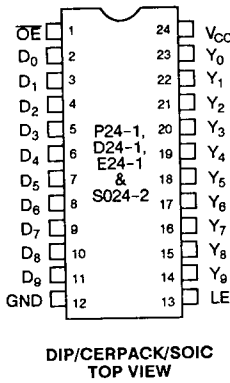
CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

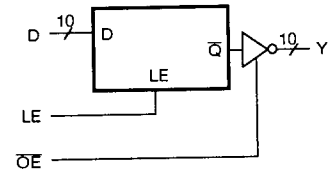
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**PIN CONFIGURATIONS**

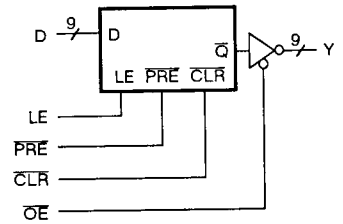
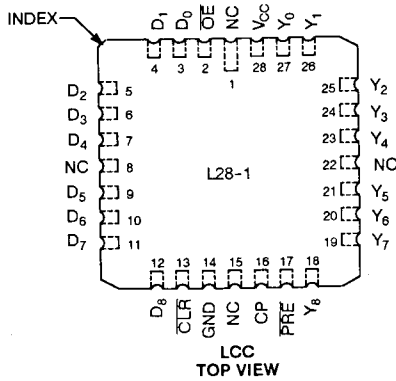
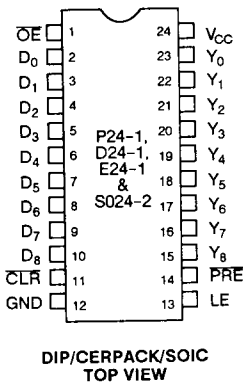
**IDT54/74FCT841/IDT54/74FCT842 10-BIT LATCHES**



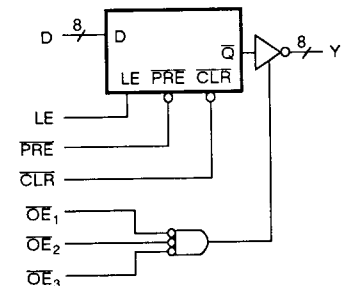
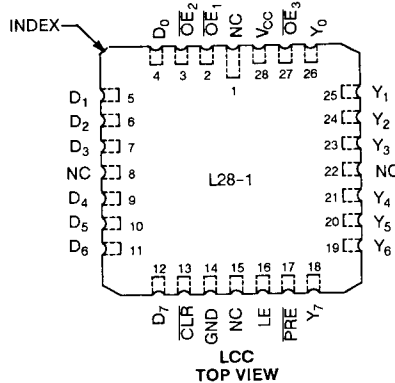
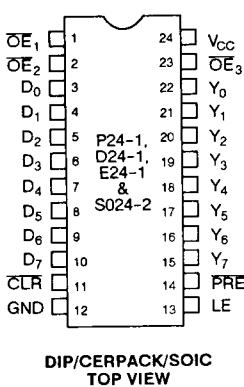
**LOGIC SYMBOLS**



**IDT54/74FCT843/IDT54/74FCT844 9-BIT LATCHES**



**IDT54/74FCT845/IDT54/74FCT846 8-BIT LATCHES**



**PIN DESCRIPTION**

NAME	I/O	DESCRIPTION
<b>IDT54/74FCT841/43/45 (Non-inverting)</b>		
CLR	I	When CLR is low, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
D <sub>i</sub>	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y <sub>i</sub>	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y <sub>i</sub> are in the high-impedance (off) state.
PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.
<b>IDT54/74FCT842/44/46 (Inverting)</b>		
CLR	I	When CLR is low, the outputs are LOW if OE is LOW. When CLR is HIGH, data can be entered into the latch.
D <sub>i</sub>	I	The latch inverting data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y <sub>i</sub>	O	The 3-state latch outputs.
OE	I	The output enable control. When OE is LOW, the outputs are enabled. When OE is HIGH, the outputs Y <sub>i</sub> are in the high-impedance (off) state.
PRE	I	Preset line. When PRE is LOW, the outputs are HIGH if OE is LOW. Preset overrides CLR.

**FUNCTION TABLES <sup>(1)</sup>**  
**IDT54/74FCT841/43/45**

INPUTS					INTER- NAL	OUT- PUTS	FUNCTION
CLR	PRE	OE	LE	D <sub>i</sub>	Q <sub>i</sub>	Y <sub>i</sub>	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

**NOTE:**

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

**FUNCTION TABLES <sup>(1)</sup>**  
**IDT54/74FCT842/44/46**

INPUTS					INTER- NAL	OUT- PUTS	FUNCTION
CLR	PRE	OE	LE	D <sub>i</sub>	Q <sub>i</sub>	Y <sub>i</sub>	
H	H	H	X	X	X	Z	High Z
H	H	H	H	H	L	Z	High Z
H	H	H	H	L	H	Z	High Z
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	H	L	L	Transparent
H	H	L	H	L	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

**NOTE:**

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, ↑ = LOW-to-HIGH Transition, Z = High Impedance

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**ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>**

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	100	100	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**CAPACITANCE** (T<sub>A</sub> = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER <sup>(1)</sup>	CONDITIONS	TYP.	MAX.	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

**NOTE:**

1. This parameter is guaranteed by characterization data and not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following conditions apply unless otherwise specified:

V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Commercial: T<sub>A</sub> = 0°C to +70°C; V<sub>CC</sub> = 5.0V ± 5%

Military: T<sub>A</sub> = -55°C to +125°C; V<sub>CC</sub> = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT	
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V	
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max.	V <sub>I</sub> = V <sub>CC</sub>	—	—	5	μA
I <sub>IL</sub>	Input LOW Current		V <sub>I</sub> = 2.7V	—	—	5 <sup>(4)</sup>	
			V <sub>I</sub> = 0.5V	—	—	-5 <sup>(4)</sup>	
			V <sub>I</sub> = GND	—	—	-5	
I <sub>oz</sub>	Off State (High Impedance) Output Current	V <sub>CC</sub> = Max.	V <sub>O</sub> = V <sub>CC</sub>	—	—	10	μA
			V <sub>O</sub> = 2.7V	—	—	10 <sup>(4)</sup>	
			V <sub>O</sub> = 0.5V	—	—	-10 <sup>(4)</sup>	
			V <sub>O</sub> = GND	—	—	-10	
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	—	-0.7	-1.2	V	
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-75	-120	—	mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32 μA	V <sub>HC</sub>	V <sub>CC</sub>	—	V	
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -300 μA	V <sub>HC</sub>	V <sub>CC</sub>		—
			I <sub>OH</sub> = -15mA MIL.	2.4	4.3		—
		I <sub>OH</sub> = -24mA COM'L.	2.4	4.3	—		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300 μA	—	GND	V <sub>LC</sub>	V	
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 300 μA	—	GND		V <sub>LC</sub>
			I <sub>OL</sub> = 32mA MIL.	—	0.3		0.5
		I <sub>OL</sub> = 48mA COM'L.	—	0.3	0.5		
V <sub>H</sub>	Input Hysteresis on Clock Only	—	—	200	—	mV	

**NOTES:**

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

**POWER SUPPLY CHARACTERISTICS**

$V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V$





SYMBOL	PARAMETER	TEST CONDITIONS <sup>(1)</sup>		MIN.	TYP. <sup>(2)</sup>	MAX.	UNIT
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}; V_{IN} \leq V_{LC}$ $f_i = 0$		—	0.001	1.5	mA
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2.0	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.5	4.0	mA
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	1.8	5.0	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	3.0	6.5 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5.0	14.5 <sup>(5)</sup>	

**NOTES:**

- For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient and maximum loading.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_I)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_H$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 $f_i$  = Input Frequency  
 $N_I$  = Number of Inputs at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PARAMETER	DESCRIPTION	TEST <sup>(1)</sup> CONDITIONS	IDT54/74FCT841A-46A				IDT54/74FCT841B-46B				UNIT
			COM'L		MIL.		COM'L		MIL.		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{PLH}$ (IDT54/74FCT841, 43, 45) $t_{PHL}$	Data ( $D_i$ ) to Output ( $Y_i$ ) (LE = HIGH)	$C_L = 50pF$ $R_L = 500\Omega$	-	9.5	-	11	-	6.5	-	7.5	ns
		$C_L = 300pF^{(3)}$ $R_L = 500\Omega$	-	13	-	15	-	13	-	15	ns
$t_{SU}$	Data to LE Set-up Time	$C_L = 50pF$ $R_L = 500\Omega$	2.5	-	2.5	-	2.5	-	2.5	-	ns
$t_H$	Data to LE Hold Time	$C_L = 50pF$ $R_L = 500\Omega$	2.5	-	3	-	2.5	-	2.5	-	ns
$t_{PLH}$ (IDT54/74FCT842, 44, 46) $t_{PHL}$	Data ( $D_i$ ) to Output ( $Y_i$ ) (LE = HIGH)	$C_L = 50pF$ $R_L = 500\Omega$	-	10	-	12	-	8.0	-	9.0	ns
		$C_L = 300pF^{(3)}$ $R_L = 500\Omega$	-	13	-	15	-	13	-	15	ns
$t_{SU}$	Data to LE Set-up Time	$C_L = 50pF$ $R_L = 500\Omega$	2.5	-	2.5	-	2.5	-	2.5	-	ns
$t_H$	Data to LE Hold Time	$C_L = 50pF$ $R_L = 500\Omega$	2.5	-	3	-	2.5	-	2.5	-	ns
$t_{PLH}$ $t_{PHL}$	Latch Enable (LE) to $Y_i$	$C_L = 50pF$ $R_L = 500\Omega$	-	12	-	16	-	8.0	-	10.5	ns
		$C_L = 300pF^{(3)}$ $R_L = 500\Omega$	-	16	-	20	-	15.5	-	18	ns
$t_{PLH}$	Propagation Delay, Preset to $Y_i$	$C_L = 50pF$ $R_L = 500\Omega$	-	12	-	14	-	8.0	-	10	ns
$t_{SU}$	Preset Recovery (PRE  ) Time		-	14	-	17	-	10	-	13	ns
$t_{PHL}$	Propagation Delay, Clear to $Y_i$		-	13	-	15	-	10	-	11	ns
$t_{SU}$	Clear Recovery (CLR  ) Time		-	14	-	17	-	10	-	10	ns
$t_{PWH}$	LE Pulse Width		HIGH	6	-	6	-	4	-	4	-
$t_{PWL}$	Preset Pulse Width	LOW	8	-	9	-	4	-	4	-	ns
$t_{PWL}$	Clear Pulse Width	LOW	8	-	9	-	4	-	4	-	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$  to $Y_i$	$C_L = 50pF$ $R_L = 500\Omega$	-	14	-	15	-	8	-	8.5	ns
		$C_L = 300pF^{(3)}$ $R_L = 500\Omega$	-	23	-	25	-	14	-	15	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time $\overline{OE}$  to $Y_i$	$C_L = 5pF^{(3)}$ $R_L = 500\Omega$	-	9	-	10	-	6	-	6.5	ns
		$C_L = 50pF$ $R_L = 500\Omega$	-	12	-	12	-	7.0	-	7.5	ns

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter guaranteed but not tested.

ORDERING INFORMATION

<u>IDTXXFCT</u> Temp. Range	<u>XXXX</u> Device Type	<u>X</u> Package	<u>X</u> Process		
				Blank	Commercial
				B	MIL-STD-883, Class B
				P	Plastic DIP
				D	CERDIP
				E	CERPACK
				L	Leadless Chip Carrier
				SO	Small Outline IC
				841A	10-Bit Non-inverting Latch
				842A	10-Bit Inverting Latch
				843A	9-Bit Non-inverting Latch
				844A	9-Bit Inverting Latch
				845A	8-Bit Non-inverting Latch
				846A	8-Bit Inverting Latch
841B	Fast 10-Bit Non-inverting Latch				
842B	Fast 10-Bit Inverting Latch				
843B	Fast 9-Bit Non-inverting Latch				
844B	Fast 9-Bit Inverting Latch				
845B	Fast 8-Bit Non-inverting Latch				
846B	Fast 8-Bit Inverting Latch				
54	-55°C to +125°C				
74	0°C to +70°C				