HARRIS SEMICONDUCTOR

CDP1852
CDP1852C

T-52-33-53

February 1992

Byte-Wide Input/Output Port

Features

- Static Silicon-Gate CMOS Circuitry
- Parallel 8 Bit Data Register and Buffer
- Handshaking Via Service Request Flip-Flop
- Low Quiescent and Operating Power
- Interfaces Directly with CDP1800-Series Microprocessors
- Single Voltage Supply
- Full Military Temperature Range (-55°C to +125°C)

Ordering Information

PACKAGE	TEMPERATURE RANGE	5V	10V
Plastic DIP	-40°C to +85°C	CDP1852CE	CDP1852E
Burn-in		CDP1852CEX	CDP1852EX
Ceramic DIP	-40°C to +85°C	CDP1852CD	CDP1852D
* 883B	-55°C to +125°C	CDP1852CD3	CDP1852D3

* Respective specifications are included at the end of this data sheet.

Description

The CDP1852 and CDP1852C are parallel, 8 bit, mode-programmable input/output ports. They are compatible and will interface directly with CDP1800-series microprocessors. They are also useful as 8 bit address latches when used with the CDP1800 multiplexed address bus and as I/O ports in general-purpose applications.

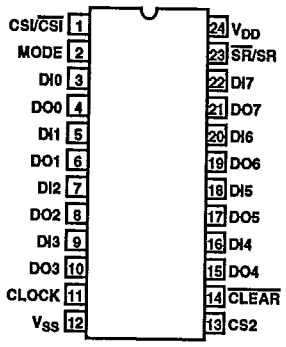
The mode control is used to program the device as an input port (mode = 0) or as an output port (mode = 1). The $\overline{SR}$/SR output can be used as a signal to indicate when data is ready to be transferred. In the input mode, a peripheral device can strobe data into the CDP1852, and microprocessor can read that data by device selection. In the output mode, a microprocessor strobes data into the CDP1852, and handshaking is established with a peripheral device when the CDP1852 is deselected.

In the input mode, data at the data-in terminals (D10-D17) is strobed into the port's 8 bit register by a high (1) level on the clock line. The negative high-to-low transition of the clock latches the data in the register and sets the service request output low ($\overline{SR}$/SR = 0). When CS1/$\overline{CS1}$ and CS2 are high (CS1/$\overline{CS1}$ and CS2 = 1), the 3-state output drivers are enabled and data in the 8-bit register appear at the data-out terminals (D00-D07). When either CS1/$\overline{CS1}$ or CS2 goes low (CS1/$\overline{CS1}$ or CS2 = 0), the data-out terminals are tristated and the service request output returns high ($\overline{SR}$/SR =1).

In the output mode, the output drivers are enabled at all times. Data at the data-in terminals (D10-D17) is strobed into the 8 bit register when CS1/$\overline{CS1}$ is low (CS1/$\overline{CS1}$ = 0) and CS2 and the clock are high (1), and are present at the data-out terminals (D00-D07). The negative high-to-low transition of the clock latches the data in the register. The $\overline{SR}$/SR output goes high ($\overline{SR}$/SR = 1) when the device is deselected (CS1/$\overline{CS1}$ = 1 or CS2 = 0) and returns low ($\overline{SR}$/SR = 0) on the following trailing edge of the clock.

Pinout

24-LEAD DIP
TOP VIEW



Typical CDP1802 Microprocessor System

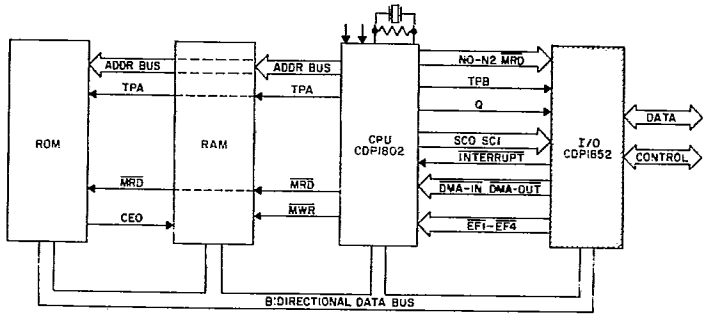


FIGURE 1.

4 CMOS PERIPHERALS

A $\overline{\text{CLEAR}}$ control is provided for resetting the port's register (D00-D07 = 0) and service request flip-flop (input mode: $\overline{SR}$/SR=1 and output mode: $\overline{SR}$/SR=0).

The CDP1852 is functionally identical to the CDP1852C. The CDP1852 has a recommended operating voltage range of 4 to 10.5 volts, and the CDP1852C has a recommended operating voltage range of 4 to 6.5 volts.

The CDP1852 and CDP1852C are supplied in 24-lead, hermetic, dual-in-line ceramic packages (D suffix), in 24-lead dual-in-line plastic packages (E suffix). The CDP1852C is also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} Terminal
CDP1852 ..... −0.5 to +11 V
CDP1852C ..... −0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = −55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, H ..... −55 to +125° C
PACKAGE TYPE E ..... −40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

RECOMMENDED OPERATING CONDITIONS at T_A = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1852		CDP1852C		
	Min.	Max.	Min.	Max.	
DC Operating Voltage Range	4	10.5	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	V_{SS}	V_{DD}	

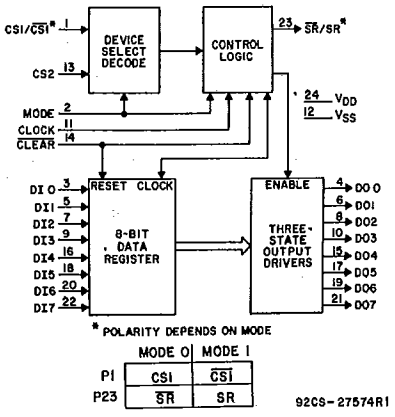


Fig. 2 - Block diagram of CDP1852.

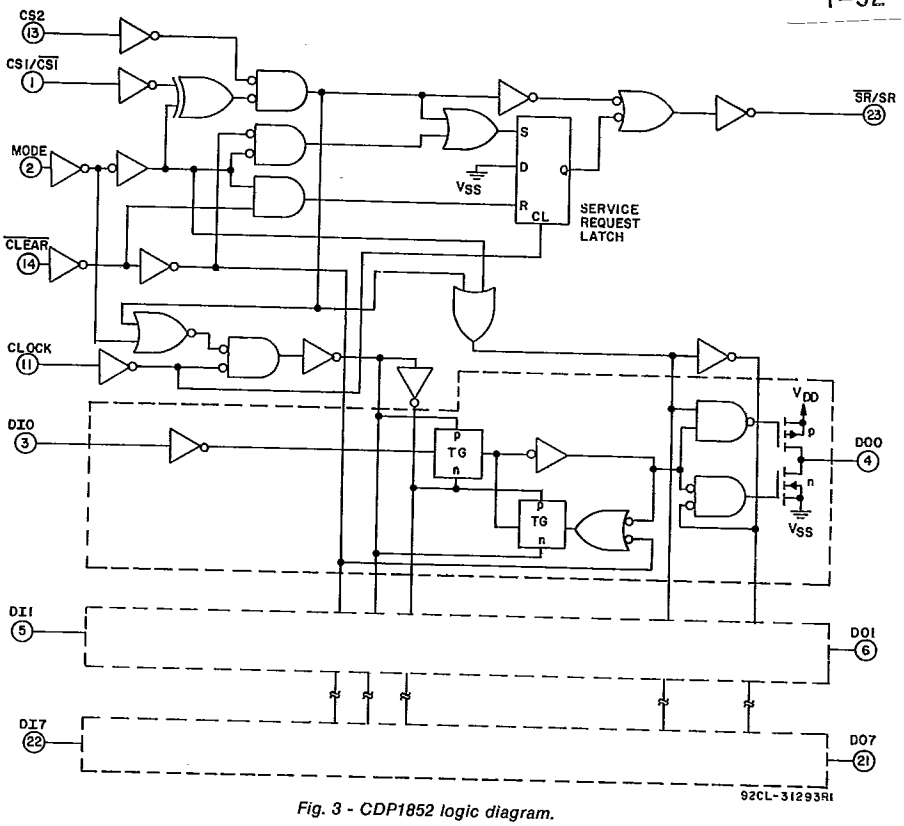


Fig. 3 - CDP1852 logic diagram.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852 Min.	CDP1852 Typ.*	CDP1852 Max.	CDP1852C Min.	CDP1852C Typ.*	CDP1852C Max.	
Quiescent Device Current, I_{DD}	—	0,5	5	—	—	10	—	—	50	μA
	—	0,10	10	—	—	100	—	—	—	
Output Low Drive (Sink) Current, I_{OL}	0.4	0,5	5	1.6	3.2	—	1.6	3.2	—	mA
	0.5	0,10	10	3	6	—	—	—	—	
Output High Drive (Source) Current, I_{OH}	4.6	0,5	5	−1.15	−2.3	—	−1.15	−2.3	—	
	9.5	0,10	10	−3	−6	—	—	—	—	
Output Voltage Low Level, V_{OL}†	—	0,5	5	—	0	0.1	—	0	0.1	V
	—	0,10	10	—	0	0.1	—	—	—	
Output Voltage High Level, V_{OH}	—	0,5	5	4.9	5	—	4.9	5	—	
	—	0,10	10	9.9	10	—	—	—	—	
Input Low Voltage, V_{IL}	0.5,4.5	—	5	—	—	1.5	—	—	1.5	
	0.5,9.5	—	10	—	—	3	—	—	—	
Input High Voltage, V_{IH}	0.5,4.5	—	5	3.5	—	—	3.5	—	—	
	0.5,9.5	—	10	7	—	—	—	—	—	

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$ (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS						UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	CDP1852			CDP1852C			
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input Current, I_{IN}	—	0,5	5	—	—	±1	—	—	±1	μA
	—	0,10	10	—	—	±2	—	—	—	
3-State Output Leakage Current, I_{OUT}	0,5	0,5	5	—	—	±1	—	—	±1	
	0,10	0,10	10	—	—	±2	—	—	—	
Operating Current, I_{DD1}‡	—	0,5	5	—	130	300	—	150	300	
	—	0,10	10	—	550	800	—	—	—	
Input Capacitance, C_{IN}	—	—	—	—	5	7.5	—	5	7.5	pF
Output Capacitance, C_{OUT}	—	—	—	—	5	7.5	—	—	—	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}.
†$I_{OL} = I_{OH} = 1$ μA.
‡Operating current is measured at 2 MHz in an CDP1802 system with open outputs and a program of 6N55, 6NAA, 6N55, 6NAA, -------.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} = \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, and 1 TTL Load

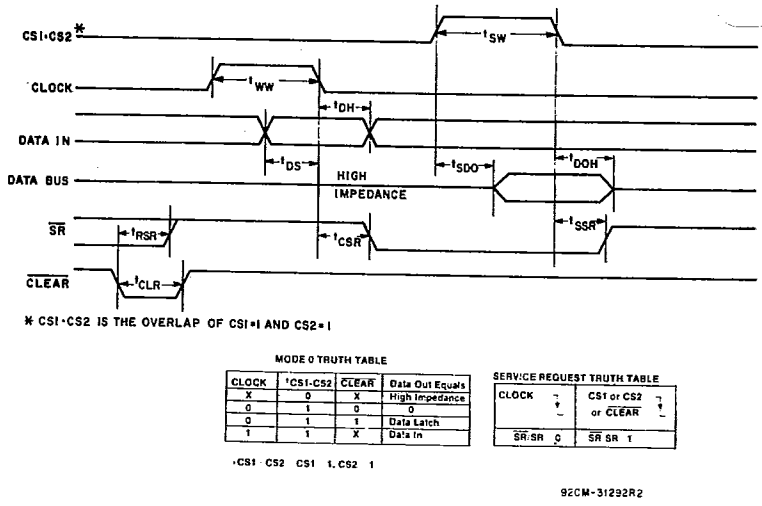
CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
MODE 0 — Input Port (Fig. 4)					
Minimum Select Pulse Width, t_{SW}	5	—	180	360	ns
	10	—	90	180	
Minimum Write Pulse Width, t_{WW}	5	—	90	180	
	10	—	45	90	
Minimum Clear Pulse Width, t_{CLR}	5	—	80	160	
	10	—	40	80	
Minimum Data Setup Time, t_{DS}	5	—	−10	0	
	10	—	−5	0	
Mininum Data Hold Time, t_{DH}	5	—	75	150	
	10	—	35	75	
Data Out Hold Time, t_{DOH}†	5	30	185	370	
	10	15	100	200	
Propagation Delay Times, t_{PLH}, t_{PHL}: Select to Data Out†, t_{SDO}	5	30	185	370	
	10	15	100	200	
Clear to SR, T_{RSR}	5	—	170	340	
	10	—	85	170	
Clock to SR, t_{CSR}	5	—	110	220	
	10	—	55	110	
Select to SR, t_{SSR}	5	—	120	240	
	10	—	60	120	

†Minimum value is measured from CS2, maximum value is measured from CS1/$\overline{CS1}$
*Typical values are for $T_A = 25°C$ and nominal V_{DD}.

INPUT PORT MODE 0 — TYPICAL OPERATION

General Operation

When the mode control is tied to VSS, the CDP1852 becomes an input port. In this mode, the peripheral device places data into the CDP1852 with a strobe pulse and the CDP1852 signals the microprocessor that data is ready to be transferred on the strobe's trailing edge via the $\overline{SR}$ output line. The CDP1802 then issues an input instruction that enables the CDP1852 to place the information from the peripheral device on the data bus to be entered into a memory location and the accumulator of the microprocessor.



MODE 0 TRUTH TABLE

CLOCK	tCS1-CS2	CLEAR	Data Out Equals
X	0	X	High Impedance
0	1	0	0
0	1	1	Data Latch
1	1	X	Data In

SERVICE REQUEST TRUTH TABLE

CLOCK	CS1 or CS2 or CLEAR
SR:SR 0	SR SR 1

•CS1 · CS2 CS1 1, CS2 1

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Fig. 4 - MODE 0 input port timing waveforms and truth tables.

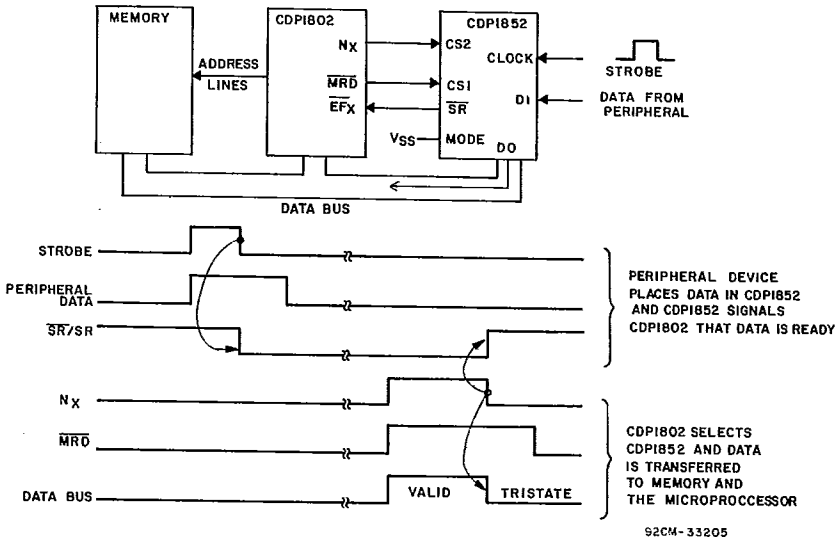

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Fig. 5 - Input port mode 0 functional diagram and waveforms - typical operation.

Detailed Operation (See Fig. 5)

The STROBE from the peripheral device places DATA into the 8-bit register of the CDP1852 when it goes high and latches the DATA on its trailing edge. The $\overline{SR}$ output is set low on the strobe's trailing edge. This output is connected to a flag line of the CDP1802 microprocessor and software polling will determine that the flag line has gone low and peripheral data is ready to be transferred. The CDP1802 then issues an input instruction that places an N_x line high. With the $\overline{MRD}$ line also high, the CDP1852 is selected and its output drivers place the DATA from the peripheral device on the DATA BUS. When the CDP1802 selected the CDP1852, it also selected and addressed the memory via one of the 16 internal address registers selected by an internal "X" register. The data from the CDP1852 is therefore entered into the memory [Bus → M(R(X))]. The data is also transferred to the D register (accumulator) in the microprocessor (Bus → D). When the CDP1802's execute cycle is completed, the CDP1852 is deselected by the N_X line returning low and its data output pins are tri-stated. The $\overline{SR}$ output returns high.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -40$ to $+85°C$, $V_{DD} = \pm 5\%$, t_r, $t_f = 20$ ns, $V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$, $C_L = 100$ pF, and 1 TTL Load

CHARACTERISTIC	V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.*	Max.	
MODE 1 — Output Port (Fig. 6)					
Minimum Clock Pulse Width, t_{CLK}	5	—	130	260	ns
	10	—	65	130	
Minimum Write Pulse Width, t_{WW}	5	—	130	260	
	10	—	65	130	
Minimum Clear Pulse Width, t_{CLR}	5	—	60	120	
	10	—	30	60	
Minimum Data Setup Time, t_{DS}	5	—	−10	0	
	10	—	−5	0	
Minimum Data Hold Time, t_{DH}	5	—	75	150	
	10	—	35	75	
Minimum Select-after-Clock Hold Time, t_{SH}	5	—	−10	0	
	10	—	−5	0	
Propagation Delay Times, t_{PLH}, t_{PHL}: Clear to Data Out, t_{RDO}	5	—	140	280	
	10	—	70	140	
Write to Data Out, t_{WDO}	5	—	220	440	
	10	—	110	220	
Data In to Data Out, t_{DDO}	5	—	100	200	
	10	—	50	100	
Clear to SR, t_{RSR}	5	—	120	240	
	10	—	60	120	
Clock to SR, t_{CSR}	5	—	120	240	
	10	—	60	120	
Select to SR, t_{SSR}	5	—	120	240	
	10	—	60	120	

*Typical values are for $T_A = 25°C$ and nominal V_{DD}.

OUTPUT PORT MODE 1 — TYPICAL OPERATION

General Operation

Connecting the mode control to V_{DD} configures the CDP1852 as an output port. The output drivers are always on in this mode, so any data in the 8-bit register will be present at the data-out lines when the CDP1852 is selected. The N line and MRD connections between the CDP1852 and CDP1802 remain the same as in the input mode configuration, but now the clock input of the CDP1852 is tied to the TPB output of the CDP1802 and the SR output of the CDP1852 will be used to signal the peripheral device that valid data is present on its input lines. The microprocessor issues an output instruction, and data from the memory is strobed into the CDP1852 with the TPB pulse. When the CDP1852 is deselected, the SR output goes high to signal the peripheral device.

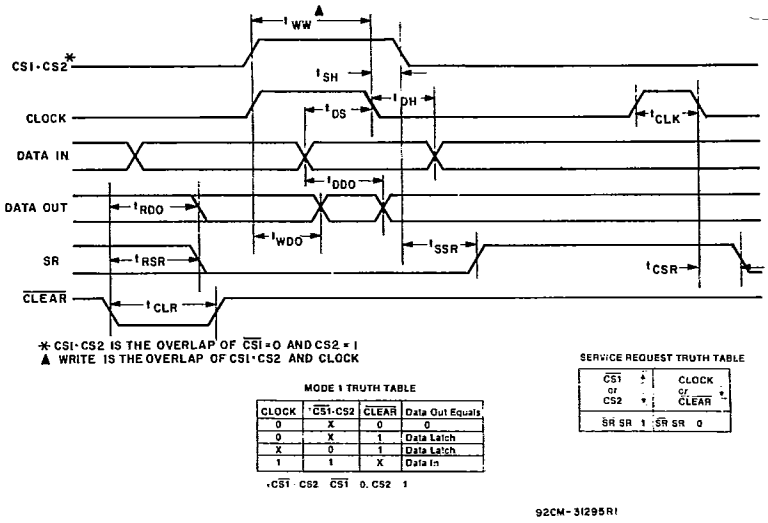

Fig. 6 - MODE 1 output port timing waveforms and truth tables.

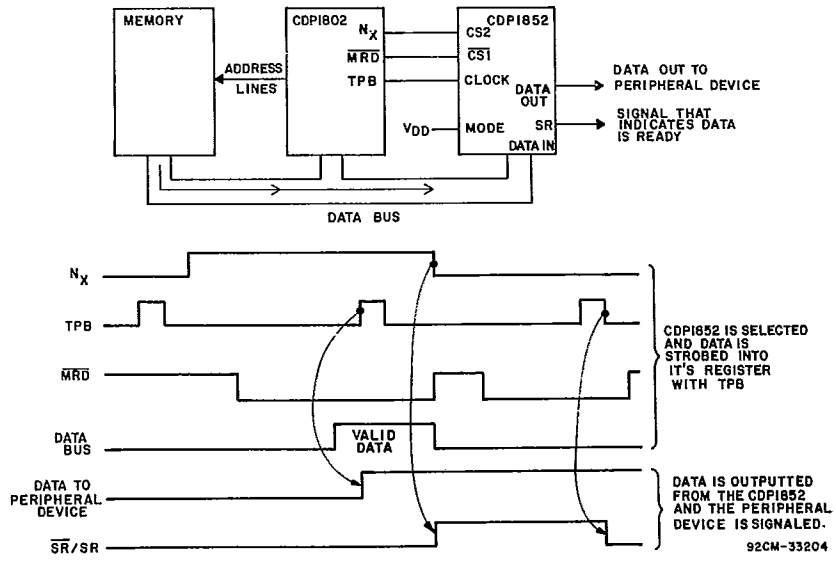

Fig. 7 - Output port mode 1 functional diagram and waveforms - typical operation.

Detailed Operation (See Fig. 7)

The CDP1802 issues an output instruction. The N_x line goes high and the $\overline{MRD}$ line goes low. The memory is accessed M(R(X)) → BUS and places data on the DATA BUS. This data are strobed into the 8-bit register of the CDP1852 when TPB goes high and latched on the TPB's trailing edge. The valid data thus appears on the CDP1852 output lines. When the CDP1802 output instruction cycle is complete, the N_x line goes low and the SR output goes high. SR will remain high until the trailing edge of the next TPB pulse, when it will return low.

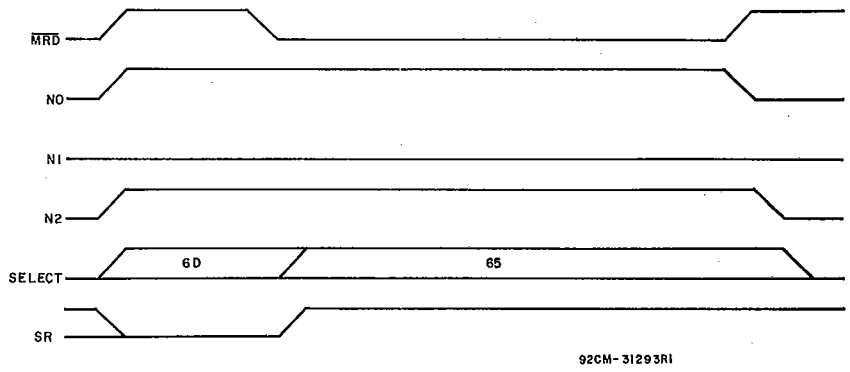

Fig. 8 - Execution of a "65" output instruction showing momentary selection of input port "D".

Application Information

In a CDP1800 series microprocessor-based system where $\overline{MRD}$ is used to distinguish between INP and OUT instructions, an INP instruction is assumed to occur at the beginning of every I/O cycle because $\overline{MRD}$ starts high. Therefore, at the start of an OUT instruction, which uses the same 3-bit N code as that used for selection of an input port, the input device is selected for a short time (see Fig. 8). This condition forces SR low and sets the internal SR latch (see Fig. 3). In a small system with unique N codes for inputs and outputs, this situation does not arise. Using the CDP1853 N-bit decoder or equivalent logic to decode the N lines after TPA prevents dual selection in larger systems (see Fig. 9 and Fig. 10).

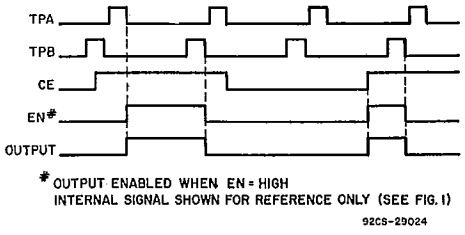

Fig. 9 - CDP1853 timing waveforms.

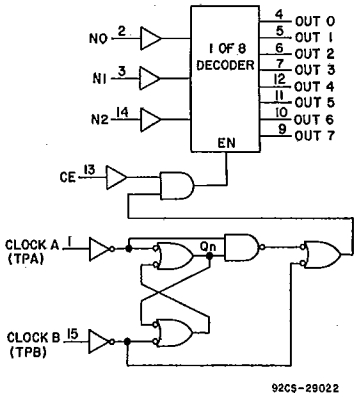

Fig. 10 - CDP1853 functional diagram.