National Semiconductor

April 1993

54AC/74AC161 • 54ACT/74ACT161
Synchronous Presettable Binary Counter

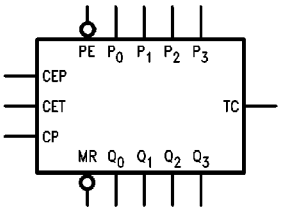
General Description

The 'AC/'ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

Features

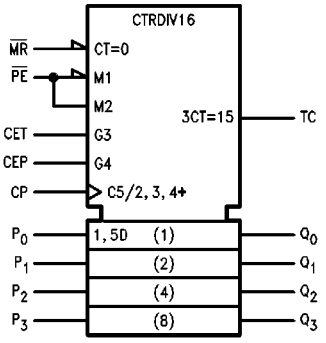
- I_{CC} reduced by 50%
- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT161 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - — 'AC161: 5962-89561
  - — 'ACT161: 5962-89848

Logic Symbols



TL/F/9931–1

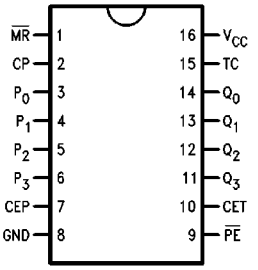
IEEE/IEC



TL/F/9931–2

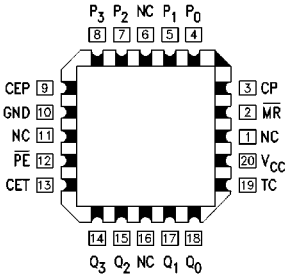
Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9931–3

Pin Assignment for LCC



TL/F/9931–4

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$	Asynchronous Master Reset Input
P_0–P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Inputs
Q_0–Q_3	Flip-Flop Outputs
TC	Terminal Count Output

TRI-STATE® is a registered trademark of National Semiconductor Corporation.
FACT™ is a trademark of National Semiconductor Corporation.

RRD-B30M75/Printed in U. S. A.

Functional Description

The 'AC/'ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs—Master Reset, Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 use D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative $\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in *Figure 2* are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

Logic Equations: Count Enable = CEP • CET • $\overline{PE}$

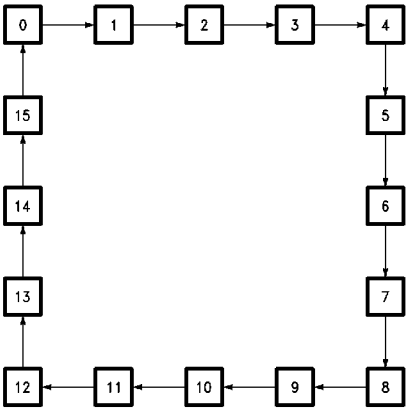
$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

Mode Select Table

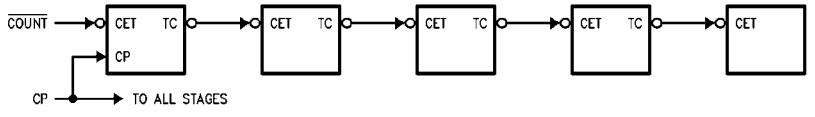
$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐‾)
X	X	X	Reset (Clear)
L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	Count (Increment)
H	L	X	No Change (Hold)
H	X	L	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram

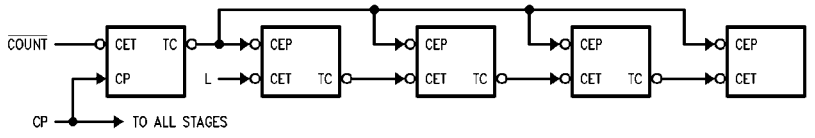


TL/F/9931–5



TL/F/9931–8

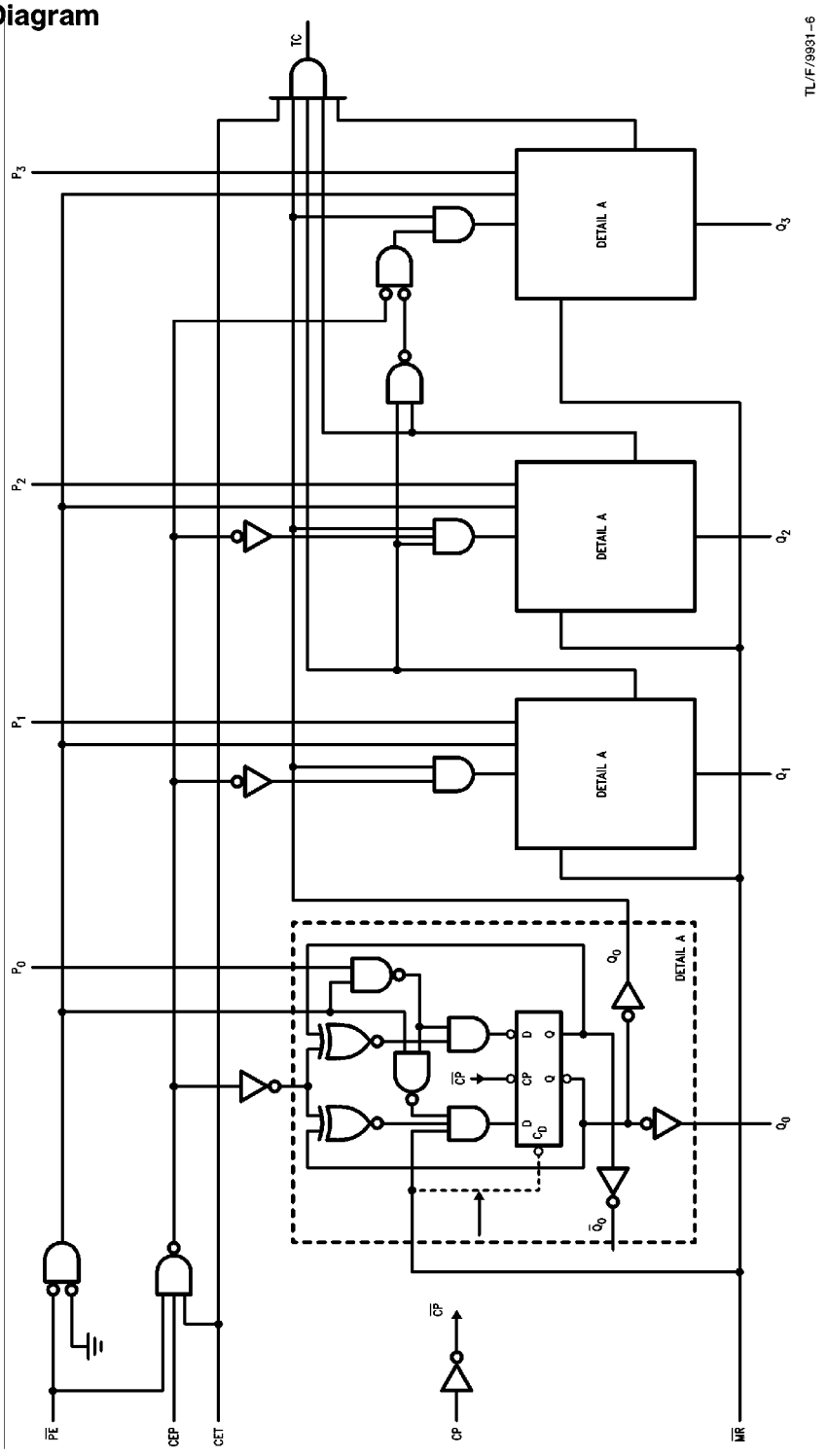
FIGURE 1. Multistage Counter with Ripple Carry



TL/F/9931–9

FIGURE 2. Multistage Counter with Lookahead Carry

Block Diagram



TL/F/9931–6

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74AC/ACT	−40°C to +85°C
54AC/ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V_{IN} from 30% to 70% of V_{CC} V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C	54AC T_A = −55°C to +125°C	74AC T_A = −40°C to +85°C	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9	V	I_{OUT} = −50 μA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.4	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −12 mA
		4.5		3.86	3.7		I_{OH} −24 mA
		5.5		4.86	4.7		−24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 μA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.5	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 12 mA
		4.5		0.36	0.5		I_{OL} 24 mA
		5.5		0.36	0.5		24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND

*All outputs loaded; thresholds on input associated with output under test.

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	74AC $T_A = +25°C$		54AC $T_A = -55°C$ to $+125°C$	74AC $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$		54ACT $T_A = -55°C$ to $+125°C$	74ACT $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5		3.86 4.86	3.70 4.70	3.76 4.76	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5		0.36 0.36	0.50 0.50	0.44 0.44	V	*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	±1.0	μA	$V_I = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	†Minimum Dynamic Output Current	5.5			50	75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−50	−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	80.0	40.0	μA	$V_{IN} = V_{CC}$ or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	111 167		55 80		60 95		MHz
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	2.0 1.5	7.0 5.0	12 9.0	1.0 1.0	14.0 10.0	1.5 1.0	13.5 9.5	ns
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.5 1.5	7.0 5.0	12 9.5	1.0 1.0	14.0 10.0	1.5 1.5	13 10	ns
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	3.0 2.0	9 6	15 10.5	3.0 3.0	18.5 13.0	2.5 1.5	16.5 11.5	ns
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	3.5 2.0	8.5 6.5	14 11	1.0 1.0	17.5 13.0	2.5 2.0	15.5 11.5	ns
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	2.0 1.5	5.5 3.5	9.5 6.5	1.0 1.0	13.0 8.5	1.5 1.0	11 7.5	ns
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	2.5 2.0	6.5 5	11 8.5	1.0 1.0	13.5 10.5	2.0 1.5	12.5 9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	2.0 1.5	6.5 5.5	12 9.5	1.0 1.0	14.5 10.5	1.5 1.5	13.5 10	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0	3.5 2.5	10 8.5	15 13	1.0 1.0	18.5 14.0	3.0 2.5	17.5 13.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	6.0 3.5	13.5 8.5	16.0 10.5	16 10.5	ns
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −4.0	−1 0	0.5 1.5	−0.5 0	ns
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	6.5 4.0	11.5 7.5	15.0 10.5	14 8.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−6.0 −3.5	0 0.5	−1.0 0.0	0 1	ns
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.0 2.0	6.0 4.5	7.5 5.5	7 5	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−3.5 −2	0 0	2.0 2.0	0 0.5	ns
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	2.0 2.0	3.5 2.5	5.0 5.0	4 3	ns
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	2.0 2.0	4.0 3.0	5.0 5.0	4.5 3.5	ns
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	3.0 2.5	5.5 4.5	5.0 5.0	7.5 6.0	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP		−2 −1	−0.5 0	1.5 2.0	0 0.5	ns

*Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	5.0	115	125		85		100		MHz
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	5.5	9.5	1.0	10.5	1.5	10.5	ns
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.5	6.0	10.5	1.0	10.5	1.5	11.5	ns
t_{PLH}	Propagation Delay CP to TC	5.0	2.0	7.0	11.0	1.0	14.0	1.5	12.5	ns
t_{PHL}	Propagation Delay CP to TC	5.0	1.5	8.0	12.5	1.0	12.5	1.5	13.5	ns
t_{PLH}	Propagation Delay CET to TC	5.0	1.5	5.5	8.5	1.0	9.5	1.5	10.0	ns
t_{PHL}	Propagation Delay CET to TC	5.0	1.5	6.5	9.5	1.0	9.5	1.5	10.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.5	6.0	10.0	1.0	10.0	1.5	11.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	2.5	8.0	13.5	1.0	11.5	2.0	14.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	9.5	13.0	11.5	ns
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0	0	0	ns
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5	11.0	9.5	ns
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5	0	−0.5	ns
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5	7.0	6.5	ns
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0	0.5	0	ns
t_w	Clock Pulse Width, (Load) HIGH or LOW	5.0	2.0	3.0	5.0	3.5	ns
t_w	Clock Pulse Width, (Count) HIGH or LOW	5.0	2.0	3.0	5.0	3.5	ns
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0	6.5	7.5	ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0	0.5	0.5	ns

*Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	45.0	pF	V_{CC} = 5.0V

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74AC 161 P C QR

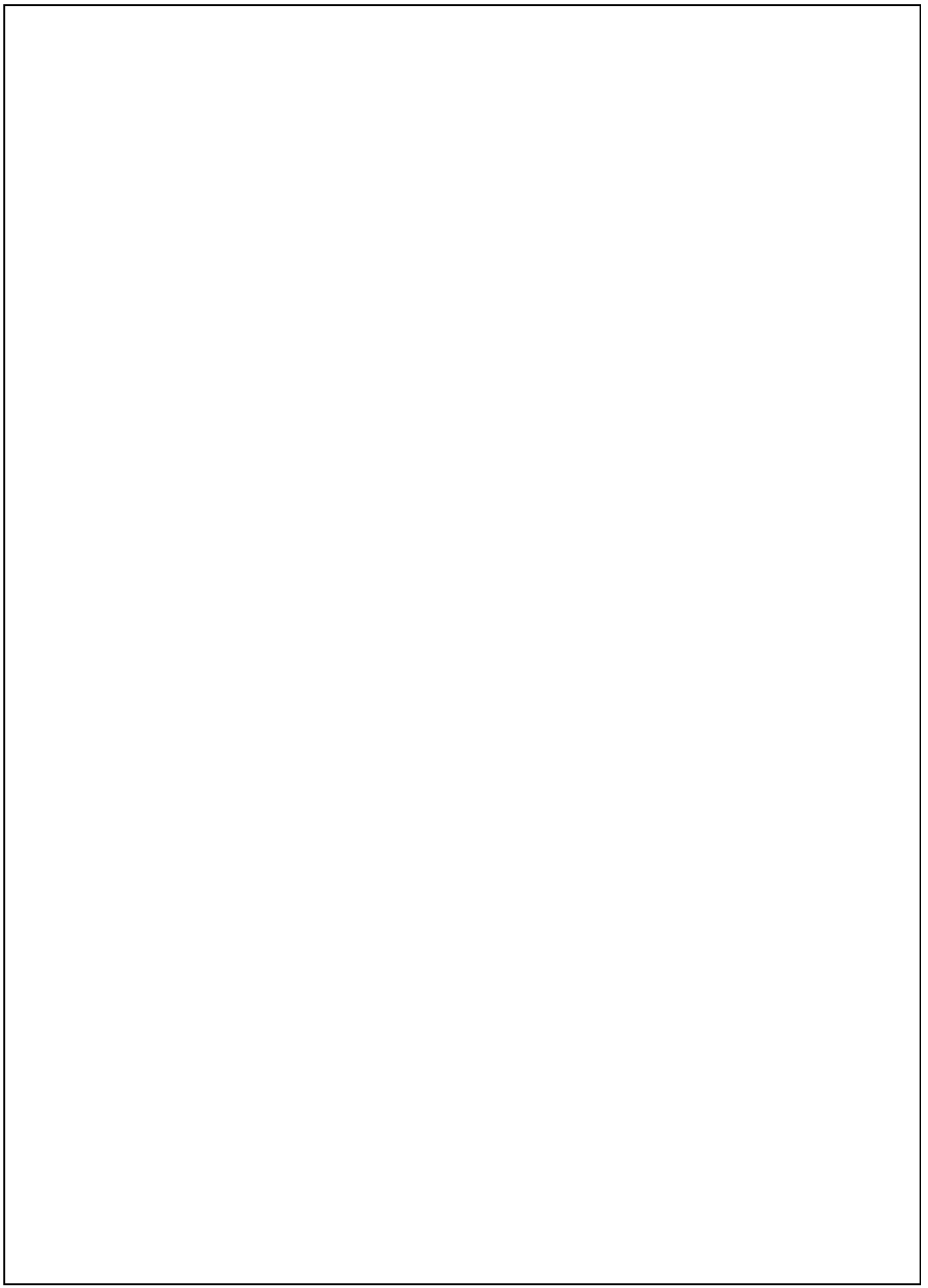
Temperature Range Family
- 74AC = Commercial
- 54AC = Military
- 74ACT = Commercial TTL-Compatible
- 54ACT = Military TTL-Compatible

Device Type

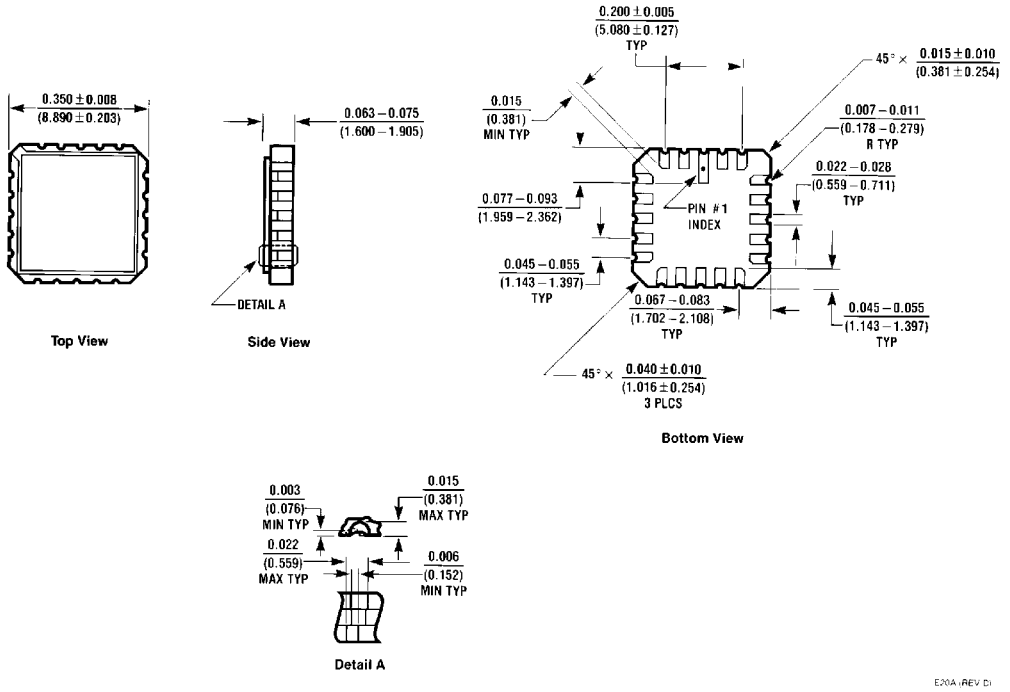
Package Code
- P = Plastic DIP
- D = Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- S = Small Outline (SOIC)

Temperature Range
- C = Commercial (−40°C to +85°C)
- M = Military (−55°C to +125°C)

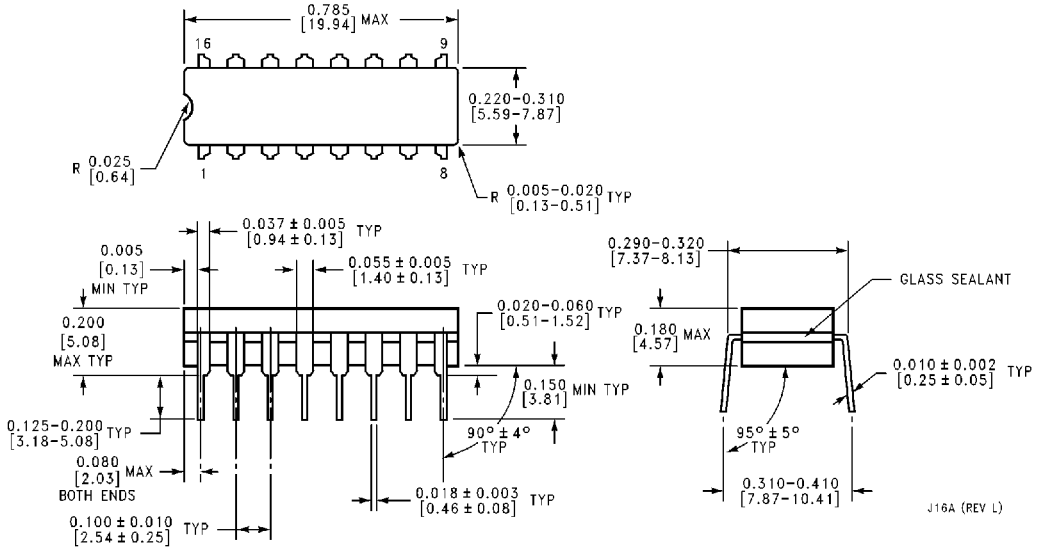
Special Variations
- X = Devices shipped in 13″ reels
- QR = Commercial grade device with burn-in
- QB = Military grade device with environmental and burn-in processing shipped in tubes



Physical Dimensions inches (millimeters)

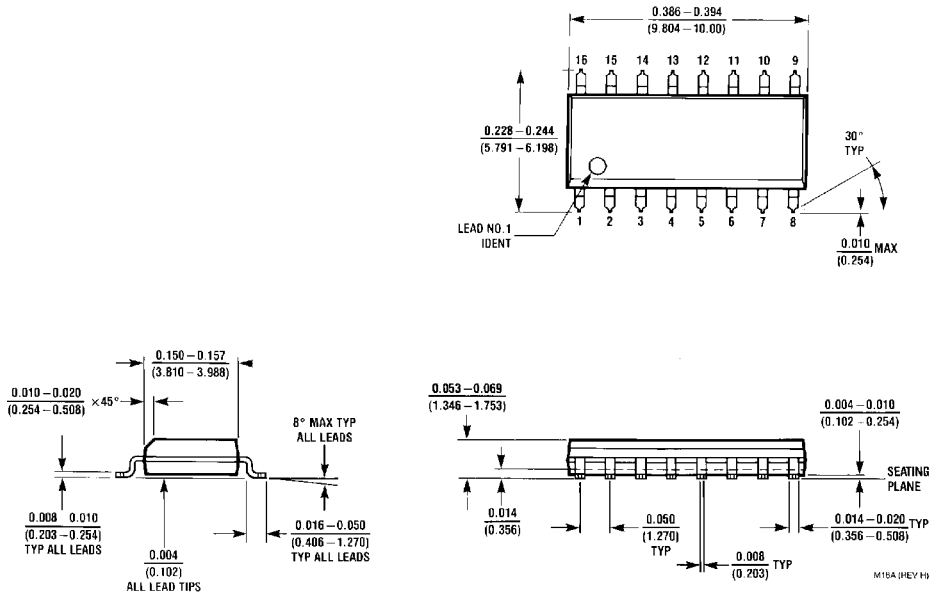


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

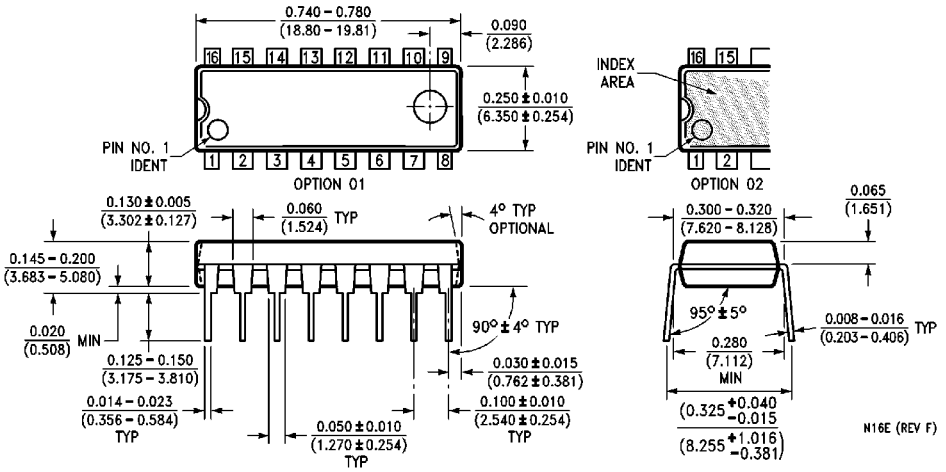


16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

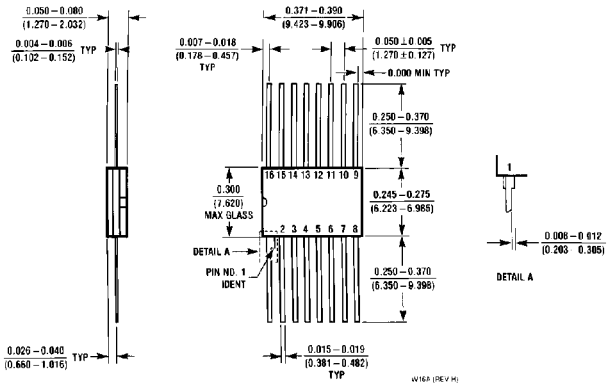


16 Lead Small Outline Integrated Circuit (S)
NS Package Number M16A



16 Lead Plastic Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16 Lead Ceramic Flatpak (F)
NS Package Number W16A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998