20 V, 200 mA, Low Noise, CMOS LDO

Preliminary Technical Data

ADP7118

FEATURES

Low Noise: 11 µVRMS independent of fixed output voltage
PSRR of 83 dB @ 10 KHz, 68 dB @ 100 KHz, 50 dB @ 1 MHz, V_{OUT} ≤5V, V_{IN} = 7V
Input voltage range: 2.7 V to 20 V
Maximum output current: 200 mA
Low dropout voltage: 200 mV @ 200 mA load, V_{OUT} = 5V
Initial accuracy: ±1%
Accuracy over line, load, and temperature: ±2%
User programmable Soft Start (LFCSP and SOIC only)
Low Quiescent Current, I_{GND} = 50 µA with no load
Low shutdown current: 1.5 µA @ V_{IN} = 5 V, 3µA @ V_{IN} = 40 V
Stable with small 2.2µF ceramic output capacitor
16 fixed output voltage options: 1.2V to 5.0V
Adjustable output from 1.2 V to V_{IN} - V_{DO}
Output may be adjusted above initial set point
Precision Enable
2x2mm, 6-lead LFCSP package, 8-Lead SOIC, 5-Lead TSOT

APPLICATIONS

Regulation to noise sensitive applications: ADC, DAC circuits, Precision amplifiers, Power for VCO Vtune control

Communications and Infrastructure

Medical and Healthcare

Industrial and Instrumentation

TYPICAL APPLICATION CIRCUITS

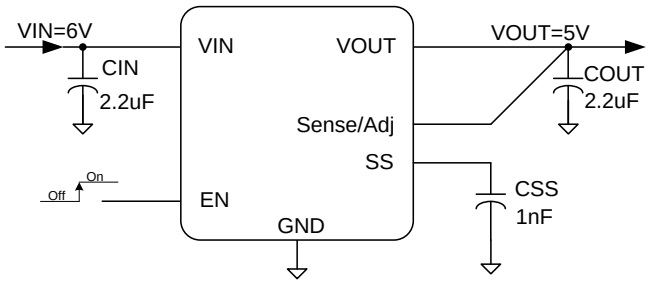

Figure 1. ADP7118 with Fixed Output Voltage, 5 V

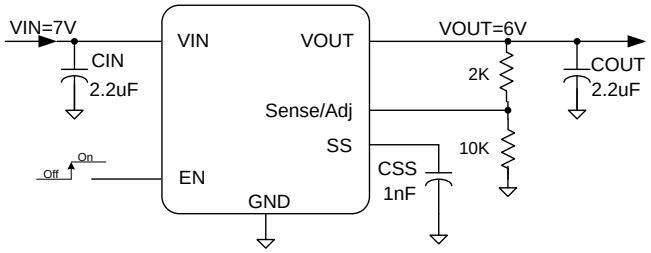

Figure 2. ADP7118 with 5V Output Adjusted to 6 V

GENERAL DESCRIPTION

The ADP7118 is a CMOS, low dropout linear regulator that operates from 2.7 V to 20 V and provide up to 200 mA of output current. These high input voltage LDOs are ideal for regulation of high performance analog and mixed signal circuits operating from 40 V down to 1.2 V rails. Using an advanced proprietary architecture, they provide high power supply rejection, low noise, and achieve excellent line and load transient response with just a small 2.2 µF ceramic output capacitor.

The ADP7118 is available in 16 fixed output voltage options. Each fixed output voltage may be adjusted above the initial set point with an external feedback divider. This allows the ADP7118 to provide an output voltage from 1.2 V to VOUT - V_{DO} with high PSRR and low noise.

User programmable soft start with an external capacitor is available in the LFCSP and SOIC packages.

The ADP7118 regulator output noise is 11 µVrms independent of the output voltage for the fixed options of 5V or less. The ADP7118 is available in a 6-lead, 2 mm × 2 mm LFCSP making them not only very compact solutions, but also providing excellent thermal performance for applications requiring up to 200 mA of output current in a small, low-profile footprint. The ADP7118 is also available in a 5-lead TSOT and an 8-lead SOIC.

Rev. PrD

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SPECIFICATIONS

V_{IN} = V_{OUT} +1 V or 2.7 V, whichever is greater, V_{OUT} = 5V, EN= V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, C_{SS} = 0pF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.7		20	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		50	140	µA
		I_{OUT} = 10 mA		80	200	µA
		I_{OUT} = 200 mA		180	320	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		1.8		µA
		EN = GND, T_J = −40°C to +85°C			10	µA
OUTPUT VOLTAGE ACCURACY						
Output Voltage Accuracy	V_{OUT}	I_{OUT} = 10 mA	−1		+1	%
		100 µA< I_{OUT} < 200 mA V_{IN} = (VOUT + 1V) to 40 V	−2		+2	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (VOUT + 1V) to 40 V	−0.01		+0.01	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 200 mA		0.002	0.005	%/mA
SENSE INPUT BIAS CURRENT	$SENSE_{I-BIAS}$	100 µA< IOUT < 200 mA V_{IN} = (VOUT + 1V) to 40 V		10	1000	nA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10 mA		30	60	mV
		I_{OUT} = 200 mA		200	450	mV
START-UP TIME[3]	$T_{START-UP}$	V_{OUT} = 5 V		380		µs
SOFT-START SOURCE CURRENT	$SS_{I-SOURCE}$	SS = GND		1.2		µA
CURRENT LIMIT THRESHOLD[4]	I_{LIMIT}		220	400	600	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage Rising	$UVLO_{RISE}$				2.69	V
Input Voltage Falling	$UVLO_{FALL}$		2.2			V
Hysteresis	$UVLO_{HYS}$			180		mV
EN INPUT STANDBY		2.7 V ≤ VIN ≤ 40 V				
EN Input Logic High	$EN_{STBY-HIGH}$		1.0			V
EN Input Logic Low	$EN_{STBY-LOW}$				0.4	V
EN Input Logic Hysteresis	$EN_{STBY-HYS}$			200		mV
EN INPUT PRECISION		2.7 V ≤ VIN ≤ 40 V				
EN Input Logic High	EN_{HIGH}		1.16	1.22	1.28	V
EN Input Logic Low	EN_{LOW}		1.07	1.13	1.18	V
EN Input Logic Hysteresis	EN_{HYS}			100		mV
EN Input Leakage Current	I_{EN-LKG}	EN = V_{IN} or GND		0.04	1	µA
EN Input Delay Time	TI_{EN-DLY}	From EN rising from 0V to V_{IN} to 0.1×V_{OUT}		80		µs
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, All output voltage options		11		µVrms
POWER SUPPLY REJECTION RATIO	PSRR	1 MHz, V_{IN} = 7V, V_{OUT} = 5V		50		dB
		100 KHz, V_{IN} = 7V, V_{OUT} = 5V		68		dB
		10 KHz, V_{IN} = 7V, V_{OUT} = 5V		88		dB

[1] Based on an end-point calculation using 100 µA and 200 mA loads. See **Figure 7** for typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages above 2.7 V.
[3] Start-up time is defined as the time between the rising edge of EN to OUT being at 90% of its nominal value.
[4] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V, or 4.5 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Minimum Input and Output Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	1.5			µF
Capacitor ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		0.3	Ω

[1] The minimum input and output capacitance should be greater than 1.5 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	–0.3 V to +44 V
VOUT to GND	–0.3 V to VIN
EN to GND	–0.3 V to VIN
SENSE to GND	–0.3 V to 6V
SS to GND	–0.3 V to VIN or 6V (whichever is less)
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Operating Ambient Temperature Range	–40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7118 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 in. × 3 in. circuit ™board. See JESD51-7 and JESD51-9 for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} , θ_{JC} , and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
6-Lead LFCSP	72.1	42.3	47.1	°C/W
8-Lead SOIC	52.7	41.5	32.7	°C/W
5-Lead TSOT	170	n/a	43	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

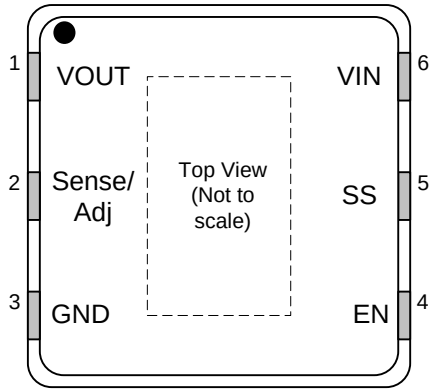


Figure 3. LFCSP Package

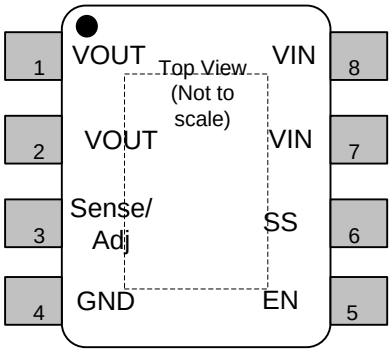


Figure 5. SOIC Package

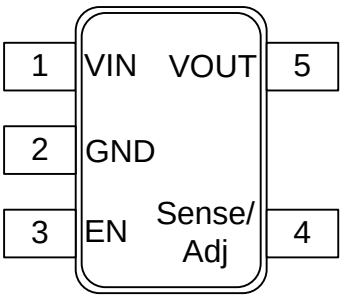


Figure 4. TSOT Package

Table 4. Pin Function Descriptions

LFCSP	Mnemonic	Description
1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
2	SENSE/ADJ	Sense input. Connect to load. An external resistor divider may also be used to set the output voltage higher than the fixed output voltage
3	GND	Ground.
4	EN	Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
5	SS	Soft Start. An external capacitor connected to this pin determines the soft-start time. This pin may be left open for a typical 320 µS start up time. DO NOT ground this pin.
6	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
EP	EP	Exposed pad on the bottom of the package. EP enhances thermal performance and is electrically connected to GND inside the package. It is recommended that the EP connect to the ground plane on the board.
SOIC	**Mnemonic**	**Description**
1	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
2	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
3	SENSE/ADJ	Sense input. Connect to load. An external resistor divider may also be used to set the output voltage higher than the fixed output voltage
4	GND	Ground.
5	EN	Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
6	SS	Soft Start. An external capacitor connected to this pin determines the soft-start time. This pin may be left open for a typical 320 µS start up time. DO NOT ground this pin.
7	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
8	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.

SOIC	Mnemonic	Description
EP	EP	Exposed pad on the bottom of the package. EP enhances thermal performance and is electrically connected to GND inside the package. It is recommended that the EP connect to the ground plane on the board.

TSOT	Mnemonic	Description
1	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
2	GND	Ground.
3	EN	Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
4	SENSE/ADJ	Sense input. Connect to load. An external resistor divider may also be used to set the output voltage higher than the fixed output voltage
5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 7.5 V, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

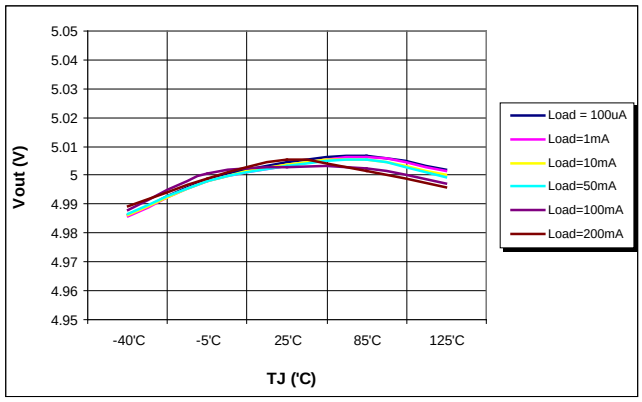


Figure 6. Output Voltage vs. Junction Temperature

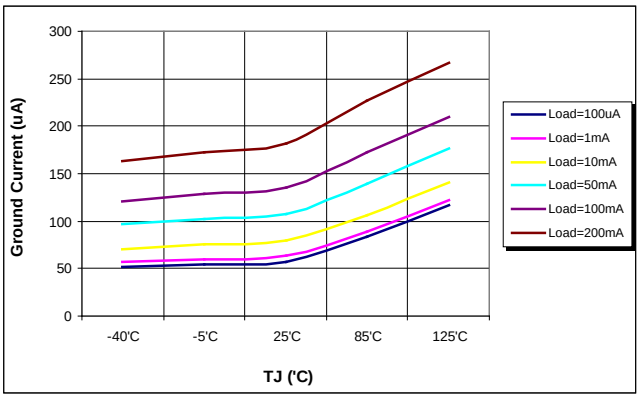


Figure 9. Ground Current vs. Junction Temperature

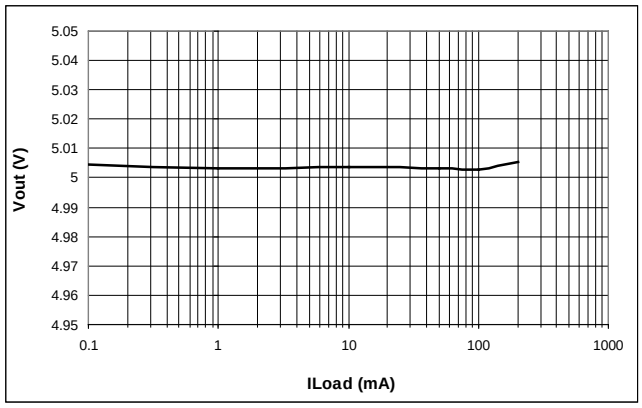


Figure 7. Output Voltage vs. Load Current

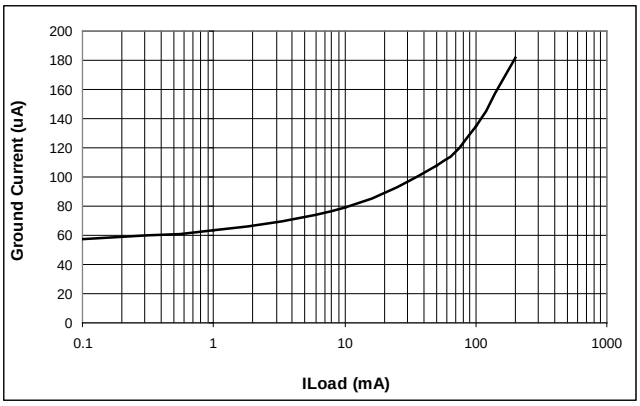


Figure 10. Ground Current vs. Load Current

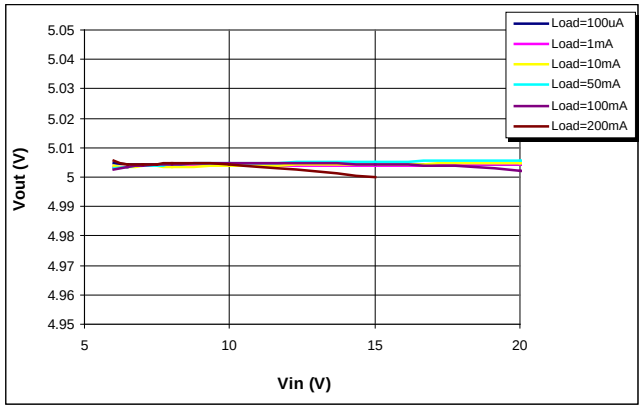


Figure 8. Output Voltage vs. Input Voltage

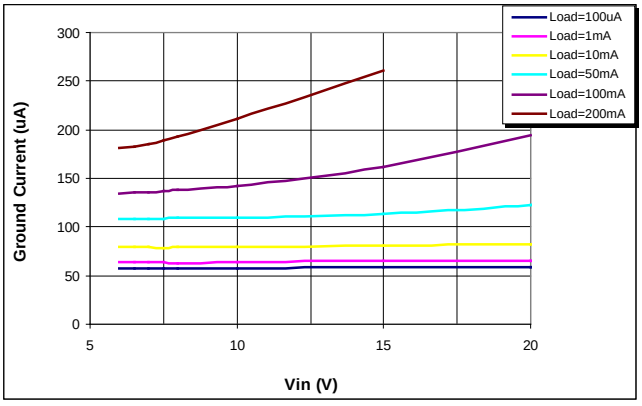


Figure 11. Ground Current vs. Input Voltage

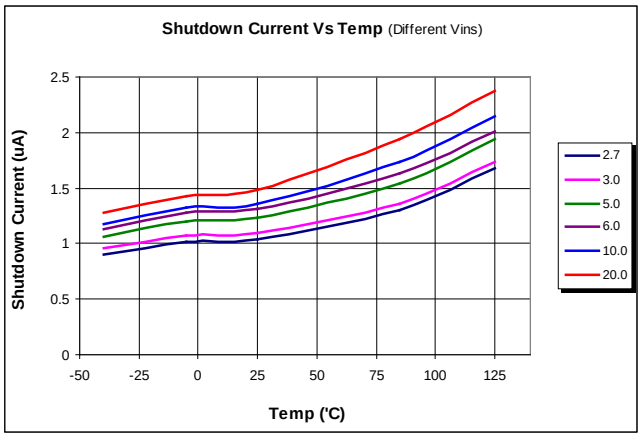


Figure 12. Shutdown Current vs. Temperature at Various Input Voltages

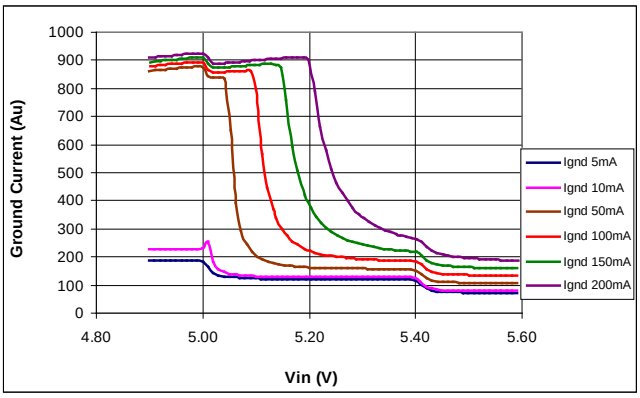


Figure 15. Ground Current vs. Input Voltage (in Dropout) , V_{OUT} = 5 V

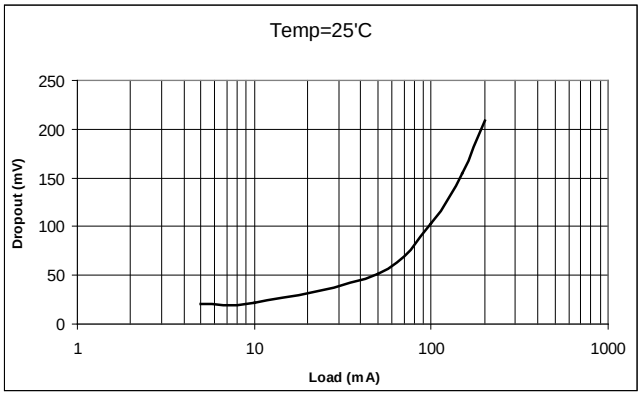


Figure 13. Dropout Voltage vs. Load Current, V_{OUT} = 5 V

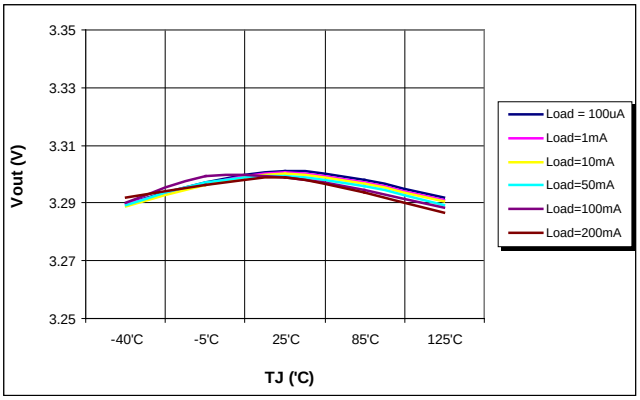


Figure 16. Output Voltage vs. Junction Temperature, V_{OUT} = 3.3 V

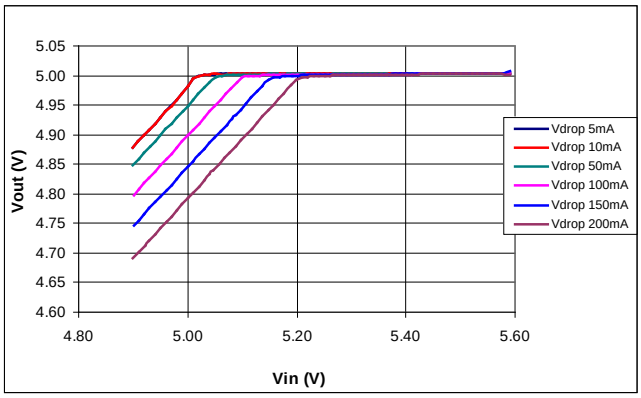


Figure 14. Output Voltage vs. Input Voltage (in Dropout) , V_{OUT} = 5 V

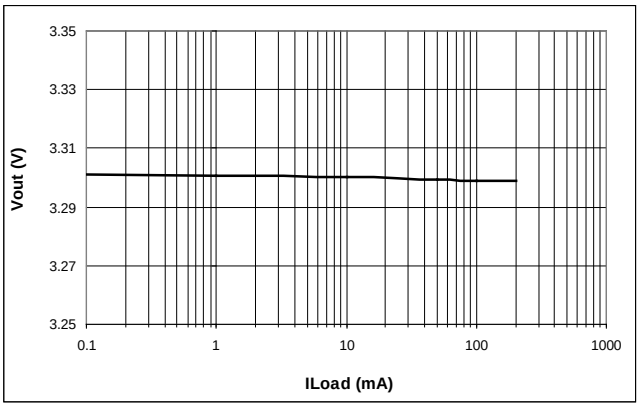


Figure 17. Output Voltage vs. Load Current, V_{OUT} = 3.3 V

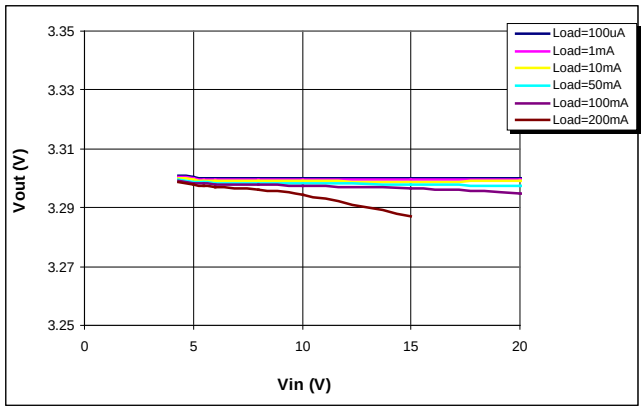


Figure 18. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V

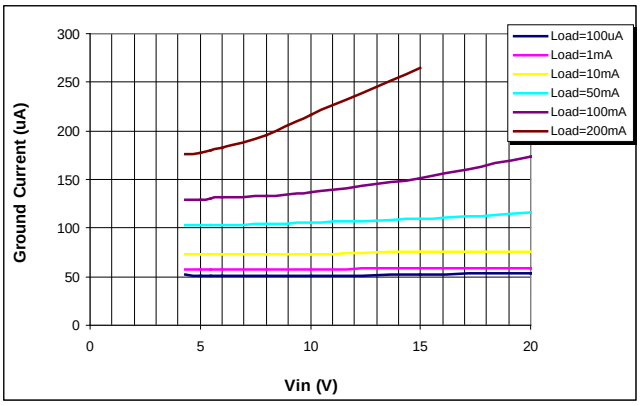


Figure 21. Ground Current vs. Input Voltage, V_{OUT} = 3.3 V

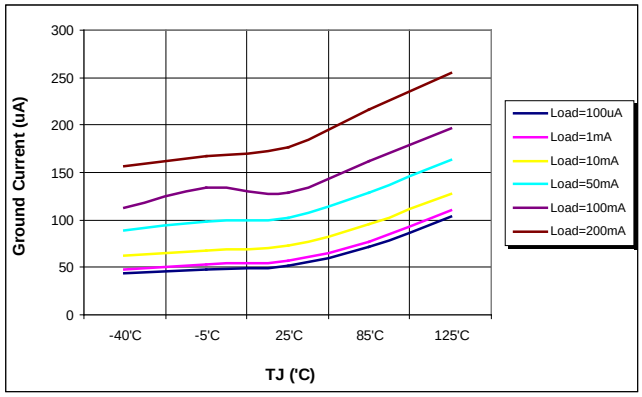


Figure 19. Ground Current vs. Junction Temperature, V_{OUT} = 3.3 V

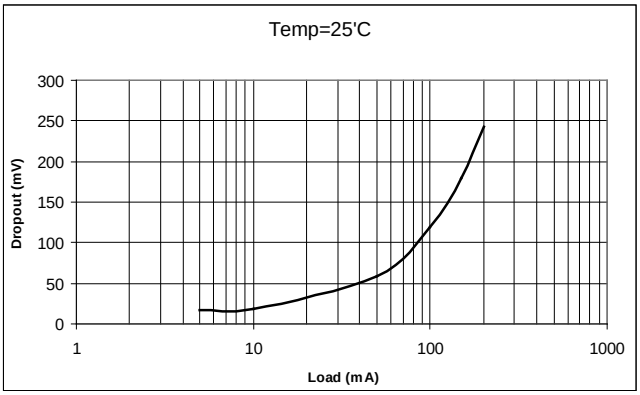


Figure 22. Dropout Voltage vs. Load Current, V_{OUT} = 3.3 V

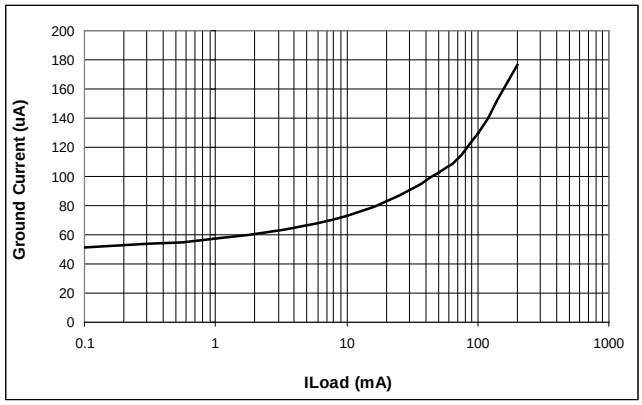


Figure 20. Ground Current vs. Load Current, V_{OUT} = 3.3 V

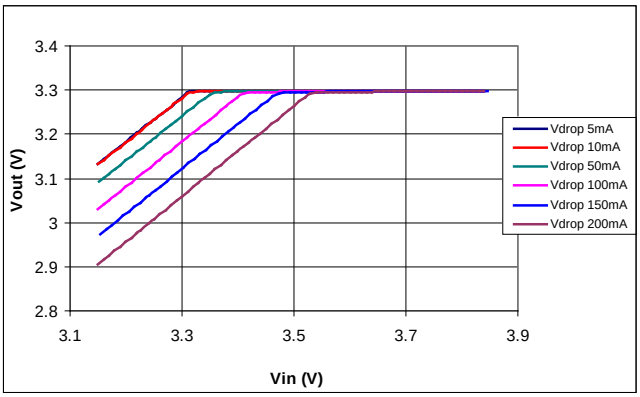


Figure 23. Output Voltage vs. Input Voltage (in Dropout) , V_{OUT} = 3.3 V

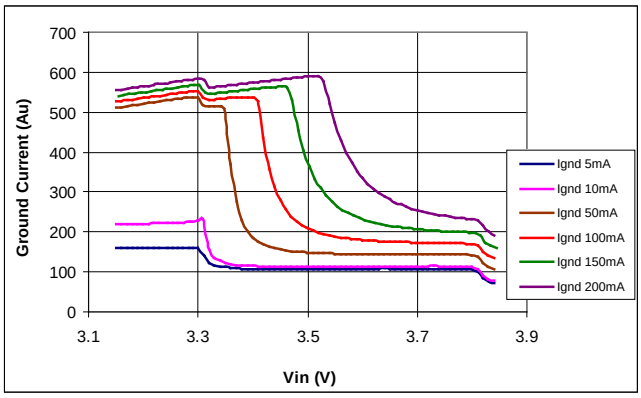


Figure 24. Ground Current vs. Input Voltage (in Dropout) , V_{OUT} = 3.3 V

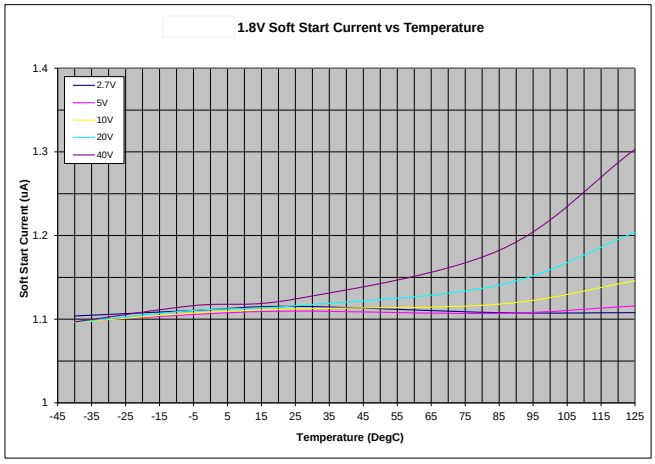


Figure 25. Soft Start Current vs. Temperature, Different Input Voltage, V_{OUT} = 5 V

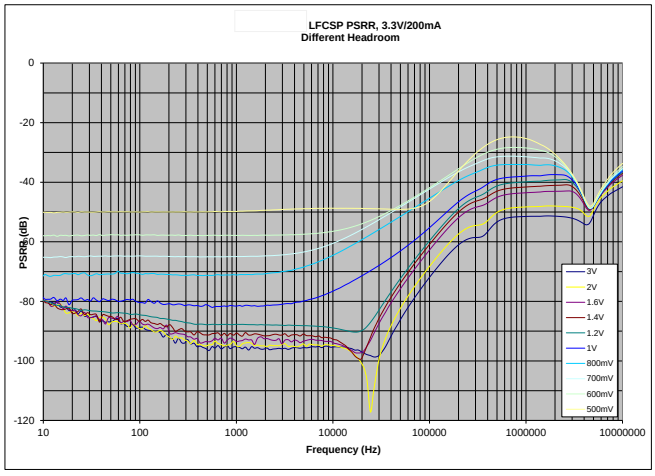


Figure 26. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 3.3 V, Various Headroom voltage

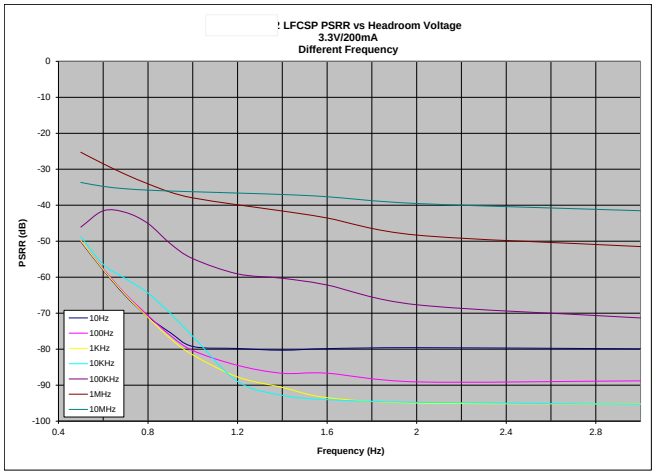


Figure 27. Power Supply Rejection Ratio vs. Headroom, V_{OUT} = 3.3V, Different Frequencies

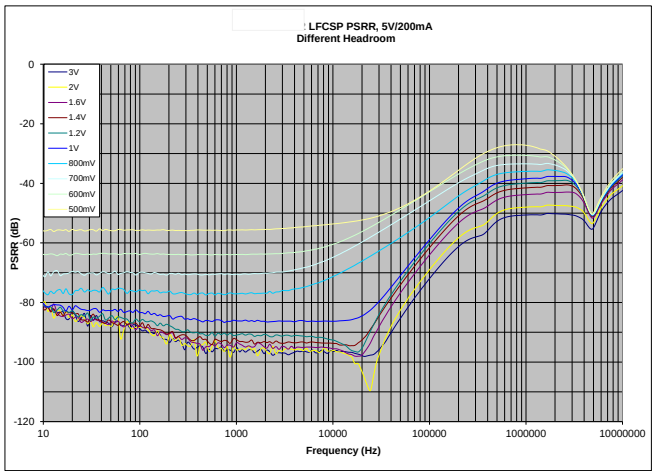


Figure 28. Power Supply Rejection Ratio vs. Frequency, V_{OUT} = 5 V, Various Headroom voltage

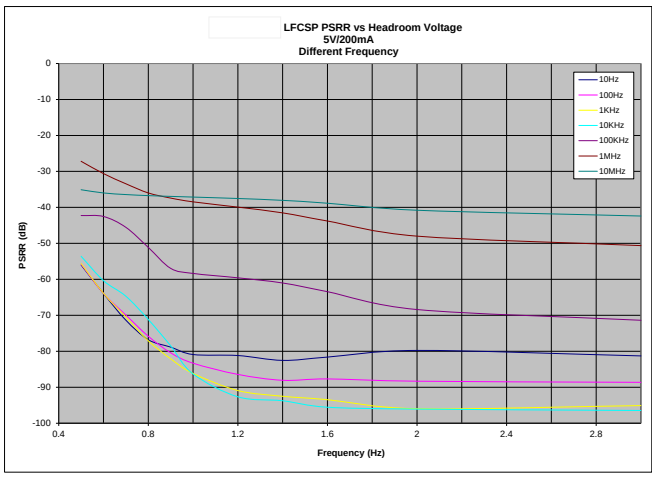


Figure 29. Power Supply Rejection Ratio vs. Headroom, V_{OUT} = 5 V, Different Frequencies

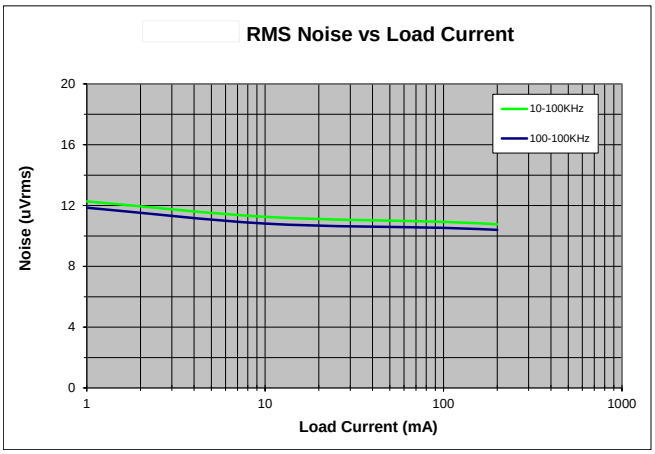


Figure 30. RMS Output Noise vs. Load Current

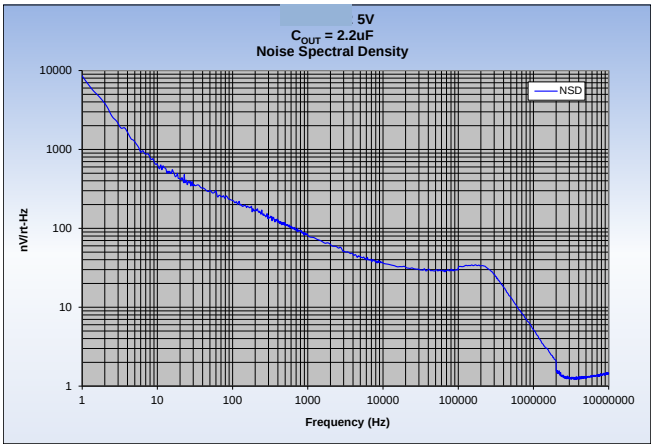


Figure 31. Output Noise Spectral Density, I_{LOAD} = 10 mA

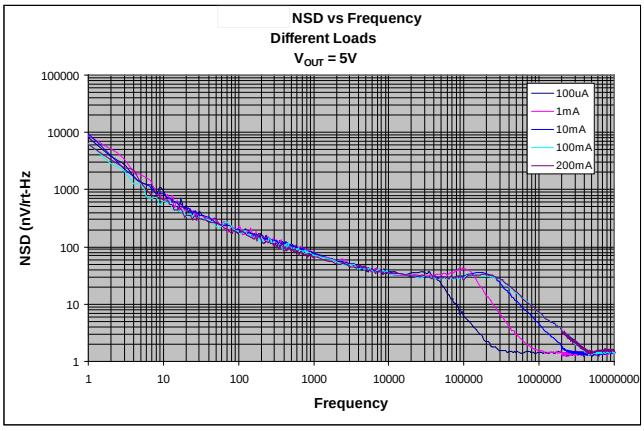


Figure 32. Output Noise Spectral Density vs I_{LOAD}

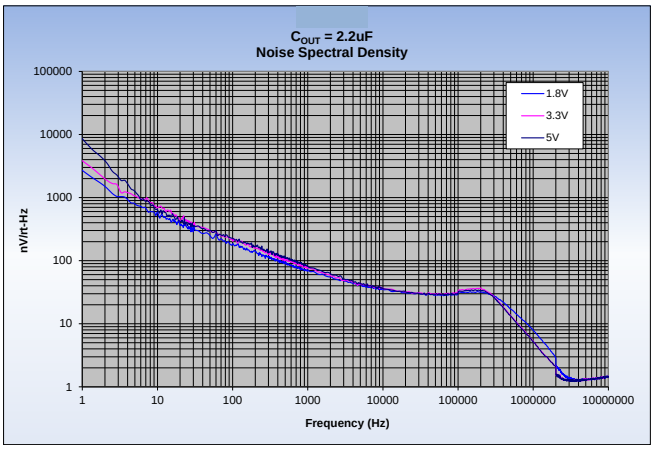


Figure 33. Output Noise Spectral Density, Different Output Voltages

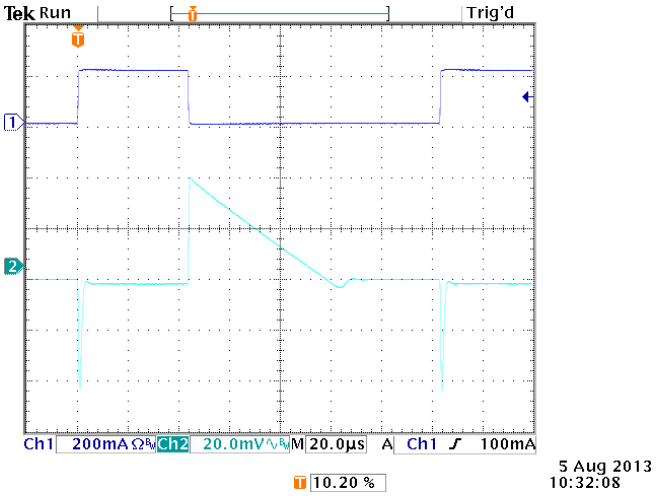


Figure 34. Load Transient Response, I_{LOAD} = 1 mA to 200 mA, V_{OUT} = 5 V, V_{IN} = 7 V, CH1 Load Current, CH2 V_{OUT}

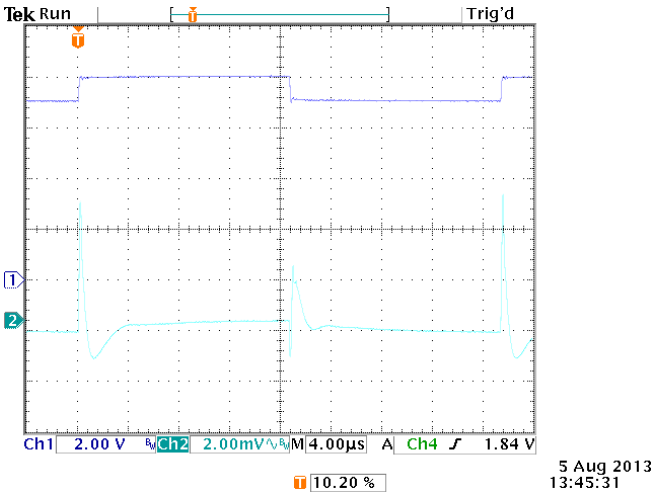


Figure 35. Line Transient Response, I_{LOAD} = 200 mA, V_{OUT} = 5 V, CH1 V_{IN}, CH2 V_{OUT}

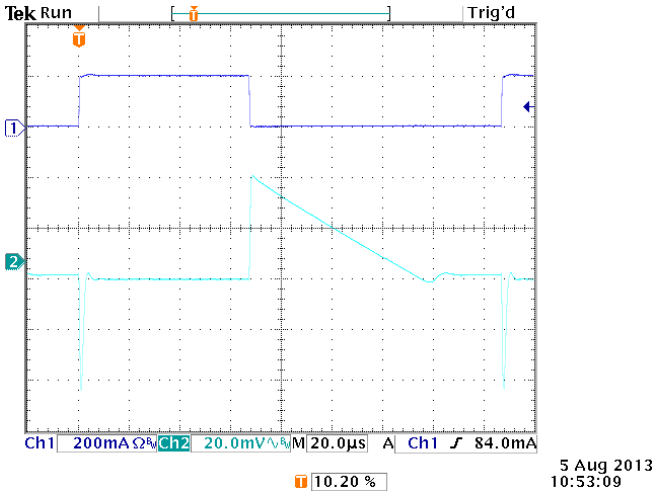


Figure 36. Load Transient Response, I_{LOAD} = 1 mA to 200 mA, V_{OUT} = 1.8 V, V_{IN} = 3 V, CH1 Load Current, CH2 V_{OUT}

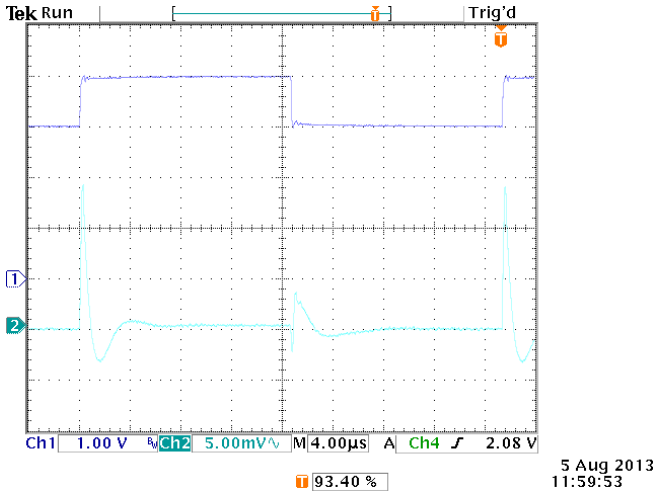


Figure 37. Line Transient Response, I_{LOAD} = 200 mA, V_{OUT} = 1.8 V, CH1 V_{IN}, CH2 V_{OUT}

THEORY OF OPERATION

The ADP7118 is a low quiescent current, low-dropout linear regulator that operates from 2.7 V to 20 V and provides up to 200 mA of output current. Drawing a low 250 µA of quiescent current (typical) at full load makes the ADP7118 ideal for portable equipment. Typical shutdown current consumption is 3 µA at room temperature.

Optimized for use with small 2.2 µF ceramic capacitors, the ADP7118 provides excellent transient performance.

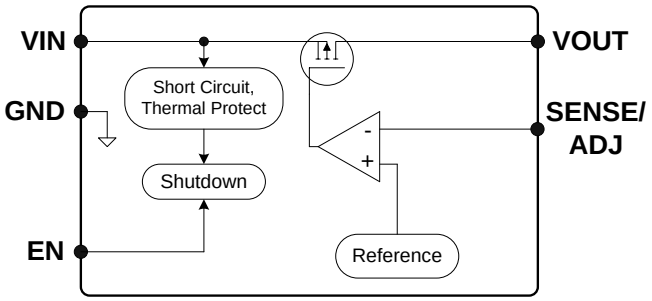


Figure 38. Internal Block Diagram

Internally, the ADP7118 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP7118 is available in 16 fixed output voltage options, ranging from 1.2 V to 5 V. The ADP7118 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5V output ADP7118 can be set to a 6V output according to the following equation:

$$V_{OUT} = 5\ V(1 + R1/R2)$$

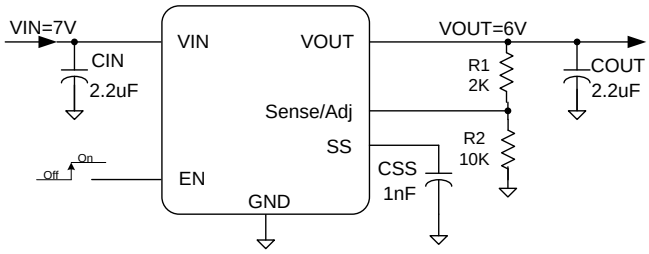


Figure 39. Typical Adjustable Output Voltage Application Schematic

The value of R2 should be less than 200 kΩ to minimize errors in the output voltage caused by the SENSE/ADJ pin input current. For example, when R1 and R2 each equal 200 kΩ and the default output voltage is 1.2V, the adjusted output voltage is 2.44 V. The output voltage error introduced by the SENSE/ADJ pin input current is 1mV or 0.04%, assuming a typical SENSE/ADJ pin input current of 10 nA at 25°C.

The ADP7118 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP7118 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 0.3 Ω or less is recommended to ensure the stability of the ADP7118. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP7118 to large changes in load current. Figure 62 shows the transient responses for an output capacitance value of 2.2 µF.

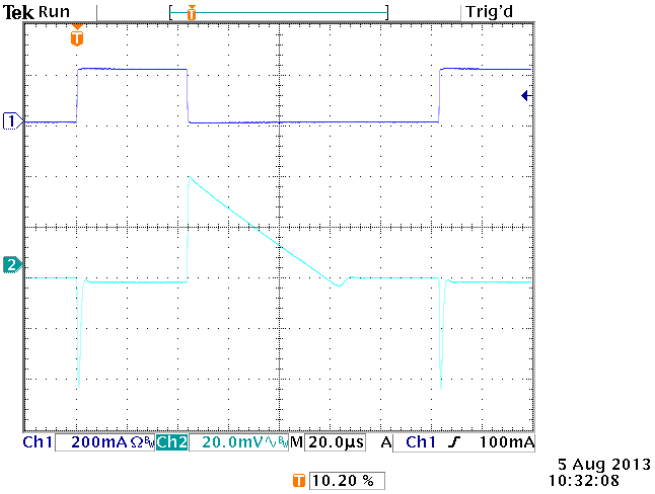


Figure 40. Output Transient Response, V_{OUT} = 5 V, C_{OUT} = 2.2 µF

Input Bypass Capacitor

Connecting a 2.2 µF capacitor from VIN to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 2.2 µF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP7118, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 100 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 63 depicts the capacitance vs. voltage bias characteristic of an 0805, 2.2 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

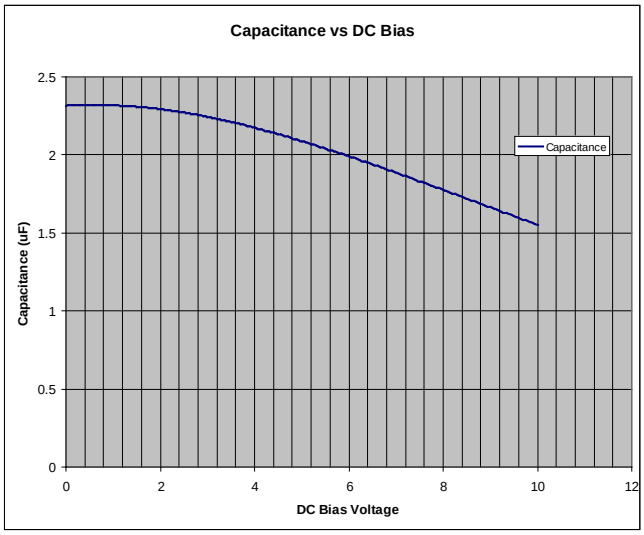


Figure 41. Capacitance vs. Voltage Characteristic

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 2.09 µF at 5 V, as shown in Figure 63.

Substituting these values in Equation 1 yields

$$C_{EFF} = 2.09\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 1.59\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7118, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

PROGRAMABLE PRECISION ENABLE

The ADP7118 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 42, when a rising voltage on EN crosses the upper threshold, nominally 1.2V, VOUT turns on. When a falling voltage on EN crosses the lower threshold, nominally 1.1V, VOUT turns off. The hysteresis of the EN threshold is approximately 100mV.

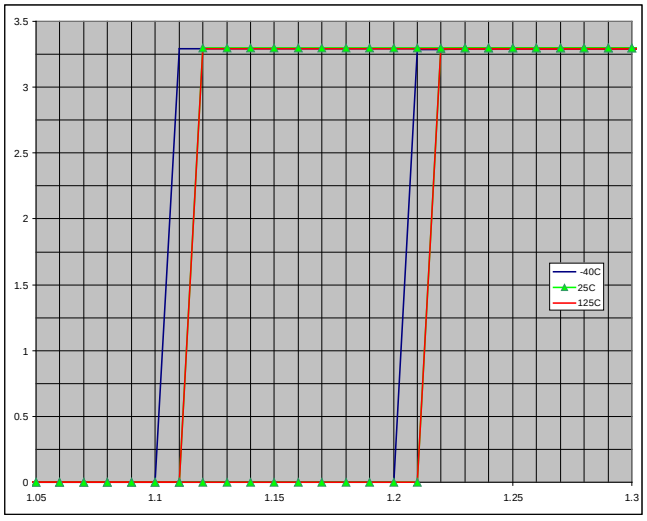


Figure 42. Typical VOUT Response to EN Pin Operation

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.2V threshold by using two resistors. The resistance values, Ren1 and Ren2 can be determined from:

Ren2 = Nominally 10KΩ to 100KΩ

$$Ren1 = Ren2 \times (V_{IN}-1.2V)/1.2V$$

where:
V_{IN} is the desired turn-on voltage.

The hysteresis voltage will increased by the factor (Ren1+Ren2) /Ren1. For the example shown in Figure 43, the enable threshold is 3.6 V with a hysteresis of 300 mV.

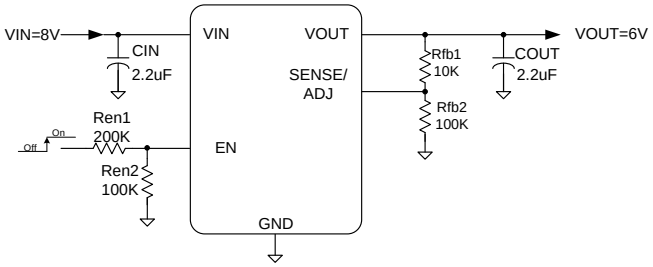


Figure 43. Typical EN Pin Voltage Divider

Figure 64 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The ADP7118 uses an internal soft-start (SS pin open) to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 320 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 44, the start-up time is dependent on the output voltage setting.

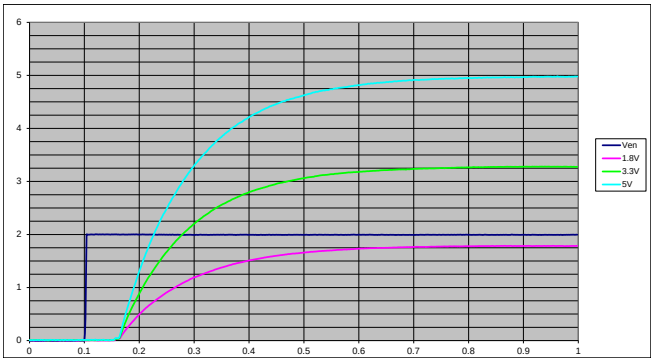


Figure 44. Typical Start-Up Behavior

SOFT START

An external capacitor connected to the SS pin determines the soft-start time. This pin may be left open for a typical 320 µS start up time. DO NOT ground this pin. When an external soft start capacitor is used, the soft start time is determined by the following equation:

$SS_{TIME}(\mu s) = 320\ \mu s + 0.6 \times C_{SS}$ where C_{SS} is in farards

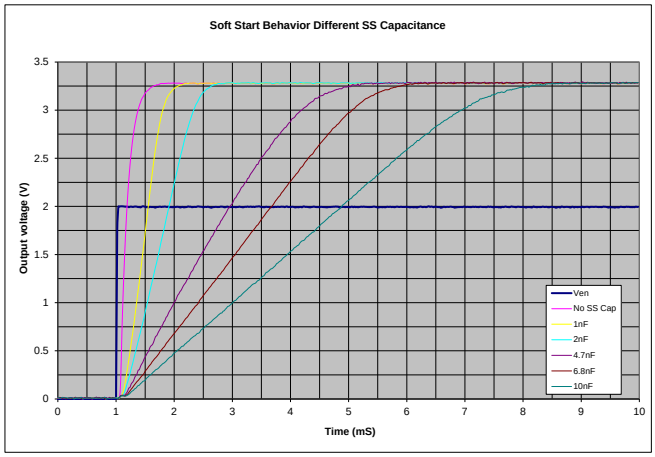


Figure 45. Typical Soft Start Behavior, Different C_{SS}

NOISE REDUCTION OF THE ADP7118 IN ADJUSTABLE MODE

The ultralow output noise of the ADP7118 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO in the conventional sense. However, the ADP7118 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5V output ADP7118 can be set to a 6V output according to the following equation:

$$V_{OUT} = 5\ V(1 + R1/R2)$$

The disadvantage using the ADP1742 in this manner is that the output voltage noise is proportional to the output voltage. Therefore, it is best to choose a fixed output voltage that is close to the target voltage to minimize the increase in output noise.

The adjustable LDO circuit may be modified to reduce the output voltage noise to levels close to that of the fixed output ADP7118. The circuit shown in Figure 46 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R_{FB1} to reduce the ac gain of the error amplifier. R_{NR} is chosen to be small with respect to R_{FB2}. If R_{NR} is 1% to 10% of the value of R_{FB2}, the minimum ac gain of the error amplifier is approximately 0.1 to 0.8 dB. The actual gain is determined by the parallel combination of R_{NR} and R_{FB1}. This ensures that the error amplifier always operates at slightly greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to $R_{FB1} - R_{NR}$ at a frequency between 1 Hz and 50 Hz. This sets the frequency where the ac gain of the error amplifier is 3 dB down from its dc gain.

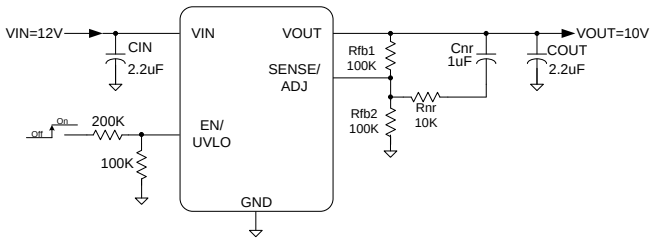


Figure 46. Noise Reduction Modification

The noise of the adjustable LDO is can be found by using the formula below assuming the noise of a fixed output LDO is approximately 11µV.

$$\text{Noise} = 11\mu V \times (R_{PAR}+R_{FB2})/R_{FB2}$$

Where:

R_{PAR} = Parallel combination of $R_{FB}1$ and R_{NR}

Based on the component values shown in Figure 46, the ADP7118 has the following characteristics:

- DC gain of 2 (6 dB)
- 3 dB roll off frequency of 1.59 Hz
- High frequency ac gain of 1.09 (0.75 dB)
- Noise reduction factor of 1.83 (5.25 dB)
- RMS noise of the adjustable LDO without noise reduction of 22 µV rms
- RMS noise of the adjustable LDO with noise reduction (assuming 11 µV rms for fixed voltage option) of 12 µV rms

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7118 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP7118 is designed to current limit when the output load reaches 400 mA (typical). When the output load exceeds 400 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP7118 current limits, so that only 400 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 400 mA into the short, again causing the junction temperature

to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 400 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with low input-to-output voltage differential, the ADP7118 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough that it causes the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP7118 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 5 shows typical θ_{JA} values of the 8-lead SOIC and 6-lead LFCSP and 5-Lead TSOT packages for various PCB copper sizes.

Table 6 shows the typical Ψ_{JB} values of the 8-lead SOIC, 6-lead LFCSP, and 5-Lead TSOT.

Table 5. Typical θ_{JA} Values

	θ_{JA} (°C/W)		
Copper Size (mm²)	**LFCSP**	**SOIC**	**TSOT**
25[1]	182.8	n/a	n/a
50	n/a	181.4	152
100	142.6	145.4	146
500	83.9	89.3	131
1000	71.7	77.5	n/a
6400	57.4	63.2	n/a

[1] Device soldered to minimum size pin traces.

Table 6. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
LFCSP	24
SOIC	38.8
TSOT	43

The junction temperature of the ADP7118 is calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 47 to Figure 55 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

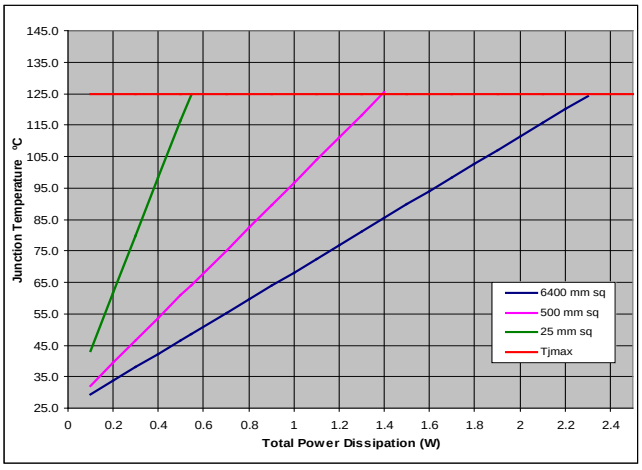


Figure 47. LFCSP, T_A = 25°C

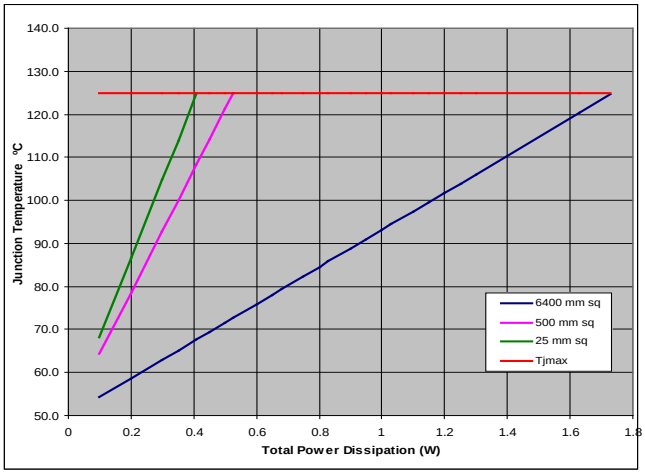


Figure 48. LFCSP, T_A = 50°C

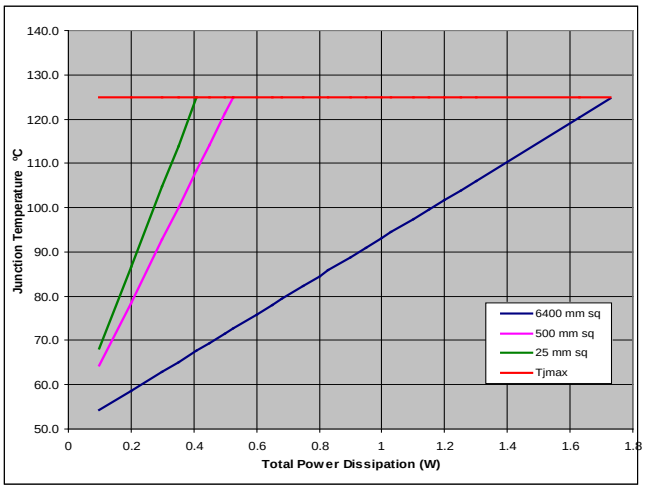


Figure 49. LFCSP, T_A = 85°C

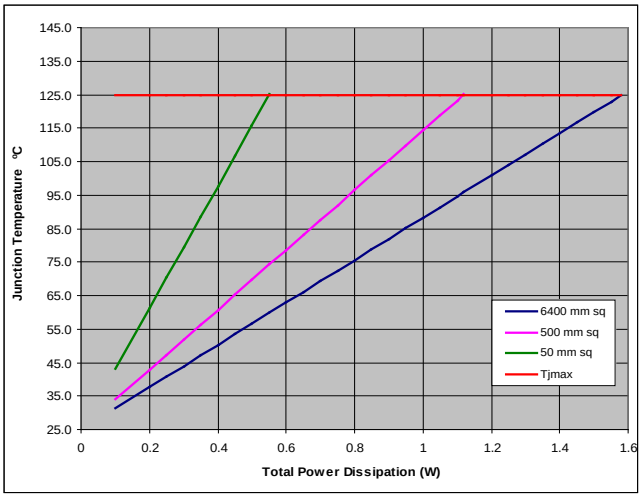


Figure 50. SOIC, T_A = 25°C

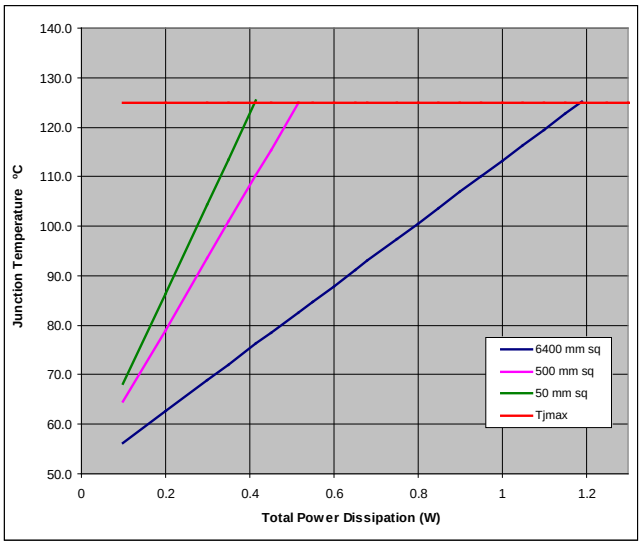


Figure 51. SOIC, T_A = 50°C

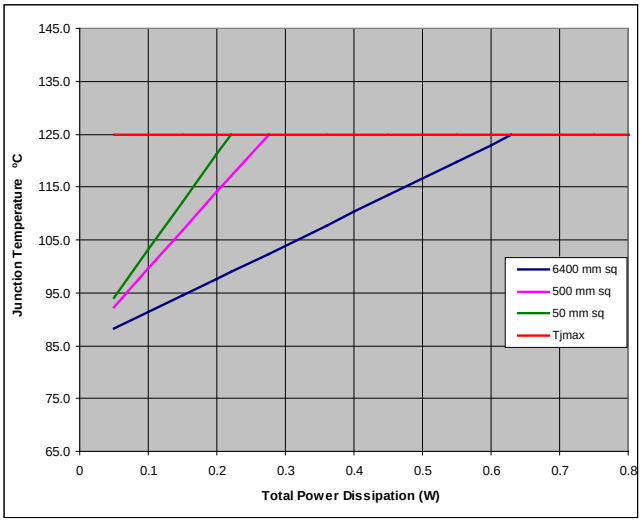


Figure 52. SOIC, T_A = 85°C

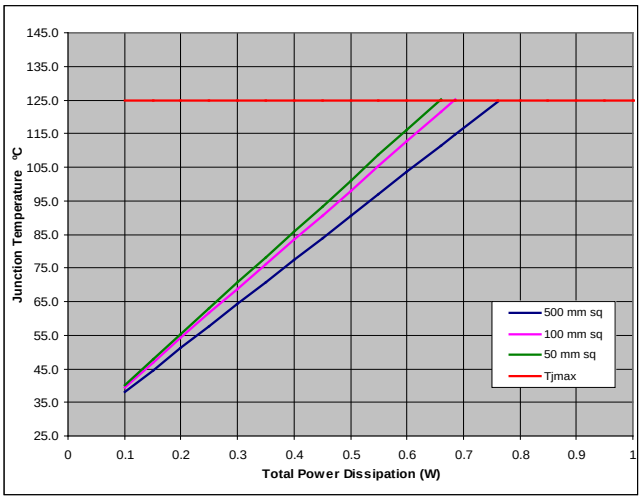


Figure 53. TSOT, T_A = 25°C

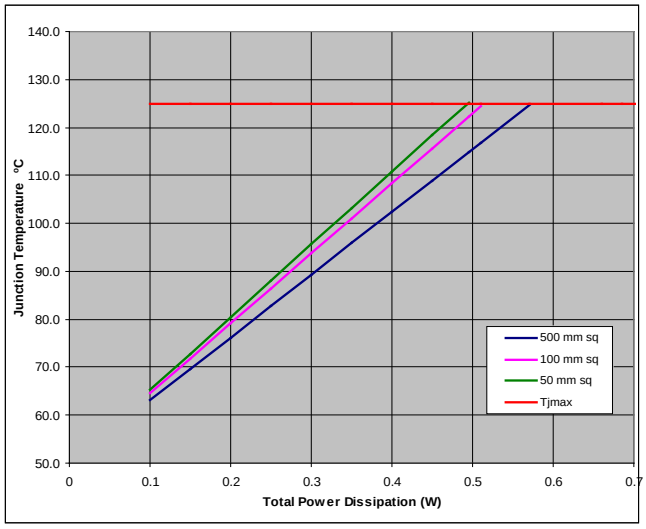


Figure 54. TSOT, T_A = 50°C

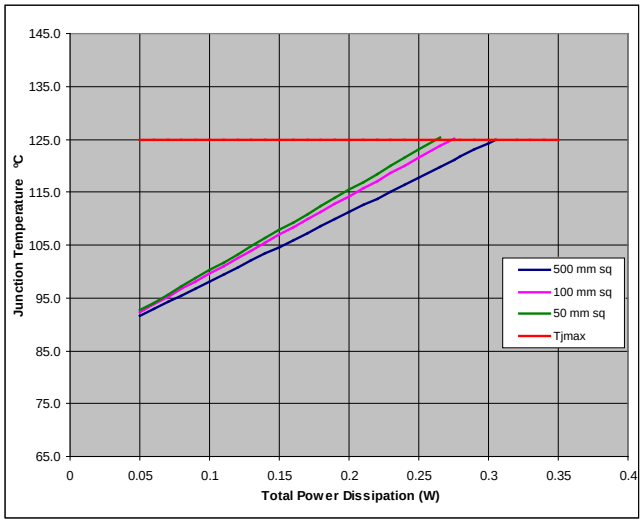


Figure 55. TSOT, T_A = 85°C

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 56, Figure 57, and Figure 58). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of Ψ_{JB} is 24°C/W for the 8-lead LFCSP package, 38.8°C/W for the 8-lead SOIC package and 43°C/W for the 5-lead TSOT package.

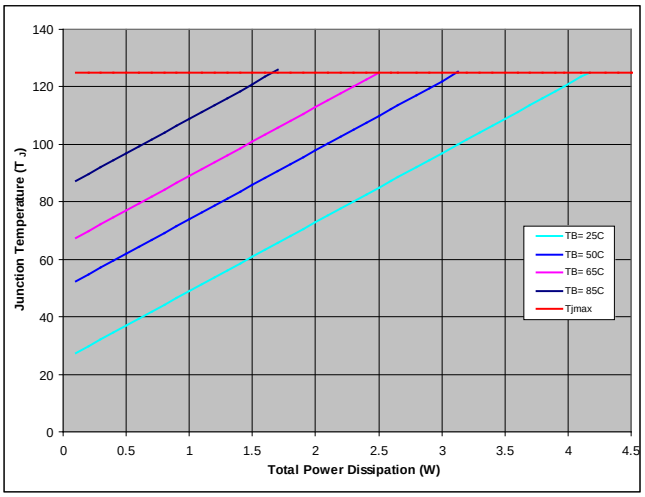


Figure 56. LFCSP

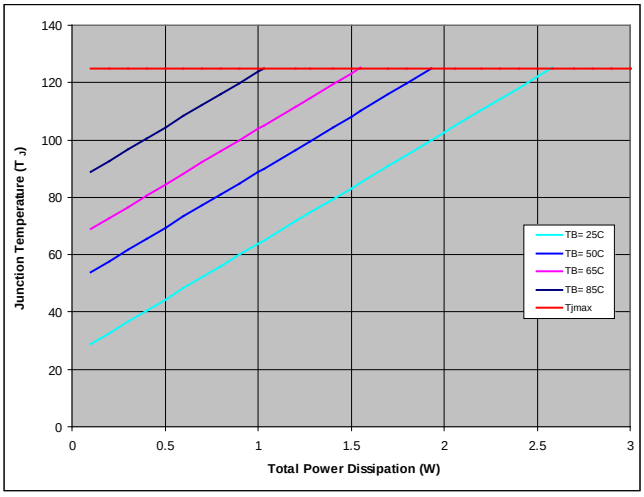


Figure 57. SOIC

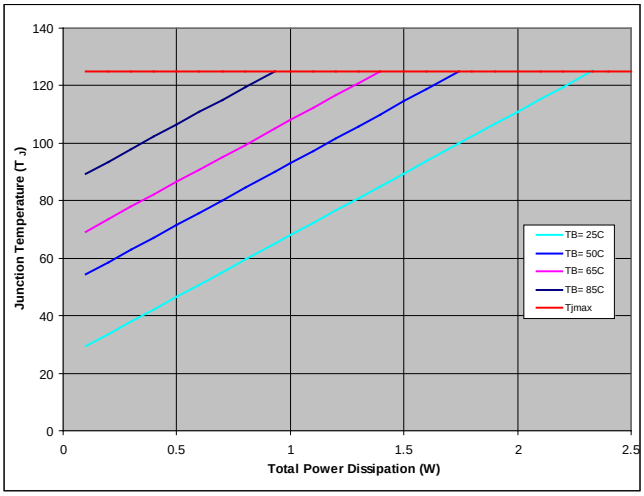


Figure 58. TSOT

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP7118. However, as listed in Table 5, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0805 or 1206 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

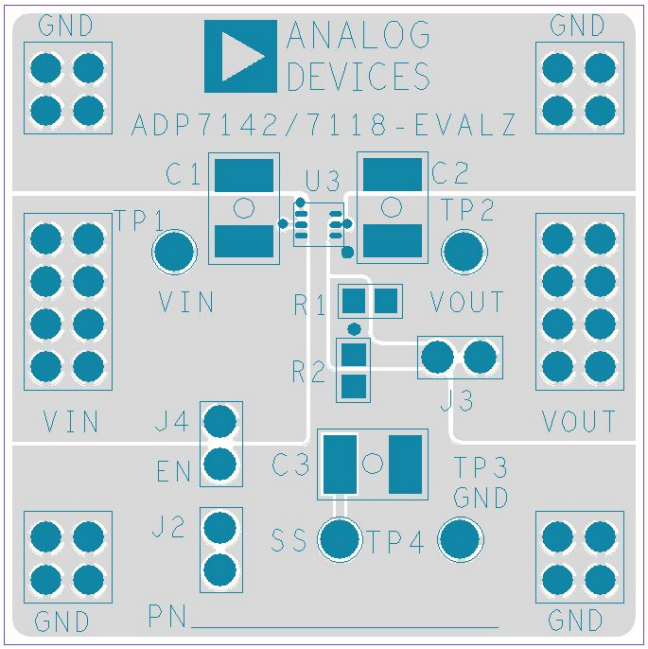


Figure 59. Example LFCSP PCB Layout

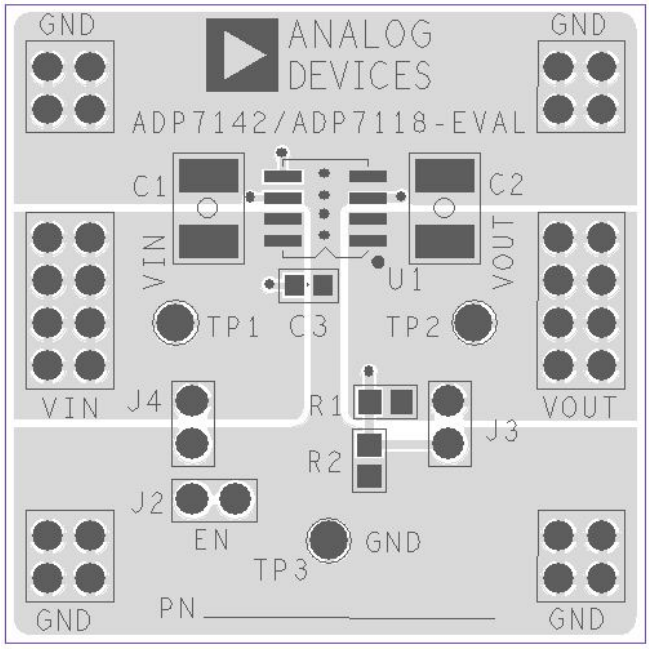


Figure 60. Example SOIC PCB Layout

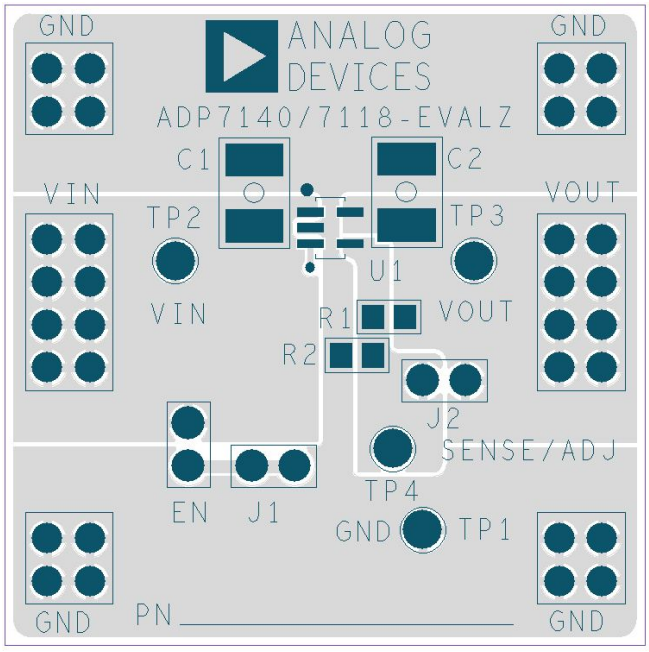


Figure 61. Example TSOT PCB Layout

OUTLINE DIMENSIONS

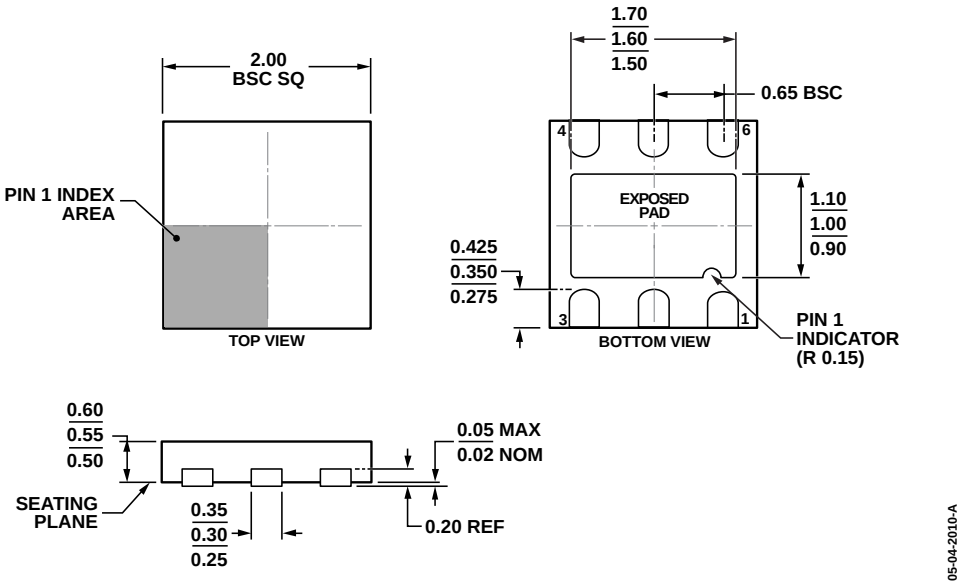
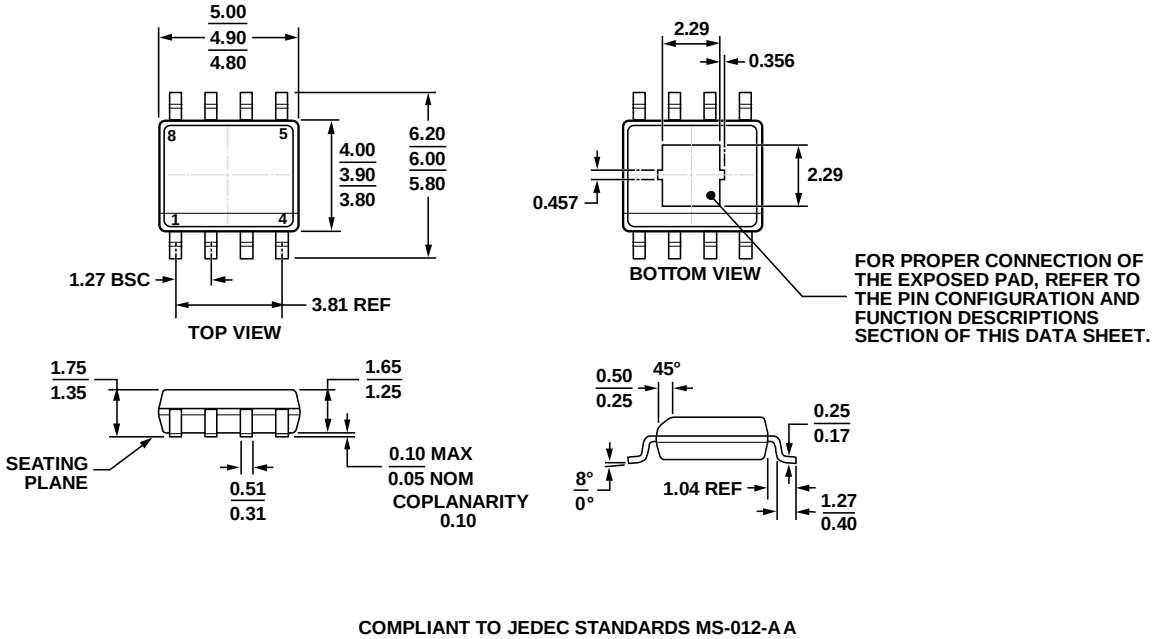
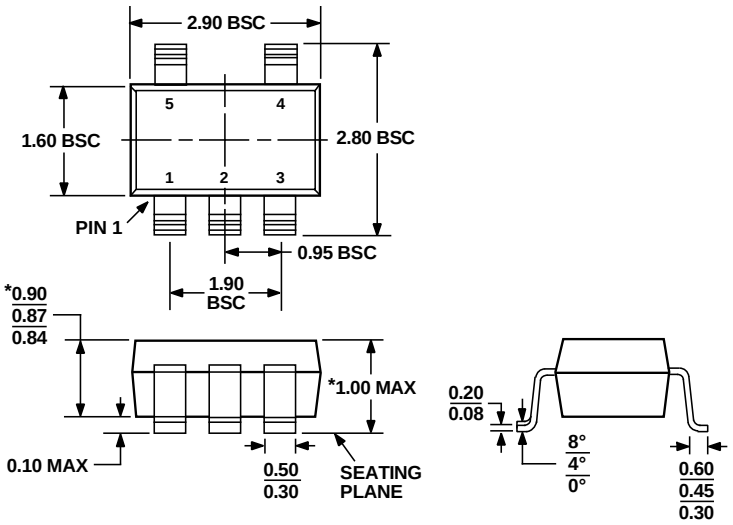


Figure 62. 6-Pin Leadframe Chip Scale Package [LFCSP]
(CP6-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-A A

Figure 63. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-193-AB WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 64. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2, 3]	Package Description	Package Option	Branding
ADP7118ACPZN-R2	−40°C to +125°C	Adjustable	6-Lead LFCSP_WD	CP-6-3	LP4
ADP7118ACPZN-R7	−40°C to +125°C	Adjustable	6-Lead LFCSP_WD	CP-6-3	LP4
ADP7118ACPZN-1.8-R2	−40°C to +125°C	1.8	6-Lead LFCSP_WD	CP-6-3	LP5
ADP7118ACPZN-1.8-R7	−40°C to +125°C	1.8	6-Lead LFCSP_WD	CP-6-3	LP5
ADP7118ACPZN-2.5-R2	−40°C to +125°C	2.5	6-Lead LFCSP_WD	CP-6-3	LP6
ADP7118ACPZN-2.5-R7	−40°C to +125°C	2.5	6-Lead LFCSP_WD	CP-6-3	LP6
ADP7118ACPZN-3.3-R2	−40°C to +125°C	3.3	6-Lead LFCSP_WD	CP-6-3	LP7
ADP7118ACPZN-3.3-R7	−40°C to +125°C	3.3	6-Lead LFCSP_WD	CP-6-3	LP7
ADP7118ACPZN-5.0-R2	−40°C to +125°C	5	6-Lead LFCSP_WD	CP-6-3	LP8
ADP7118ACPZN-5.0-R7	−40°C to +125°C	5	6-Lead LFCSP_WD	CP-6-3	LP8
ADP7118ARDZ-R7	−40°C to +125°C	Adjustable	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-1.8	−40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-1.8-R7	−40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-2.5	−40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-2.5-R7	−40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-3.3	−40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-3.3-R7	−40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-5.0	−40°C to +125°C	5	8-Lead SOIC_N_EP	RD-8-2	
ADP7118ARDZ-5.0-R7	−40°C to +125°C	5	8-Lead SOIC_N_EP	RD-8-2	
ADP7118AUJZ-R2	−40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LP4
ADP7118AUJZ-R7	−40°C to +125°C	Adjustable	5-Lead TSOT	UJ-5	LP4
ADP7118AUJZ-1.8-R2	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LP5
ADP7118AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LP5
ADP7118AUJZ-2.5-R2	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LP6
ADP7118AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LP6
ADP7118AUJZ-3.3-R2	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LP7
ADP7118AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LP7
ADP7118AUJZ-5.0-R2	−40°C to +125°C	5	5-Lead TSOT	UJ-5	LP8
ADP7118AUJZ-5.0-R7	−40°C to +125°C	5	5-Lead TSOT	UJ-5	LP8
ADP7118UJ-EVALZ		3.3	TSOT Evaluation Board		
ADP7118CP-EVALZ		3.3	LFCSP Evaluation Board		
ADP7118RD-EVALZ		3.3	SOIC Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.
[3] The evaluation boards are preconfigured with a 3.3 V ADP7118.