



256Kx16 MONOLITHIC SRAM

FEATURES

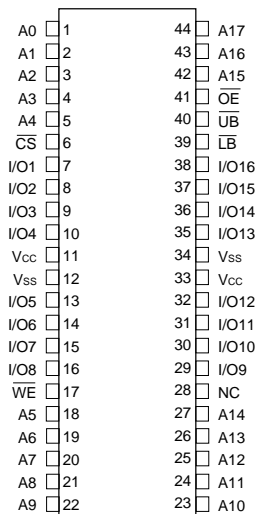
- 256Kx16 bit CMOS Static
- Random Access Memory
 - Access Times of 17, 20, 25, 35ns
 - Data Retention Function (LPA version)
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- 44 lead JEDEC Approved Revolutionary Pinout
 - Ceramic SOJ (Package 322)
 - Ceramic Flatpack (Package 323)
- Single +5V (±10%) Supply Operation

The EDI816256CA is a 4 megabit Monolithic CMOS Static RAM. The EDI816256CA uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device allows upper and lower byte access by use of the data byte control pins (\overline{LB} , \overline{UB}).

The devices are available in a fully hermetic 44 lead ceramic SOJ and a 44 lead Ceramic Flatpack. The Ceramic SOJ is pin for pin compatible with the commercially available plastic SOJ. This allows the user the luxury of designing a board that can be used for both the commercial and military market.

A Low Power version with Data Retention (EDI816256LPA) is also available for battery backed applications. Military product is available compliant to Appendix A of MIL-PRF-38535.

PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A0-17	Address Inputs
\overline{LB} (I/O1-8)	Lower-Byte Control (I/O1-8)
\overline{UB} (I/O9-16)	Upper-Byte Control (I/O9-16)
I/O1-16	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+5.0V Power
Vss	Ground
NC	No Connection



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Voltage on any pin relative to VSS	-0.5 to 7.0	V
Operating Temperature T _A (Ambient)		
Commercial	0 to +70	°C
Industrial	-40 to +85	°C
Military	-55 to +125	°C
Storage Temperature, Plastic	-65 to +125	°C
Power Dissipation	1.5	W
Output Current	20	mA
Junction Temperature, T _J	175	°C

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Address Lines	C _I	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	12	pF
Data Lines	C _{D/Q}	V _{IN} = V _{CC} or V _{SS} , f = 1.0MHz	14	pF

These parameters are sampled, not 100% tested.

TRUTH TABLE

CS	WE	OE	LB	UB	Mode	Data I/O		Supply Current
						I/O1-8	I/O9-16	
H	X	X	X	X	Not Select	High Z	High Z	I _{CC2} , I _{CC3}
L	H	H	X	X	Output Disable			
L	X	X	H	H				
L	H	L	L	H	Read	Data Out	High Z	I _{CC1}
			H	L		High Z	Data Out	
			L	L		Data Out	Data Out	
L	L	X	L	H	Write	Data In	High Z	I _{CC1}
			H	L		High Z	Data In	
			L	L		Data In	Data In	

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} +0.5	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min		Max		Units
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}				10	µA
Output Leakage Current	I _{LO}	V _{I/O} = 0V to V _{CC}				10	µA
Operating Power Supply Current	I _{CC1}	WE, CS = V _{IL} , I _{I/O} = 0mA, Min Cycle				300	mA
Standby (TTL) Power Supply Current	I _{CC2}	CS ≥ V _{IH} , V _{IN} ≤ V _{IL} , V _{IN} ≥ V _{IH}				60	mA
Full Standby Power Supply Current	I _{CC3}	CS ≥ V _{CC} -0.2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	CA	—		25	mA
			LPA	—		16	mA
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA				0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4				V

NOTE: DC test conditions: V_{IL} = 0.3V, V_{IH} = V_{CC} -0.3V

AC TEST CONDITIONS

Figure 1

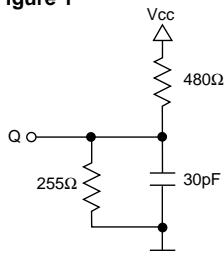
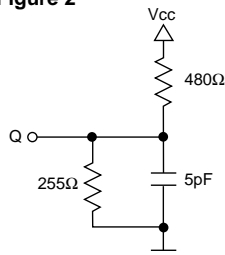


Figure 2



Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

NOTE: For t_{EH0Z}, t_{GH0Z} and t_{WLOZ}, C_L = 5pF (Figure 2)



AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		17ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	tAVAV	tRC	17		20		25		35		ns
Address Access Time	tAVQV	tAA		17		20		25		35	ns
Chip Enable Access Time	tELQV	tACS		17		20		25		35	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	2		5		5		5		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ	0	7	0	7	0	8	0	10	ns
Output Hold from Address Change	tAVQX	tOH	0		0		0		0		ns
Output Enable to Output Valid	tGLQV	tOE		10		10		12		15	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	0		0		0		0		ns
Output Disable to Output in High Z(1)	tGHQZ	tOHZ	0	7	0	7	0	8	0	10	ns
\overline{LB} , \overline{UB} Access Time	tUBLQV tLBLOV	tBA		10		10		12		15	ns
\overline{LB} , \overline{UB} Enable to Low Z Output	tUBLQX tLBLOX	tBLZ	0	0		0		0		0	ns
\overline{LB} , \overline{UB} Disable to High Z Output	tUBHQZ tLBHQZ	tBHZ	0	7	0	7	0	8	0	10	ns

NOTE:

1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

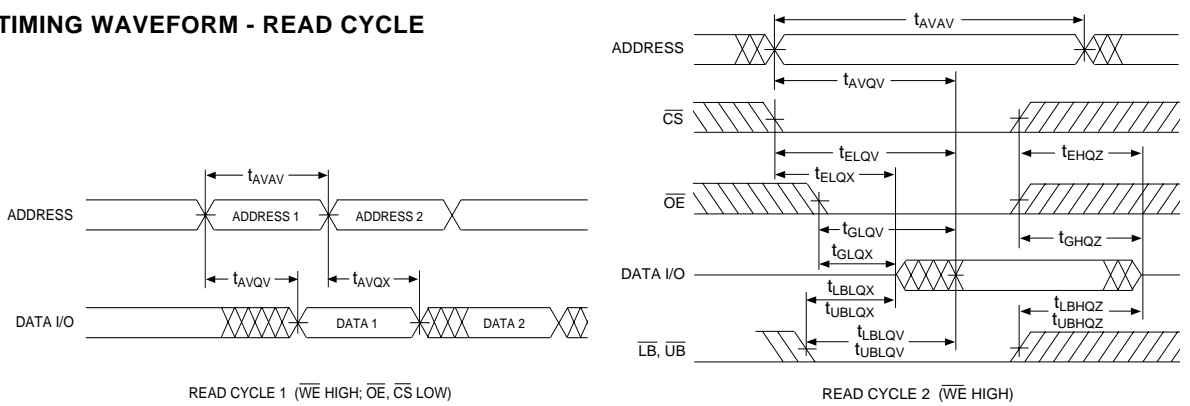
Parameter	Symbol		17ns		20ns		25ns		35ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	17		20		25		35		ns
Chip Enable to End of Write	tELWH tELEH	tCW tCW	14 14		15 15		17 17		20 20		ns ns
Address Setup Time	tAVWL tAVEL tAVUBL	tAS tAS tAS	0 0 0		0 0 0		0 0 0		0 0 0		ns ns ns
Address Valid to End of Write	tAVWH tAVEH tAVUBH	tAW tAW tAW	14 14 14		15 15 15		17 17 17		20 20 20		ns ns ns
Write Pulse Width	tWLWH tWLEH	tWP tWP	14 14		14 14		15 15		17 17		ns ns
Write Recovery Time	tWHAX tEHAX	tWR tWR	0 0		0 0		0 0		0 0		ns ns
Data Hold Time	tWHDX tEHDX	tDH tDH	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	tWLOZ	tWHZ	0	8	0	8	0	8	0	10	ns
Data to Write Time	tDWWH tDVEH	tDW tDW	10 10		10 10		12 12		15 15		ns ns
Output Active from End of Write (1)	tWHQX	tWLZ	0		0		0		0		ns
\overline{LB} , \overline{UB} Valid to End of Write	tLBLEH tUBLUBH	tBW	14		16		18		20		ns

NOTE:

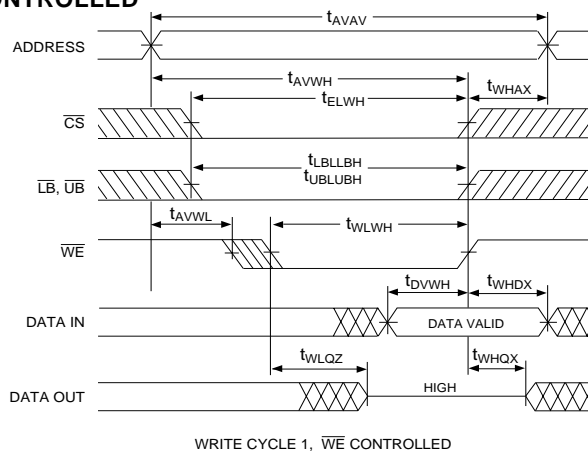
1. This parameter is guaranteed by design but not tested.



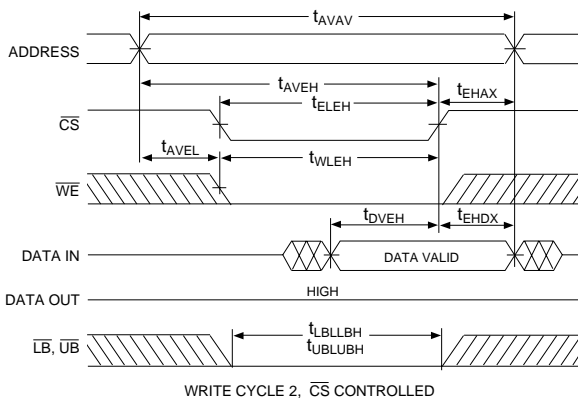
TIMING WAVEFORM - READ CYCLE



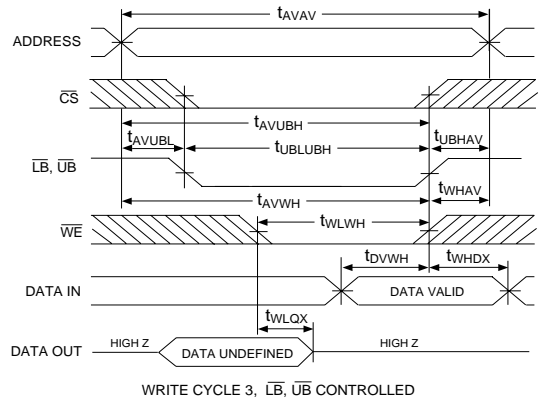
WRITE CYCLE - \overline{WE} CONTROLLED



WRITE CYCLE - \overline{CS} CONTROLLED



WRITE CYCLE - \overline{LB} , \overline{UB} CONTROLLED





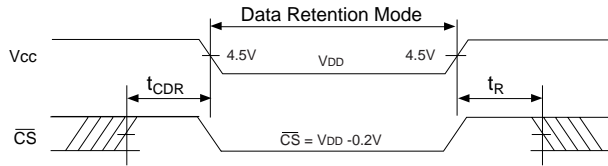
DATA RETENTION CHARACTERISTICS (EDI816256LPA ONLY)
(TA = -55°C to +125°C)

Table with 7 columns: Characteristic, Sym, Conditions, Min, Typ, Max, Units. Rows include Data Retention Voltage, Data Retention Quiescent Current, Chip Disable to Data Retention Time (1), and Operation Recovery Time (1).

NOTE:

- 1. This parameter is guaranteed by design but not tested.
* Read Cycle Time

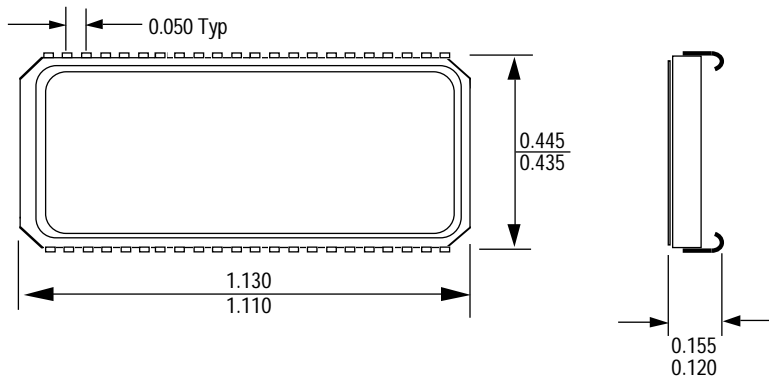
DATA RETENTION - CS CONTROLLED



DATA RETENTION, CS CONTROLLED

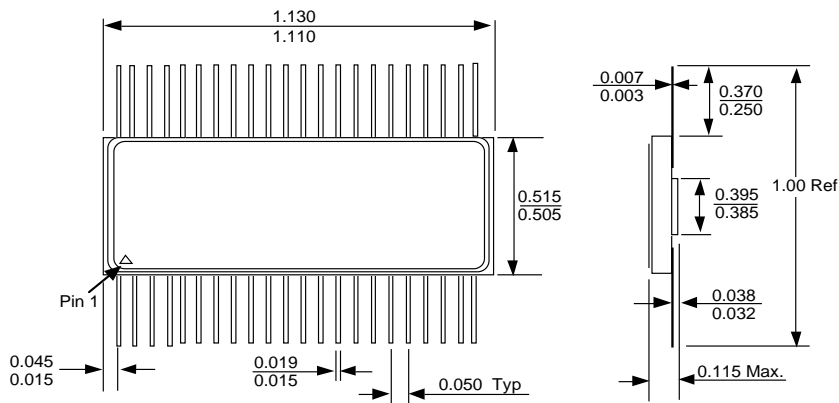


PACKAGE 322: 44 LEAD, CERAMIC SOJ



DIMENSIONS ARE IN INCHES

PACKAGE 323: 44 PIN, CERAMIC FLATPACK



DIMENSIONS ARE IN INCHES



ORDERING INFORMATION

EDI 8 16 256 CA X X X

WHITE ELECTRONIC DESIGNS _____

SRAM _____

ORGANIZATION, 256Kx16 _____

TECHNOLOGY: _____

CA = CMOS Standard Power

LPA = Low Power

ACCESS TIME (ns) _____

PACKAGE TYPE: _____

F44 = 44 pin Ceramic Flatpack (Package 323)

N44 = 44 lead Ceramic SOJ (Package 322)

DEVICE GRADE: _____

B = MIL-STD-883 Compliant

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C