

TYPES SN54LS114A, SN54S114, SN74LS114A, SN74S114 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the preset and clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54LS114A and SN54S114 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LS114A and SN74S114 are characterized for operation from 0°C to 70°C .

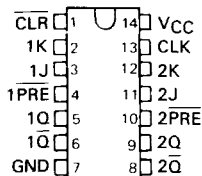
FUNCTION TABLE

INPUTS			OUTPUTS			
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H [†]	H [†]
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q ₀	\bar{Q}_0

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} minimum. Furthermore, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

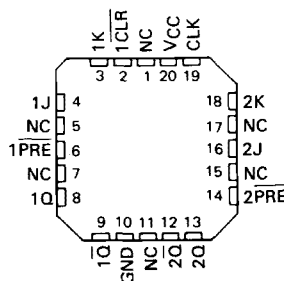
SN54LS114A, SN54S114 ... J OR W PACKAGE
SN74LS114A, SN74S114 ... D, J OR N PACKAGE

(TOP VIEW)



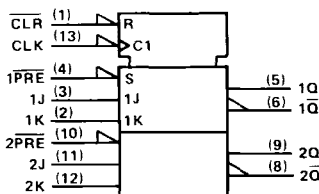
SN54LS114A, SN54S114 ... FK PACKAGE
SN74LS114A, SN74S114 ... FN PACKAGE

(TOP VIEW)



NC - No internal connection

logic symbol



Pin numbers shown on logic notation are for D, J or N packages.

3

TTL DEVICES

PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

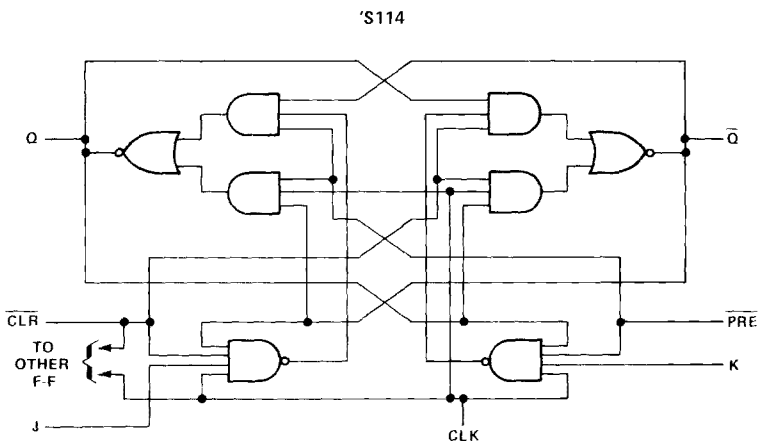
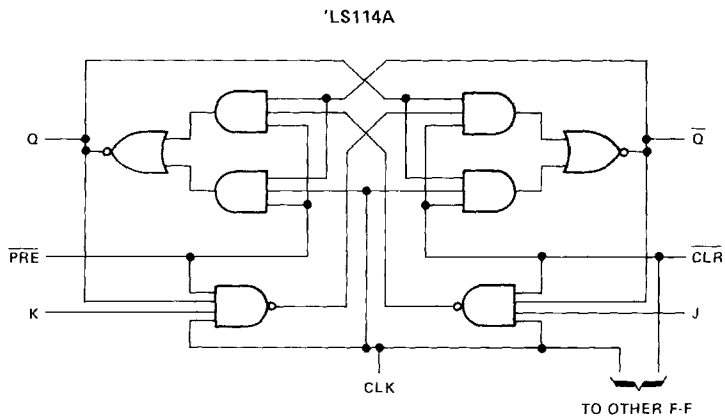
TEXAS
INSTRUMENTS

POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

3-455

TYPES SN54LS114A, SN54S114, SN74LS114A, SN74S114
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

logic diagram



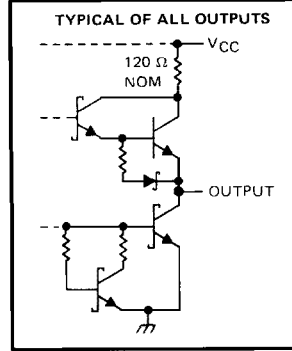
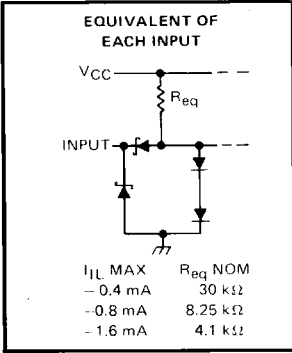
3

TTL DEVICES

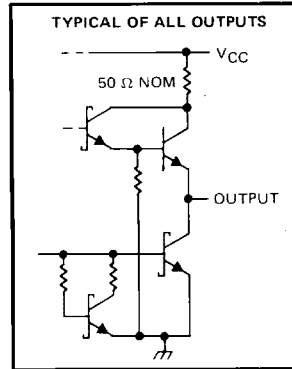
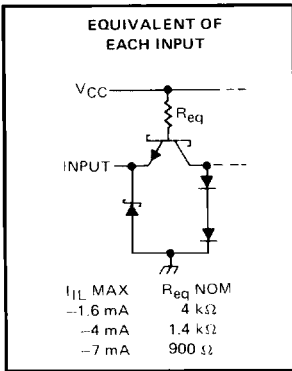
TYPES SN54LS114A, SN54S114, SN74LS114A, SN74S114 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

schematics of inputs and outputs

'LS114A



'S114



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: 'LS114A	7 V
'S114	5.5 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

3

TTL DEVICES

TYPES SN54LS114A, SN74LS114A DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SN54LS114A			SN74LS114A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.7			V
I_{OH}	High-level output current				-0.4			mA
I_{OL}	Low-level output current				4			mA
f_{clock}	Clock frequency	0			30			MHz
t_w	Pulse duration	CLK		20		20		ns
		\overline{PRE} or \overline{CLR} low		25		25		
t_{su}	Set up time-before CLK ↓	data high or low		20		20		ns
		\overline{CLR} inactive		25		25		
		\overline{PRE} inactive		20		20		
t_h	Hold time-data after CLK ↓	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS114A		SN74LS114A		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
V_{IK}		$V_{CC} = \text{MIN}, I_I = 18 \text{ mA}$		-1.5		-1.5		V	
V_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.4 \text{ mA}$		2.5	3.4	2.7	3.4	V	
V_{OL}		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V	
		$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{IH} = 2 \text{ V}, I_{OL} = 8 \text{ mA}$				0.35	0.5		
I_I	J or K	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1		0.1		mA
	\overline{CLR}				0.6		0.6		
	\overline{PRE}				0.3		0.3		
	CLK				0.8		0.8		
I_{IH}	J or K	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20		20		μA
	\overline{CLR}				120		120		
	\overline{PRE}				60		60		
	CLK				160		160		
I_{IL}	J or K	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4		-0.4		mA
	\overline{CLR}				-1.6		-1.6		
	\overline{PRE}				-0.8		-0.8		
	CLK				-1.6		-1.6		
$I_{OS}§$		$V_{CC} = \text{MAX}$,	see Note 4		-20	-100	-20	-100	mA
I_{CC}		$V_{CC} = \text{MAX}$,	see Note 2		4	6	4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O = 2.25 \text{ V}$ and 2.125 V for the '54 family and the '74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

**TYPES SN54LS114A, SN74LS114A
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS
WITH PRESET, COMMON CLEAR, AND COMMON CLOCK**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$	30	45		MHz
t_{PLH}	$\overline{\text{CLR}}$, $\overline{\text{PRE}}$ or CLK	Q or $\overline{\text{Q}}$		15	20		ns
t_{PHL}				15	20		ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

TYPES SN54S114, SN74S114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SN54S114			SN74S114			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage				0.8			V
I _{OH}	High-level output current	-1			-1			mA
I _{OL}	Low-level output current	20			20			mA
t _w	Pulse duration	CLK high		6	6		ns	
		CLK low		6.5	6.5			
		CLR or PRE low		8	8			
t _{su}	Setup time	data high or low		3	3		ns	
t _h	Hold time-data after CLK ↓			0	0		ns	
T _A	Operating free-air temperature	-55	125		0	70		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S114			SN74S114			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{IK}	V _{CC} = MIN, I _I = -18 mA	-1.2			-1.2			V
V _{OH}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	2.5	3.4		2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	0.5			0.5			V
I _I	V _{CC} = MAX, V _I = 5.5 V	1			1			mA
I _{IH}	J or K	50			50			μA
	CLR	200			200			
	PRE	100			100			
	CLK	200			200			
I _{IL}	J or K	-1.6			-1.6			mA
	CLR	-14			-14			
	PRE	-7			-7			
	CLK	-8			-8			
I _{OS} §	V _{CC} = MAX	-40	-100		-40	-100	mA	
I _{CC}	V _{CC} = MAX, see Note 2	15 25		15 25		mA		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}				80	125		MHz
t _{PLH}	PRE or CLR	Q or \bar{Q}	R _L = 280 Ω, C _L = 15 pF	4	7		ns
t _{PHL}	PRE or CLR (CLK high)	\bar{Q} or Q		5	7		ns
	PRE or CLR (CLK low)			5	7		ns
t _{PLH}	CLK	Q or \bar{Q}		4	7		ns
t _{PHL}			5	7		ns	

NOTE 3: See General Information Section for load circuits and voltage waveforms.