

NCV4275

Advance Information 5 V Low-Drop Voltage Regulator

This industry standard linear regulator has the capability to drive loads up to 450 mA at 5 V. It is available in DPAK, D²PAK, and TO-220 options. This device is pin-for-pin compatible with Infineon part number TLE4275.

Features

- 5 V, $\pm 2\%$, 450 mA Output Voltage
- Very Low Current Consumption
- Active $\overline{\text{RESET}}$
- Reset Low Down to $V_Q = 1$ V
- 500 mV (max) Dropout Voltage
- Fault Protection
 - ◆ +45 V Peak Transient Voltage
 - ◆ -42 V Reverse Voltage
 - ◆ Short Circuit
 - ◆ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes

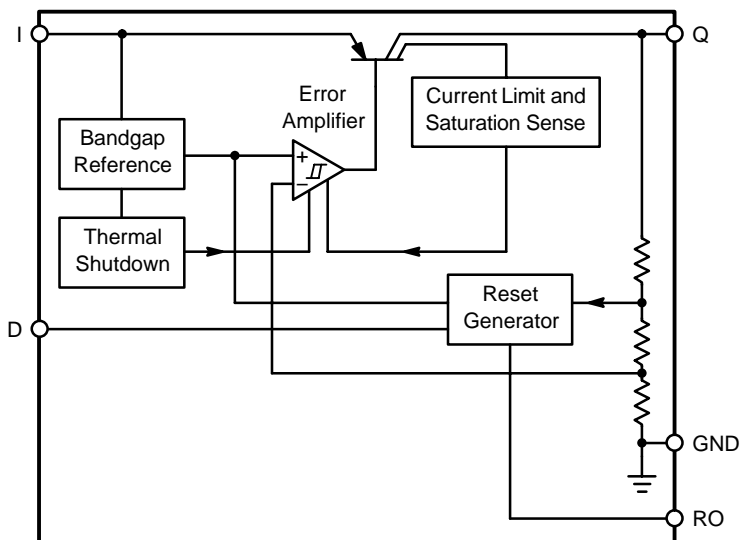


Figure 1. Block Diagram

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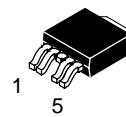
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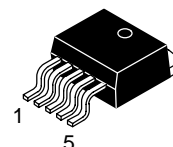


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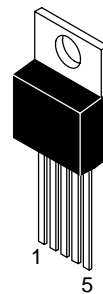


DPAK
5-PIN
DT SUFFIX
CASE 175AA

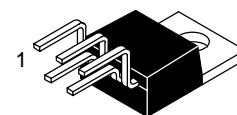


D²PAK
5-PIN
DS SUFFIX
CASE 936AC

Pin 1. I
2. RO
3. GND
4. D
5. Q



TO-220
FIVE LEAD
T SUFFIX
CASE 314D



TO-220
FIVE LEAD
TV SUFFIX
CASE 314K

ORDERING INFORMATION

Device	Package	Shipping
NCV4275DT	DPAK*	75 Units/Rail
NCV4275DTRK	DPAK*	2500 Tape & Reel
NCV4275DS	D ² PAK*	50 Units/Rail
NCV4275DSR4	D ² PAK*	750 Tape & Reel
NCV4275T	TO-220* STRAIGHT	50 Units/Rail
NCV4275TV	TO-220* BENT	50 Units/Rail

*Five pin/lead.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 6 of this data sheet.

NCV4275

MAXIMUM RATINGS*†

Rating	Min	Max	Unit
Input [I (DC)]	-42	45	V
Input [I (Peak Transient Voltage)]	-	TBD	V
Output (Q)	-1.0	16	V
Reset Output (RO)	-0.3	25	V
Reset Output (RO)	-5.0	5.0	mA
Reset Delay (D)	-0.3	7.0	V
Reset Delay (D)	-2.0	2.0	mA
Operating Range (I)	5.5	42	V
ESD Susceptibility (Human Body Model)	2.0	-	kV
Junction Temperature	-40	150	°C
Storage Temperature	-55	150	°C
Package Thermal Resistance, DPAK, 5-Pin : Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Package Thermal Resistance, D ² PAK, 5-Pin : Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Package Thermal Resistance, TO-220, 5-Lead: Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	- -	TBD TBD	°C/W °C/W
Lead Temperature Soldering Reflow (SMD styles only) Note 1	-	240 Peak (Note 3)	°C
Wave Solder (through hole styles only) Note 2	-	260 Peak	°C

1. 60 seconds max above 183°C.

2. 10 seconds max.

3. -5°C/+0°C allowable conditions.

*The maximum package power dissipation must be observed.

†During the voltage range which exceeds the maximum tested voltage of I, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

NCV4275

ELECTRICAL CHARACTERISTICS (I = 13.5 V; -40°C < T_J < 150°C; unless otherwise noted)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output					
Output Voltage	5.0 mA < I _Q < 400 mA, 6.0 V < V _I < 28 V	4.9	5.0	5.1	V
Output Voltage	5.0 mA < I _Q < 200 mA, 6.0 V < V _I < 40 V	4.9	5.0	5.1	V
Output Current Limitation	–	450	700	–	mA
Quiescent Current, I _Q = I _I – I _Q	I _Q = 1.0 mA	–	150	200	μA
Quiescent Current, I _Q = I _I – I _Q	I _Q = 250 mA	–	10	15	mA
Quiescent Current, I _Q = I _I – I _Q	I _Q = 400 mA	–	23	35	mA
Dropout Voltage	I _Q = 300 mA, V _{dr} = V _I – V _Q	–	250	500	mV
Load Regulation	I _Q = 5.0 mA to 400 mA	–30	15	30	mV
Line Regulation	ΔV = 8.0 V to 32 V, I _Q = 5.0 mA	–25	5.0	25	mV
Power Supply Ripple Rejection	f _r = 100 Hz, V _r = 0.5 V _{pp}	–	60	–	dB
Temperature Output Voltage Drift	–	–	0.5	–	mV/k

Reset Timing D and Output RO

Reset Switching Threshold	–	4.5	4.65	4.8	V
Reset Output Low Voltage	R _{ext} > 5.0 k, V _Q > 1.0 V	–	0.2	0.4	V
Reset Output Leakage Current	V _{ROH} = 5.0 V	–	0	10	μA
Reset Charging Current	V _D = 1.0 V	3.0	5.5	9.0	μA
Upper Timing Threshold	–	1.5	1.8	2.2	V
Lower Timing Threshold	–	0.2	0.4	0.7	V
Reset Delay Time	C _D = 47 nF	10	16	22	ms
Reset Reaction Time	C _D = 47 nF	–	1.5	4.0	μs

PIN DESCRIPTION

Pin No.	Symbol	Description
1	I	Input; Battery Supply Input Voltage. Bypass to ground with a ceramic capacitor.
2	RO	Reset Output; Open Collector Active Reset (accurate to I > 1.0 V).
3	GND	Ground; Pin 3 internally connected to heatsink.
4	D	Reset Delay; Connect to ground with a ≤ 22 μF capacitor, ESR < 5 Ω at 10 kHz.
5	Q	Output; ±2.0%, 450 mA output. Use 22 μF, ESR < 5.0 Ω to ground.

APPLICATION INFORMATION

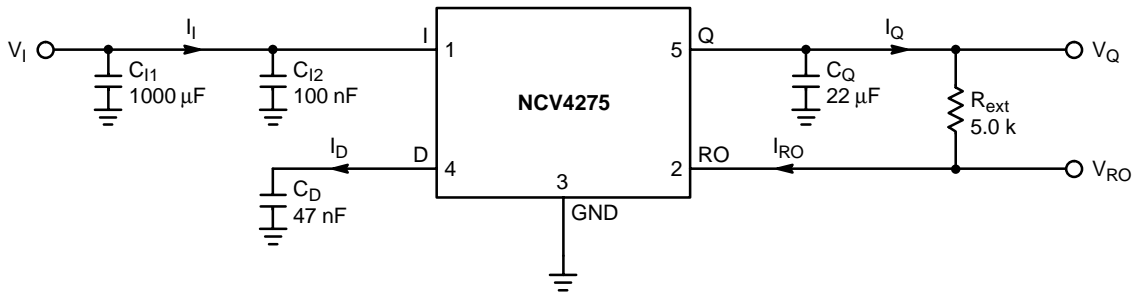


Figure 2. Test Circuit

Circuit Description

The error amplifier compares a temperature stable reference voltage to a voltage that is proportional to the output voltage (Q) (generated from a resistor divider) and drives the base of a series transistor via a buffer. Saturation control as a function of the load current prevents any oversaturation of the output power device preventing excessive substrate current (quiescent current).

Typical drop out voltage at 300 mA load is 250 mV, 500 mV maximum. Test voltage for drop out is 5 V input.

Stability Considerations

The input capacitors (C_{I1} and C_{I2}) are necessary for line influences. Using a resistor of approximately 1Ω in series with C_{I2} can solve potential oscillations due to stray inductance and capacitance.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 2 should work for most applications, however it is not necessarily the optimized solution. Stability is guaranteed for $C_Q > 22 \mu\text{F}$ and an $\text{ESR} \leq 5 \Omega$

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 3) is:

$$\text{PD}(\text{max}) = [\text{V}_{\text{IN}}(\text{max}) - \text{V}_{\text{OUT}}(\text{min})] \text{I}_{\text{OUT}}(\text{max}) + \text{V}_{\text{IN}}(\text{max}) \text{I}_{\text{q}} \quad (1)$$

where

- $\text{V}_{\text{IN}}(\text{max})$ is the maximum input voltage,
- $\text{V}_{\text{OUT}}(\text{min})$ is the minimum output voltage,
- $\text{I}_{\text{OUT}}(\text{max})$ is the maximum output current for the application,
- I_{Q} is the quiescent current the regulator consumes at $\text{I}_{\text{OUT}}(\text{max})$.

Once the value of $\text{P}_{\text{D}}(\text{max})$ is known, the maximum permissible value of $\text{R}_{\Theta\text{JA}}$ can be calculated:

$$\text{R}_{\Theta\text{JA}} = \frac{150^{\circ}\text{C} - \text{T}_{\text{A}}}{\text{P}_{\text{D}}} \quad (2)$$

The value of $\text{R}_{\Theta\text{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $\text{R}_{\Theta\text{JA}}$'s less than the calculated value in Equation 2 will keep the die temperature below 150°C .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

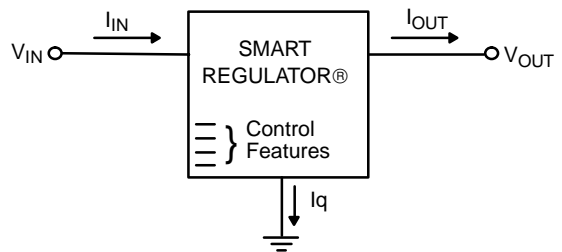


Figure 3. Single Output Regulator with Key Performance Parameters Labeled

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

- $R_{\theta JC}$ is the junction-to-case thermal resistance,
- $R_{\theta CS}$ is the case-to-heatsink thermal resistance,
- $R_{\theta SA}$ is the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

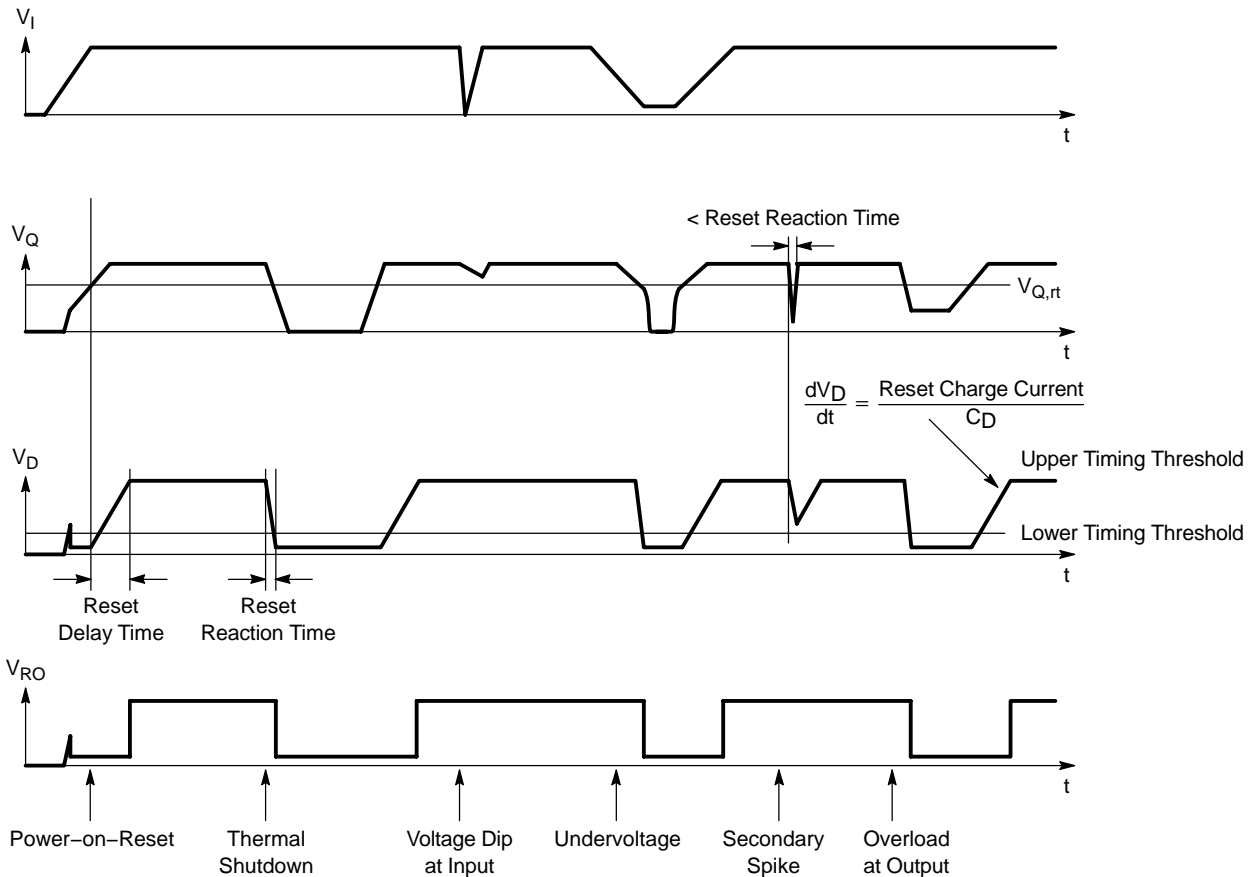
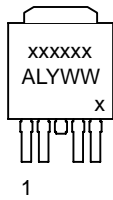


Figure 4. Reset Timing

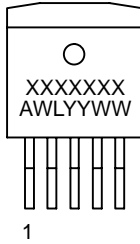
NCV4275

MARKING DIAGRAMS

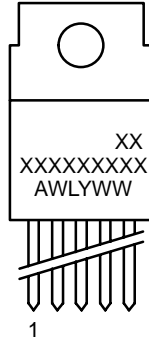
DPAK
DT SUFFIX
CASE 175AA



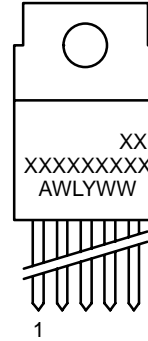
D²PAK
DS SUFFIX
CASE 936AC



TO-220
T SUFFIX
CASE 314D



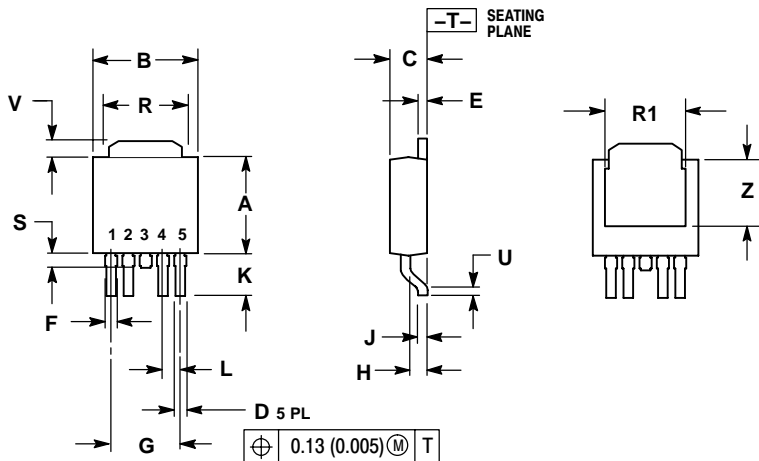
TO-220
TV SUFFIX
CASE 314K



XXX... = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

DPAK 5 CENTER LEAD CROP
DT SUFFIX
CASE 175AA-01
ISSUE O



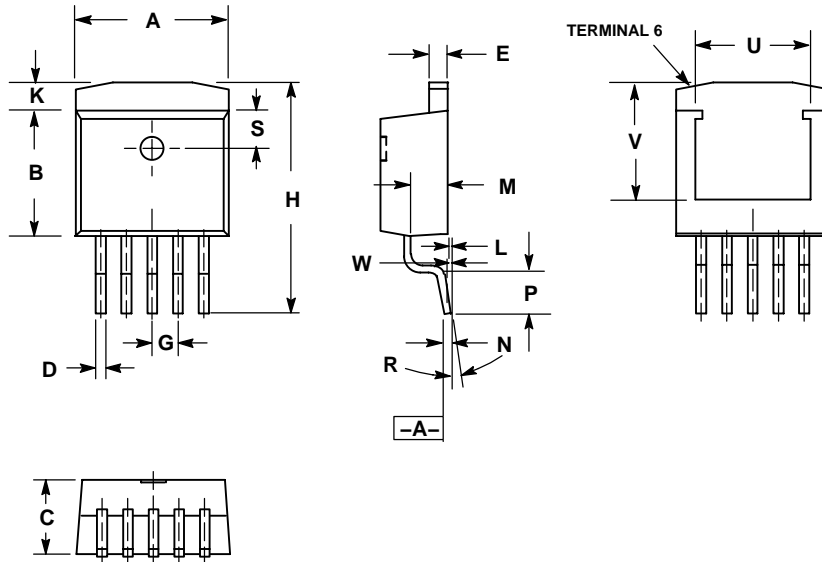
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180 BSC		4.56 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045 BSC		1.14 BSC	
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

NCV4275

PACKAGE DIMENSIONS

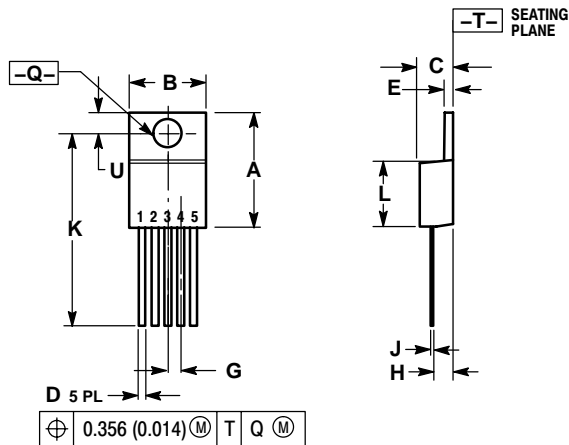
D²PAK
5 LEAD
DS SUFFIX
CASE 936AC-01
ISSUE O



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
 4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
 5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.330	0.340	8.38	8.64
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.067 REF		1.70 REF	
H	0.580	0.620	14.73	15.75
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.098	0.108	2.49	2.74
N	0.017	0.023	0.43	0.58
P	0.090	0.110	2.29	2.79
R	0°	8°	0°	8°
S	0.095	0.105	2.41	2.67
U	0.30 REF		7.62 REF	
V	0.305 REF		7.75 REF	
W	0.010		0.25	

TO-220
FIVE LEAD STRAIGHT
T SUFFIX
CASE 314D-04
ISSUE E



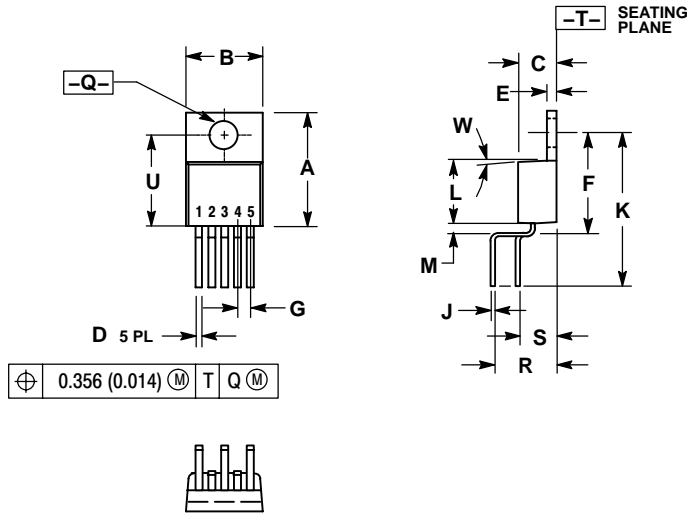
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 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

NCV4275

PACKAGE DIMENSIONS


TO-220 FIVE LEAD VERTICAL TV SUFFIX CASE 314K-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D, INCLUDING PROTRUSION, SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.78	10.54
C	0.160	0.190	4.06	4.83
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.530	0.545	13.46	13.84
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.321	0.337	8.15	8.56
M	0.063	0.078	1.60	1.98
Q	0.146	0.156	3.71	3.96
R	0.271	0.321	6.88	8.15
S	0.146	0.196	3.71	4.98
U	0.460	0.475	11.68	12.07
W	5°		5°	

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