512KX8 Bit CMOS Pseudo Static RAM

FEATURES

- **Fast Access Time:**
  - **— $\overline{CE}$ Access Time: 80,100,120ns (Max.)**
  - **— Cycle Time: Random Read/Write Cycle Time 160, 180, 210ns (Max.)**
- **Low Power Dissipation: 200mW typ. (Active) 0.5mW typ. (Standby)**
- **Single 5V±10% Power Supply**
- **TTL compatible Inputs and outputs**
- **Non multiplexed Address**
- **Three State Output**
- **2048 Refresh Cycles/32ms**
- **Self Refresh Current: 1mA/200μA (L-version) /100μA (LL-version)**
- **Data Retention Supply Voltage: 3.0V to 5.5V**
- **Battery Back-up Capability with KM658512L-L**
- **32-Pin JEDEC Standard Plastic Package**
  - **— DIP (600mil)**
  - **— SOP (525mil)**
  - **— TSOP (400mil)**

GENERAL DESCRIPTION

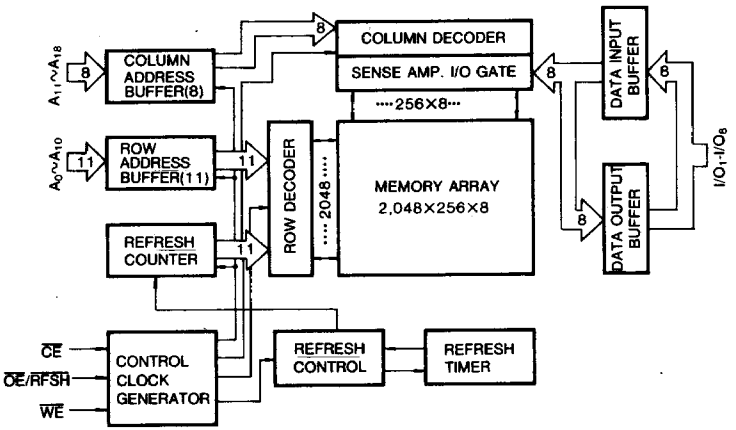
The KM658512/L/L-L is a 4,194,304-bit high-speed Pseudo Static Random Access Memory organized as 524,288 words by 8 bits, fabricated using advanced CMOS technology.

The device, utilizing one transistor DRAM cell with on-chip refresh timer, provides the advantages of DRAM (Low cost, High density) and Static RAM (Low standby power and ease of use).

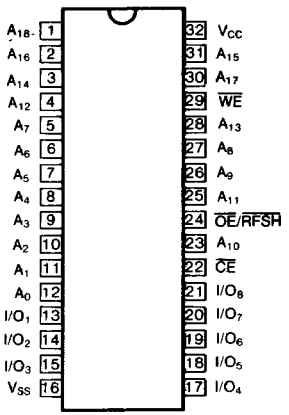
The pin-out of KM658512/L/L-L follow the JEDEC standard for Static RAM with the addition of $\overline{RFSH}$ input. The $\overline{RFSH}$ input allows two types of refresh operation; Auto Refresh and Self Refresh.
The $\overline{CE}$ only Refresh is also supported.

The KM658512/L/L-L supports a write function similiar to static RAM in that the input data is written into the memory cell at the rising edge of $\overline{WE}$, thus simplifying the interface to standard microprocessors.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin Name	Pin Function
A0-A18	Address Inputs
$\overline{WE}$	Write Enable
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh
$\overline{CE}$	Chip Enable
I/O1-I/O8	Data Inputs/Outputs
VCC	Power supply
VSS	Ground