

# Low-Voltage CMOS Octal Registered Transceiver With Dual Output and Clock Enables

## With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX2952 is a high performance, non-inverting octal registered transceiver operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX2952 inputs to be safely driven from 5V devices. The MC74LCX2952 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

Two 8-bit back to back registers store data from either of two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CAB, CBA) provided that the Clock Enable (CEAB, CEBA) is Low. The data is then presented at the 3-state output buffers, but is only accessible when the Output Enable (OEAB, OEBA) is Low. The operation of the MC74LCX2952 is symmetrical — A inputs to B outputs occurs in the same manner as B inputs to A outputs.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I<sub>OFF</sub> Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVC MOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (10 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

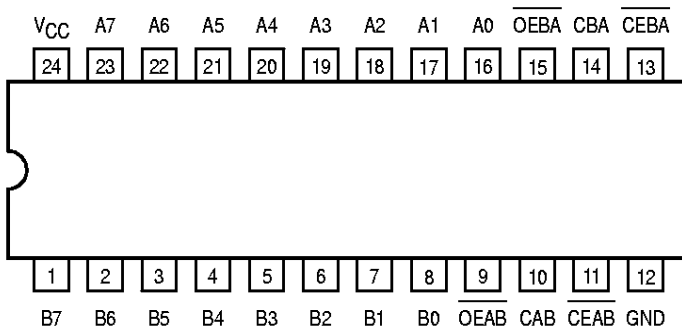


Figure 1. 24-Lead Pinout (Top View)

**MC74LCX2952**

**LCX**

**LOW-VOLTAGE CMOS  
OCTAL REGISTERED  
TRANSCEIVER**



**DW SUFFIX**  
24-LEAD PLASTIC SOIC WIDE PACKAGE  
CASE 751E-04



**SD SUFFIX**  
24-LEAD PLASTIC SSOP PACKAGE  
CASE 940D-03



**DT SUFFIX**  
24-LEAD PLASTIC TSSOP PACKAGE  
CASE 948H-01

**PIN NAMES**

Pins	Function
A0-A7	Side A Inputs/Outputs
B0-B7	Side B Inputs/Outputs
CAB, CBA	Clock Pulse Inputs
CEAB, CEBA	Clock Enable Inputs
OEAB, OEBA	Output Enable Inputs





## FUNCTION TABLE

Inputs						Data Ports		Operating Mode
OEAB	OEBA	CEAB	CEBA	CAB	CBA	An	Bn	
H	H					Input	Input	
		l	l	↑	↑	X	X	Load Register; Disable Outputs
				⊕	⊕	X	X	Hold; Disable Outputs
		h	h	X	X	X	X	Hold; Disable Outputs
L	H					Input	Output	
		l	X	↑	X	l h	L H	Load A to B Register; Read B Output
				⊕	X	X	QA	Hold; Read B Output
		h	X	X	X	QA	Hold; Read B Output	
H	L					Output	Input	
		X	l	X	↑	L H	l h	Load B to A Register; Read A Output
				X	⊕	QB	X	Hold; Read A Output
		X	h	X	X	QB	X	Hold; Read A Output

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; X = Don't Care; ↑ = Low-to-High Clock Transition; ⊕ = NOT Low-to-High Clock Transition; QA = A input storage register; QB = B input storage register; \* = The clocks are not internally gated with either the Output Enables or the Source Inputs. Therefore, data at the A or B ports may be clocked into the storage registers, at any time. For I<sub>CC</sub> reasons, Do Not Float Inputs.

## ABSOLUTE MAXIMUM RATINGS\*

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating	3.3	3.6	V
		Data Retention Only	1.5	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub> 5.5	V
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
ΔV/ΔV	Input Transition Rise or Fall Rate, V <sub>I(N)</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>I</sub> ≤ 5.5V		±5.0	μA
I <sub>OZ</sub>	3-State Output Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 0V ≤ V <sub>O</sub> ≤ 5.5V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		10	μA
I <sub>CC</sub>	Quiescent Supply Current	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = GND or V <sub>CC</sub>		10	μA
		2.7 ≤ V <sub>CC</sub> ≤ 3.6V; 3.6 ≤ V <sub>I</sub> or V <sub>O</sub> ≤ 5.5V		±10	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	2.7 ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>IH</sub> = V <sub>CC</sub> - 0.6V		500	μA

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

**AC CHARACTERISTICS** (Note 3.;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 3.0\text{V to } 3.6\text{V}$		$V_{CC} = 2.7\text{V}$		
			Min	Max	Min	Max	
$f_{\text{max}}$	Clock Pulse Frequency	3	150				MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay Clock to Output	1	1.5	8.0	1.5	9.0	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time to High and Low Level	2	1.5	8.0	1.5	9.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time From High and Low Level	2	1.5	6.0	1.5	7.0	ns
$t_s$	Setup Time, HIGH to LOW Data to Clock	3	2.5		2.5		ns
$t_h$	Hold Time, HIGH to LOW Data to Clock	3	1.5		1.5		ns
$t_s$	Setup Time, HIGH to LOW CE <sub>xx</sub> to Clock	3	2.5		2.5		ns
$t_h$	Hold Time, HIGH to LOW CE <sub>xx</sub> to Clock	3	1.5		1.5		ns
$t_w$	Clock Pulse Width, HIGH or LOW	3	3.3		3.3		ns
$t_{\text{OSHL}}$ $t_{\text{OSLH}}$	Output-to-Output Skew (Note 4.)			1.0			ns

3. These AC parameters are preliminary and may be modified prior to release. The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.
4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ); parameter guaranteed by design.

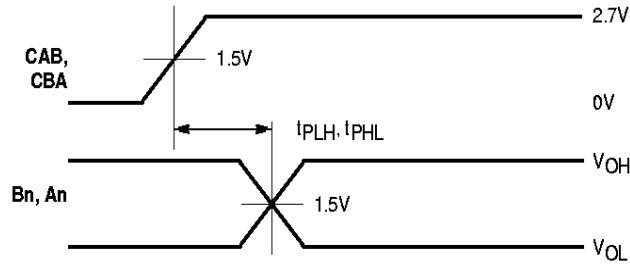
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{\text{OLP}}$	Dynamic LOW Peak Voltage (Note 5.)	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{\text{IH}} = 3.3\text{V}$ , $V_{\text{IL}} = 0\text{V}$		0.8		V
$V_{\text{OLV}}$	Dynamic LOW Valley Voltage (Note 5.)	$V_{CC} = 3.3\text{V}$ , $C_L = 50\text{pF}$ , $V_{\text{IH}} = 3.3\text{V}$ , $V_{\text{IL}} = 0\text{V}$		0.8		V

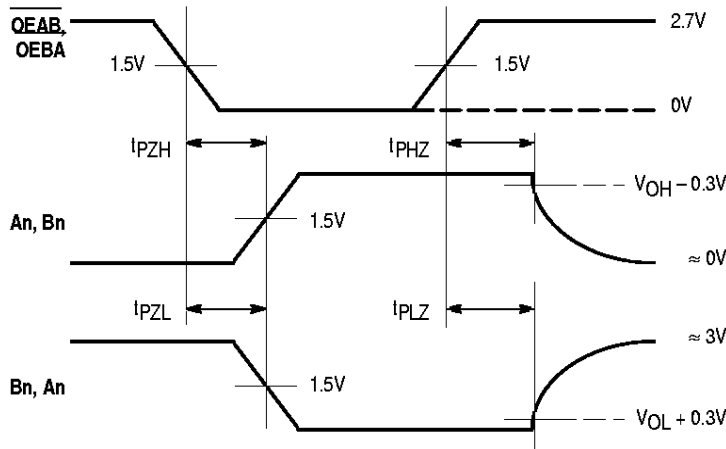
5. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

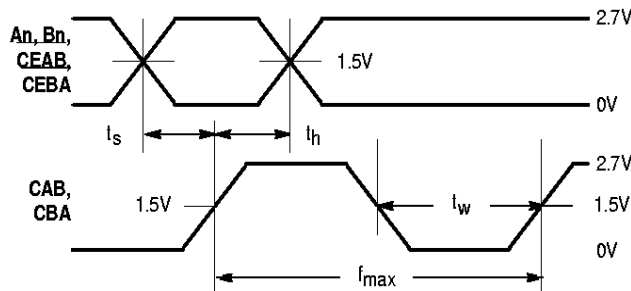
Symbol	Parameter	Condition	Typical	Unit
$C_{\text{IN}}$	Input Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	7	pF
$C_{\text{I/O}}$	Input/Output Capacitance	$V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	8	pF
$C_{\text{PD}}$	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}$ , $V_I = 0\text{V}$ or $V_{CC}$	25	pF



**WAVEFORM 1 – Cxx to An/Bn PROPAGATION DELAYS**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

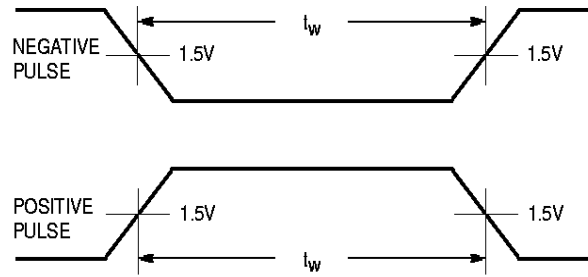


**WAVEFORM 2 – OExx to An/Bn OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



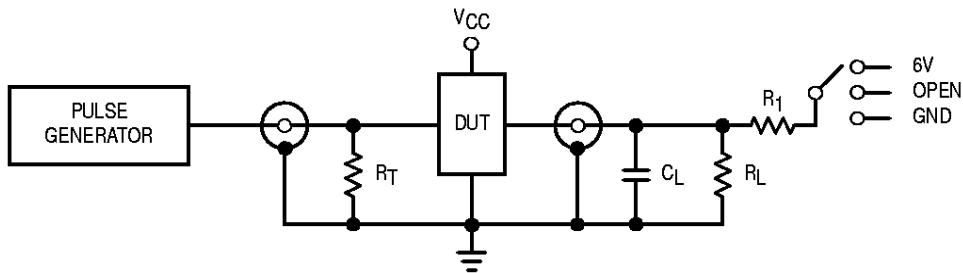
**WAVEFORM 3 – Cxx MINIMUM PULSE WIDTH, An/Bn/CExx to Cxx SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$  except when noted

**Figure 3. AC Waveforms**



**WAVEFORM 4 – INPUT PULSE DEFINITION**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90% of 0V to 2.7V

**Figure 4. AC Waveforms (continued)**



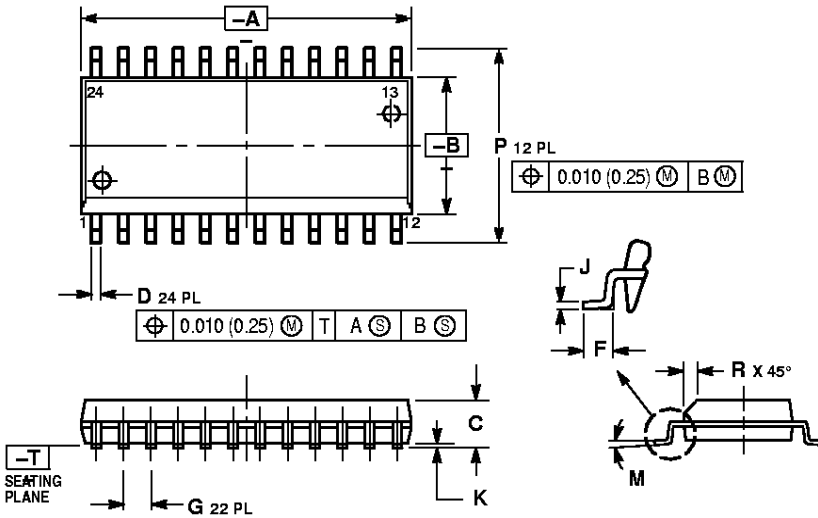
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 5. Test Circuit**

OUTLINE DIMENSIONS

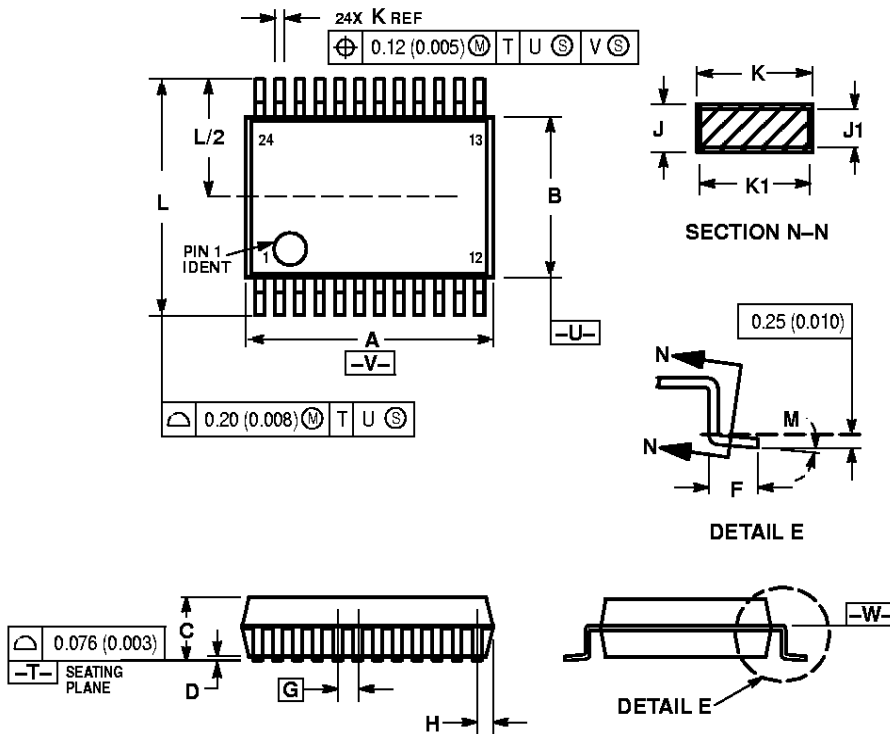
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751E-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SD SUFFIX  
PLASTIC SSOP PACKAGE  
CASE 940D-03  
ISSUE B



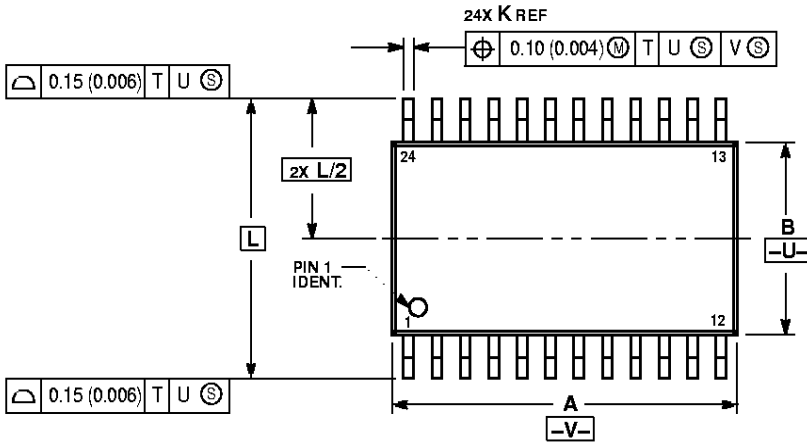
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.07	8.33	0.317	0.328
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.44	0.60	0.017	0.024
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

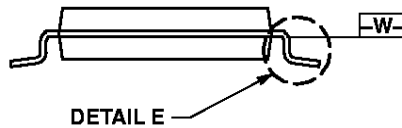
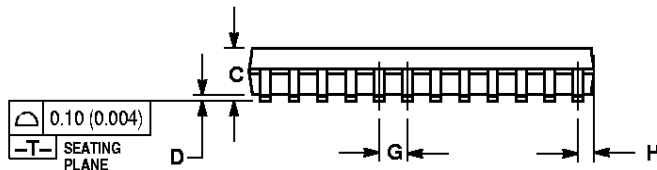


OUTLINE DIMENSIONS

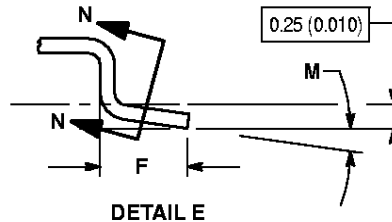
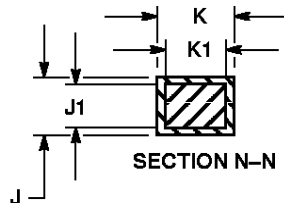
DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948H-01  
 ISSUE O




- NOTES:
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  - 2 CONTROLLING DIMENSION: MILLIMETER.
  - 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



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