National Semiconductor

PRELIMINARY

DM54ALS1641/DM74ALS1641, DM54ALS1642/DM74ALS1642, DM54ALS1644/DM74ALS1644 Octal Bus Transceivers

General Description

These advanced low power Schottky TRI-STATE® octal bus transceivers are designed to provide high speed bidirectional communication between data buses. The output characteristics of the circuits are low enough impedance to drive transmission lines terminated down to 133Ω. The input characteristics of the circuits are high impedance so they will not significantly load the transmission line. These devices allow 8-bit wide bidirectional data transmission controlled by the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to isolate both buses. The 'ALS1641, 'ALS1642 and 'ALS1644 have open-collector outputs on both the A bus and the B bus.

Features

- PNP input design reduces input loading
- Switching performance is guaranteed over full temperature and V_{CC} supply range
- Switching response specified into 500Ω and 50 pF
- Advanced low power oxide-isolated ion-implanted Schottky TTL process
- Improved switching performance with less power dissipation compared with 54/74LS counterpart
- Functional and pin compatible with 54/74LS counterpart
- Low power versions of 'ALS641, 642, 644
- Glitch-free bus during power-up/down

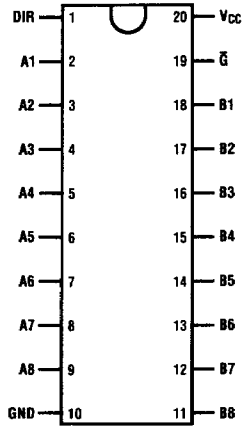
Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6268-1

54ALS1641, 1642, 1644 (J)
74ALS1641, 1642, 1644 (N)

Function Table

Control Inputs		Operation		
$\overline{G}$	DIR	'ALS1642	'ALS1641	'ALS1644
L	L	$\overline{B}$ data to A bus	B data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	A data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation	Isolation

Circuit Configurations

Device	Output	Logic
'ALS1641	Open-Collector	True
'ALS1642	Open-Collector	Inverting
'ALS1644	Open-Collector	True and Inverting

Recommended Operating Conditions

Symbol	Parameter	DM54ALS1641 DM54ALS1642 DM54ALS1644			DM74ALS1641 DM74ALS1642 DM74ALS1644			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			8			16	mA
	74ALS-1						24	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise specified)

Symbol	Parameter	Conditions	DM54ALS			DM74ALS			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA			−1.5			−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V							
		I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	V
	DM74ALS-1	I_{OL} = 48 mA					0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_I = 7V			0.1			0.1	mA
		V_I = 5.5V (I/O Port)			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_I = 2.7V			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V			−0.1			−0.1	mA
		(I/O Port)			−0.1			−0.1	mA
I_{OH}	High Level Output Current	V_{CC} = 4.5V, V_{OH} = 5.5V			0.1			0.1	mA
I_{CC}	Supply Current	V_{CC} = 5.5V							
	ALS1641			23			23		mA
	ALS1642			20			20		mA
	ALS1644			22			22		mA

'ALS1641 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1641			DM74ALS1641			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A		22			22		ns
t_{PHL}				14			14		ns
t_{PLH}	$\overline{G}$ or DIR	A or B		26			26		ns
t_{PHL}				26			26		ns

'ALS1642 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1642			DM74ALS1642			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A or B	B or A		25			25		ns
t_{PHL}				13			13		ns
t_{PLH}	$\overline{G}$ or DIR	A or B		29			29		ns
t_{PHL}				29			29		ns

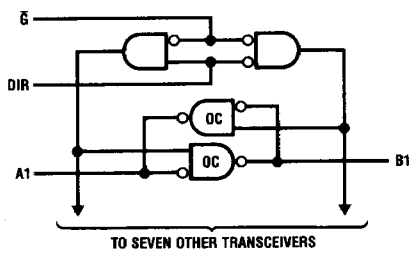
'ALS1644 Switching Characteristics (Note 1)

Parameter	From (Input)	To (Output)	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max						Units
			DM54ALS1644			DM74ALS1644			
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	B		27			27		ns
t_{PHL}				19			19		ns
t_{PLH}	B	A		24			24		ns
t_{PHL}				17			17		ns
t_{PLH}	$\overline{G}$	A		30			30		ns
t_{PHL}				27			27		ns
t_{PLH}	$\overline{G}$	B		24			24		ns
t_{PHL}				30			30		ns
t_{PLH}	DIR	A		30			30		ns
t_{PHL}				27			27		ns
t_{PLH}	DIR	B		24			24		ns
t_{PHL}				30			30		ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagrams

'ALS1641



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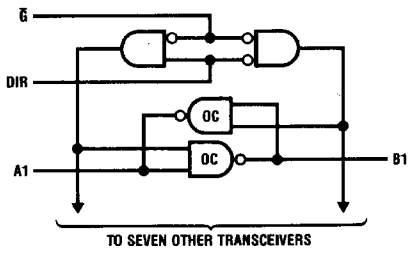
'ALS1642



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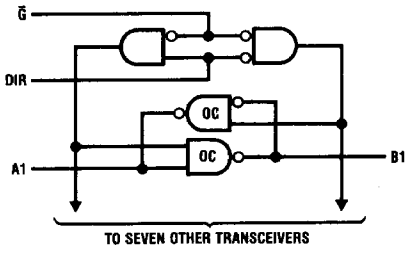
'ALS1644



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OC denotes open-collector outputs