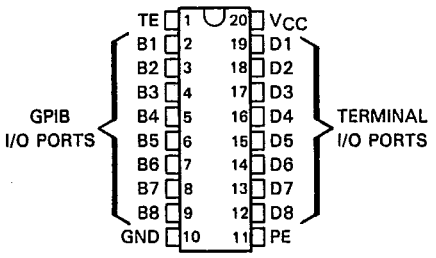
SN75ALS163
OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

D2611, JUNE 1986—REVISED SEPTEMBER 1989

- 8-Channel Bidirectional Transceivers
- High-Speed Advanced Low-Power Schottky Circuitry
- Low Power Dissipation . . . 46 mW Max per Channel
- Fast Propagation Times . . . 20 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device Is Powered Down (V_{CC} = 0)
- Power-Up/Power-Down Protection (Glitch-Free)

DW, J, OR N PACKAGE
(TOP VIEW)



description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, Advanced Low-Power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If Talk Enable (TE) is high, these outputs have the characteristics of open-collector outputs when Pullup Enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Output glitches during power-up and power-down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75ALS163 is characterized for operation from 0°C to 70°C.

FUNCTION TABLES

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

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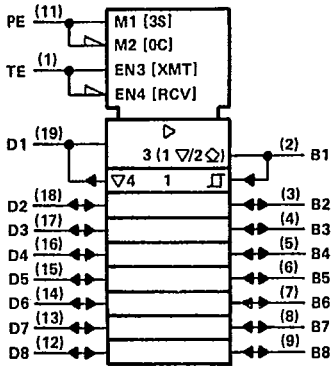
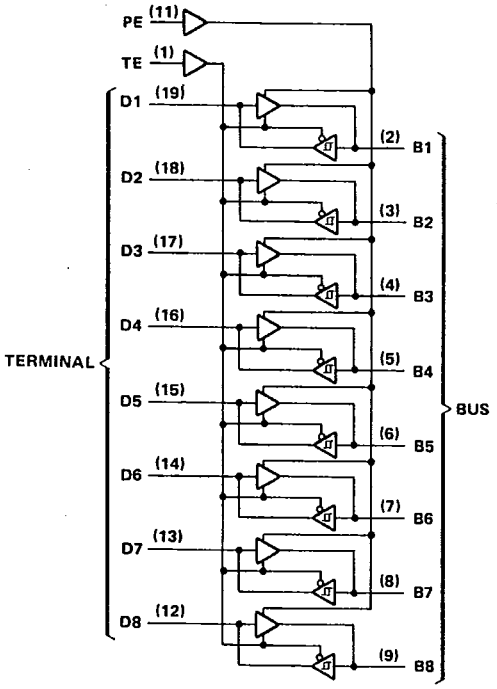
logic symbol†



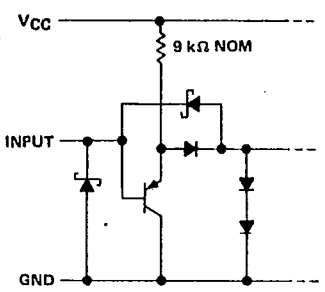
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs.
⏢ Designates open-collector outputs.

logic diagram (positive logic)

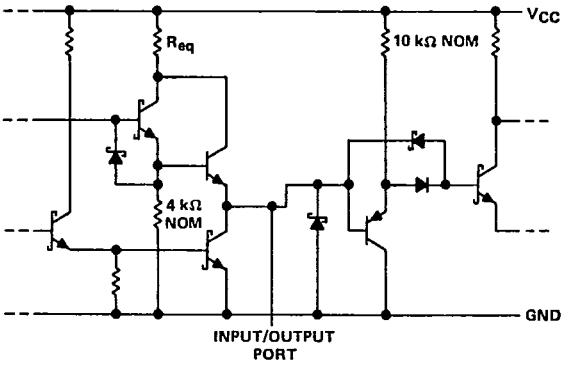


schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16) inch from the case for 60 seconds: J package . . . . . 300°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: DW or N package . . . . 260°C

NOTE: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
J	1025 mW	8.2 mW/°C	656 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature range, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus			0.4	0.65		V
V_{OH}‡	High-level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.35	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, D and TE at 2 V	PE at 0.8 V,			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal, PE, or TE	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Terminal outputs low and enabled		42	65	mA
				Bus outputs low and enabled		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0, f = 1 MHz	$V_{I/O}$ = 0 to 2 V,		30		pF

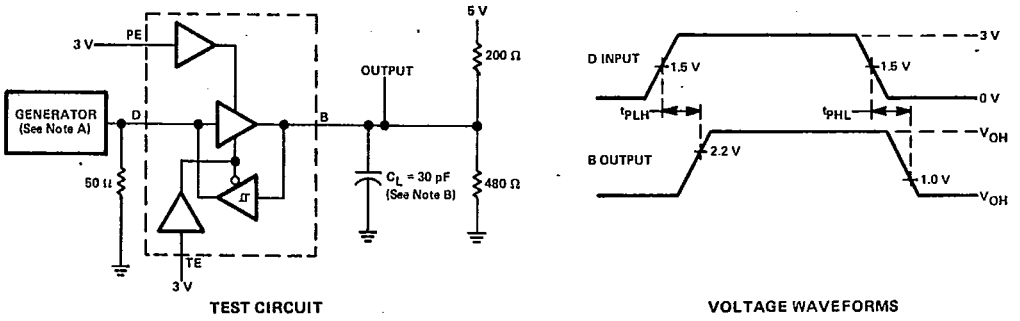
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics over recommended range of operating free-air temperature (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP§	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	C_L = 15 pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	C_L = 15 pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Bus	C_L = 15 pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

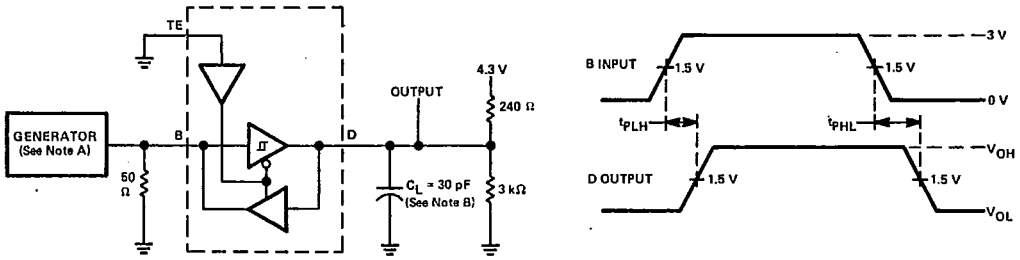
§All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



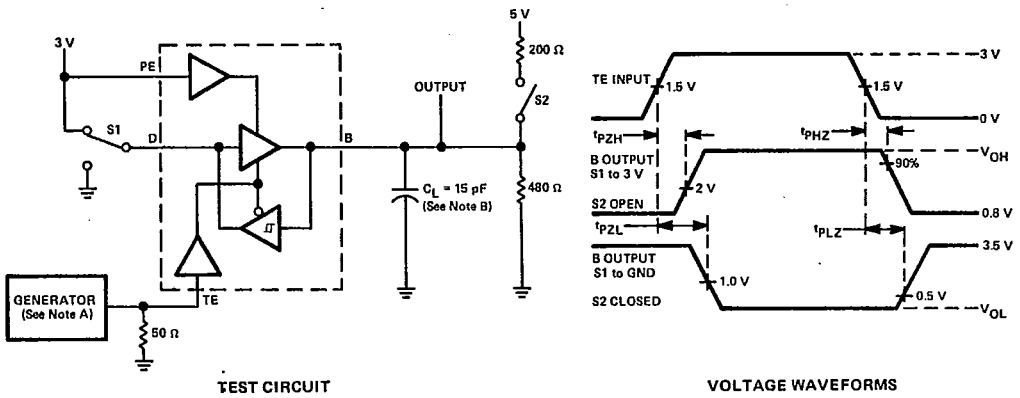
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1. TERMINAL-TO-BUS PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 2. BUS-TO-TERMINAL PROPAGATION DELAY TIMES

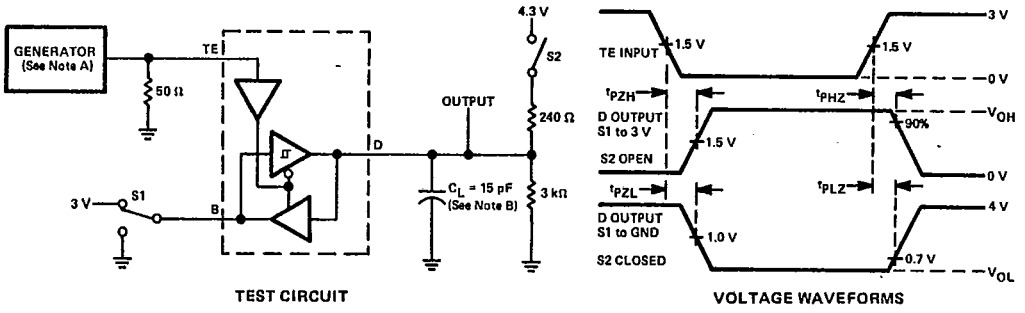


TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3. TE-TO-BUS ENABLE AND DISABLE TIMES

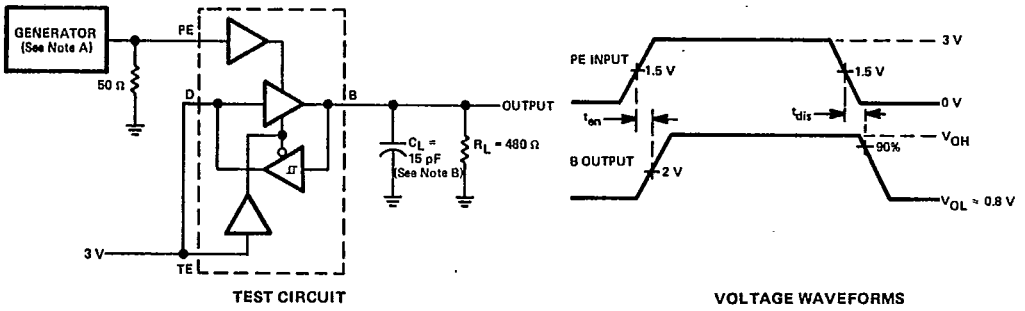
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4. TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5. PE-TO-BUS PULLUP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

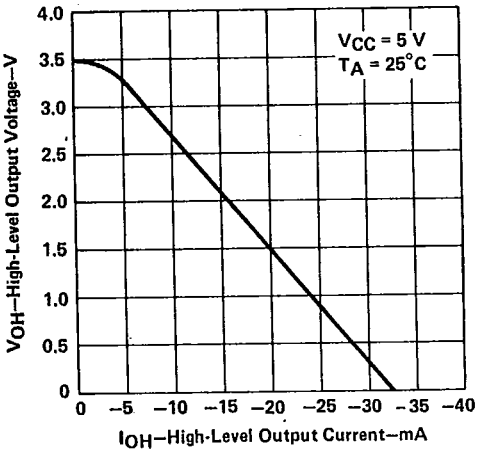

FIGURE 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

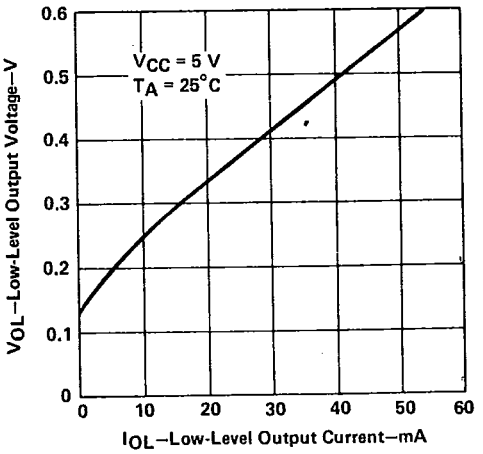

FIGURE 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

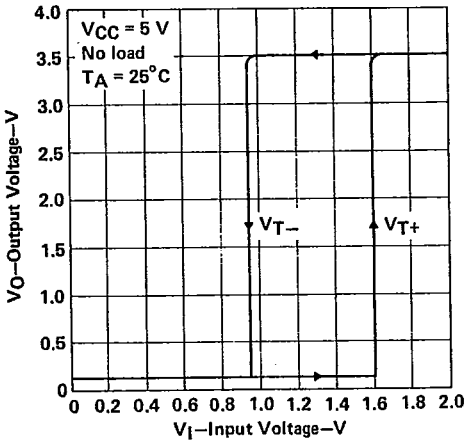

FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

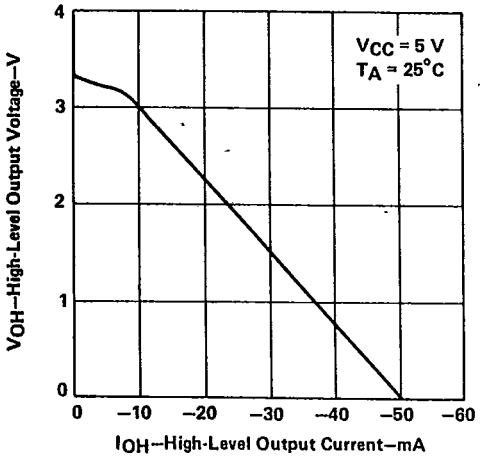

FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

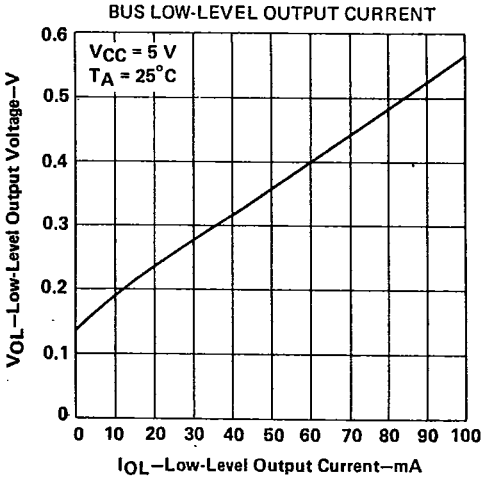

FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

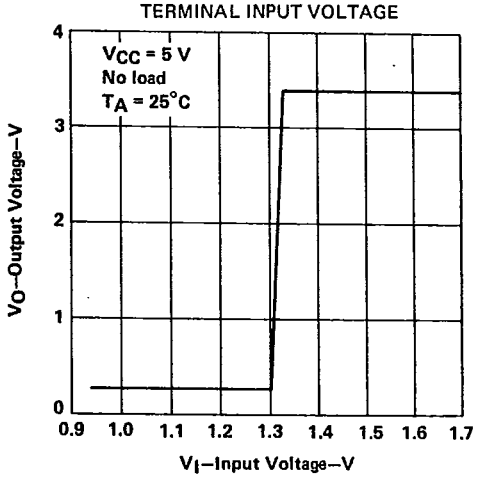

FIGURE 11

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