Dual/Quad Low Noise, High Speed Precision Op Amps

FEATURES

- 100% Tested Low Voltage Noise 2.7nV/√Hz Typ, 4.2nV/√Hz Max
- Slew Rate 4.5V/µs Typ
- Gain Bandwidth Product 12.5MHz Typ
- Offset Voltage, Prime Grade 70µV Max; Low Grade 100µV Max
- High Voltage Gain 5 Million Min
- Supply Current Per Amplifier 2.75mA Max
- Common Mode Rejection 112dB Min
- Power Supply Rejection 116dB Min
- Available in 8-Pin SO Package

APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Infrared Detectors

DESCRIPTION

The LT1124 dual and LT1125 quad are high performance op amps that offer higher gain, slew rate, and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the LT1124/LT1125 have lower I_B and I_{OS} than the OP-27; lower V_{OS} and noise than the OP-270/OP-470.

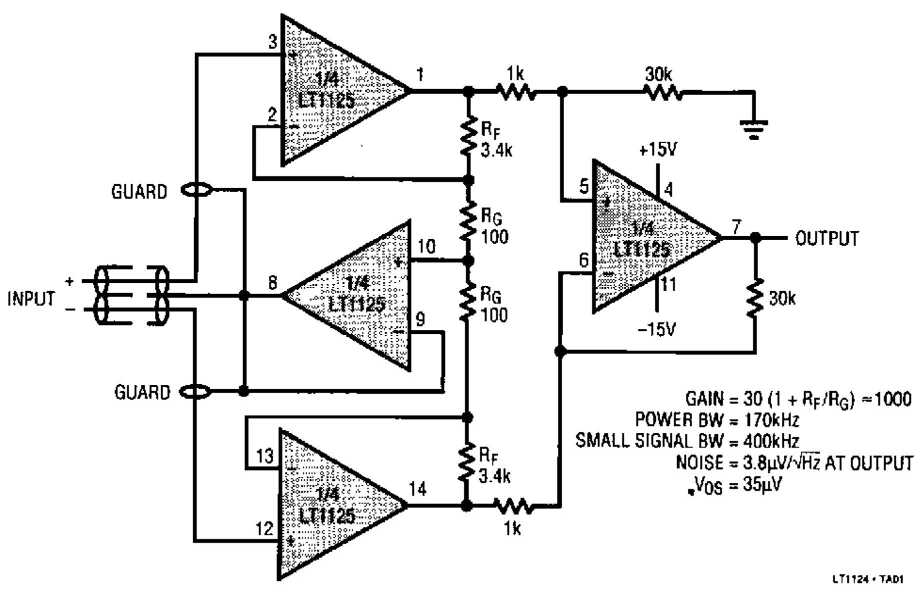
In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain bandwidth, and 1kHz noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1124C and the LT1125C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

Power consumption of the LT1124 is one half of two OP-27s. Low power and high performance in an 8-pin SO package make the LT1124 a first choice for surface mounted systems and where board space is restricted.

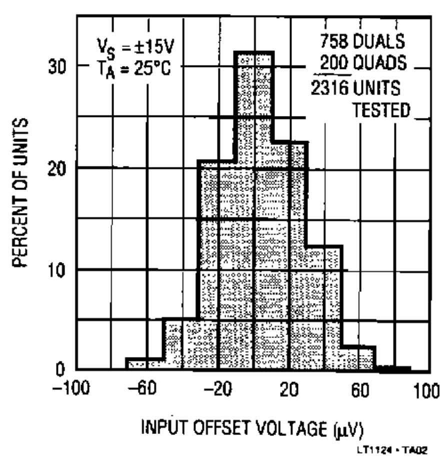
For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the LT1126/LT1127 data sheet.

Protected by U.S. patents 4,775,884 and 4,837,496.

Instrumentation Amplifier with Shield Driver



Input Offset Voltage Distribution (All Packages, LT1124 and LT1125)

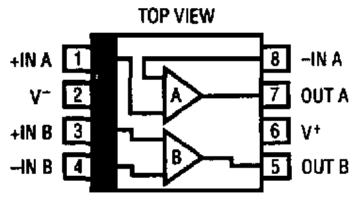


ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Input Voltages .... Equal to Supply Voltage
Output Short Circuit Duration .... Indefinite
Differential Input Current (Note 5) .... ±25mA
Lead Temperature (Soldering, 10 sec.) .... 300°C

Operating Temperature Range
LT1124AM/LT1124M
LT1125AM/LT1125M .... –55°C to 125°C
LT1124AC/LT1124C
LT1125AC/LT1125C .... –40°C to 85°C
Storage Temperature Range
All Grades .... –65°C to 150°C

PACKAGE/ORDER INFORMATION

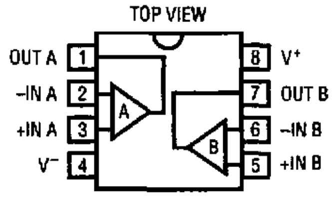


S8 PACKAGE
8-LEAD PLASTIC SOIC

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN DIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS

LT1124 • POI01

ORDER PART NUMBER
LT1124CS8
PART MARKING
1124

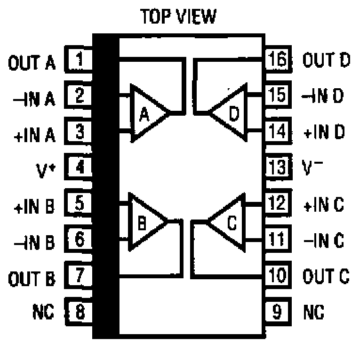


J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

LT1124 • POI02

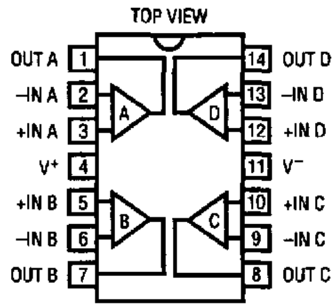
ORDER PART NUMBER
LT1124AMJ8
LT1124MJ8
LT1124CJ8
LT1124ACN8
LT1124CN8



S PACKAGE
16-LEAD PLASTIC SOL

LT1124 • POI03

ORDER PART NUMBER
LT1125CS



J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

LT1124 • POI04

ORDER PART NUMBER
LT1125AMJ
LT1125MJ
LT1125CJ
LT1125ACN
LT1125CN

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1124AM/AC LT1125AM/AC MIN	TYP	MAX	LT1124M/C LT1125M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124		20	70		25	100	µV
		LT1125		25	90		30	140	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		µV/Mo
I_{OS}	Input Offset Current	LT1124		5	15		6	20	nA
		LT1125		6	20		7	30	nA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1124AM/AC LT1125AM/AC MIN	TYP	MAX	LT1124M/C LT1125M/C MIN	TYP	MAX	UNITS
I_B	Input Bias Current			±7	±20		±8	±30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 7 and 8)		70	200		70		nVp-p
	Input Noise Voltage Density	f_O = 10Hz (Note 3)		3.0	5.5		3.0	5.5	nV/√Hz
		f_O = 1000Hz (Note 2)		2.7	4.2		2.7	4.2	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz		1.3			1.3		pA/√Hz
		f_O = 1000Hz		0.3			0.3		pA/√Hz
V_{CM}	Input Voltage Range		±12.0	±12.8		±12.0	±12.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	112	126		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	116	126		110	124		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm10V$	5.0	17.0		3.0	15.0		V/µV
		$R_L \geq 2k\Omega$, $V_O = \pm10V$	2.0	4.0		1.5	3.0		V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±13.0	±13.8		±12.5	±13.8		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	3.0	4.5		2.7	4.5		V/µs
GBW	Gain-Bandwidth Product	f_O =100kHz (Note 2)	9.0	12.5		8.0	12.5		MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		75			75		Ω
I_S	Supply Current Per Amplifier			2.3	2.75		2.3	2.75	mA
	Channel Separation	$f \leq 10Hz$ (Note 8) $V_O = \pm10V$, $R_L = 2k\Omega$	134	150		130	150		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1124AM LT1125AM MIN	TYP	MAX	LT1124M LT1125M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124	●		50	170		60	250	µV
		LT1125	●		55	190		70	290	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	µV/°C
I_{OS}	Input Offset Current	LT1124	●		18	45		20	60	nA
		LT1125	●		18	55		20	70	nA
I_B	Input Bias Current		●		±18	±55		±20	±70	nA
V_{CM}	Input Voltage Range		●	±11.3	±12		±11.3	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	110	122		104	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm10V$	●	3.0	10.0		2.0	10.0		V/µV
		$R_L \geq 2k\Omega$, $V_O = \pm10V$	●	1.0	3.0		0.7	2.0		V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	●	2.3	3.8		2.0	3.8		V/µs
I_S	Supply Current Per Amplifier		●		2.5	3.25		2.5	3.25	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1124AC LT1125AC MIN	TYP	MAX	LT1124C LT1125C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124	●		35	120		45	170	μV
		LT1125	●		40	140		50	210	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1124	●		6	25		7	35	nA
		LT1125	●		7	35		8	45	nA
I_B	Input Bias Current		●		±8	±35		±9	±45	nA
V_{CM}	Input Voltage Range		●	±11.5	±12.4		±11.5	±12.4		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.5V$	●	109	125		102	122		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	112	125		107	122		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm10V$	●	4.0	15.0		2.5	14.0		V/μV
		$R_L \ge 2k\Omega$, $V_O = \pm10V$	●	1.5	3.5		1.0	2.5		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.7		±12.0	±13.7		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Notes 2 and 6)	●	2.6	4.0		2.4	4.0		V/μs
I_S	Supply Current Per Amplifier		●		2.4	3.0		2.4	3.0	mA

2

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 9)

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1124AC LT1125AC MIN	TYP	MAX	LT1124C LT1125C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124	●		40	140		50	200	μV
		LT1125	●		45	160		55	240	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1124	●		15	40		17	55	nA
		LT1125	●		15	50		17	65	nA
I_B	Input Bias Current		●		±15	±50		±17	±65	nA
V_{CM}	Input Voltage Range		●	±11.4	±12.2		±11.4	±12.2		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.4V$	●	107	124		101	121		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	111	124		106	121		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm10V$	●	3.5	12.0		2.2	12.0		V/μV
		$R_L \ge 2k\Omega$, $V_O = \pm10V$	●	1.2	3.2		0.8	2.3		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Note 6)	●	2.4	3.9		2.1	3.9		V/μs
I_S	Supply Current Per Amplifier		●		2.4	3.25		2.4	3.25	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1125's (or 100 LT1124's) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is 100% tested for each individual amplifier.

Note 3: This parameter is sample tested only.

Note 4: This parameter is not 100% tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

Note 6: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

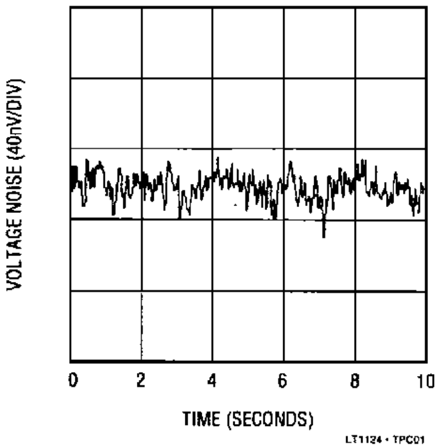
Note 7: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 data sheets.

Note 8: This parameter is guaranteed but not tested.

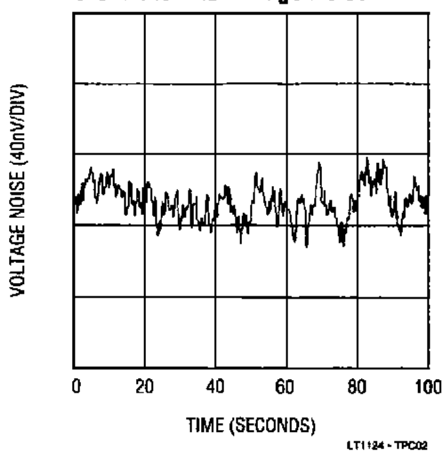
Note 9: The LT1124/LT1125 are not tested and are not quality-assurance-sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

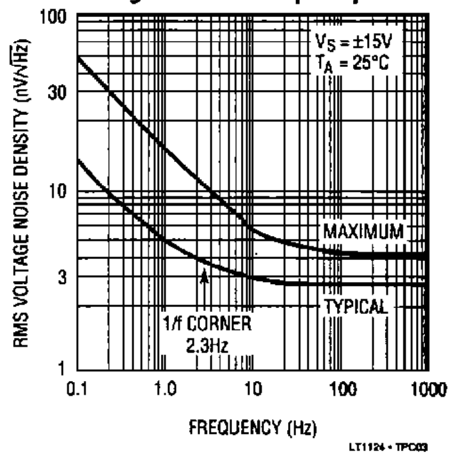
0.1Hz to 10Hz Voltage Noise



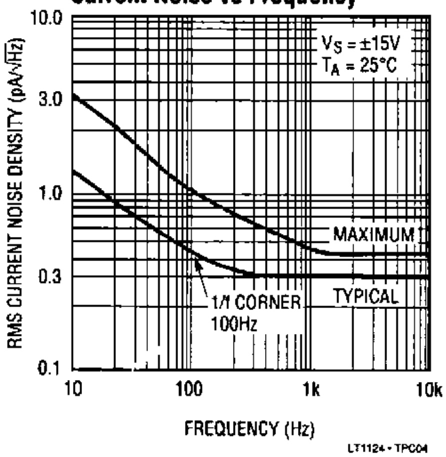
0.01Hz to 1Hz Voltage Noise



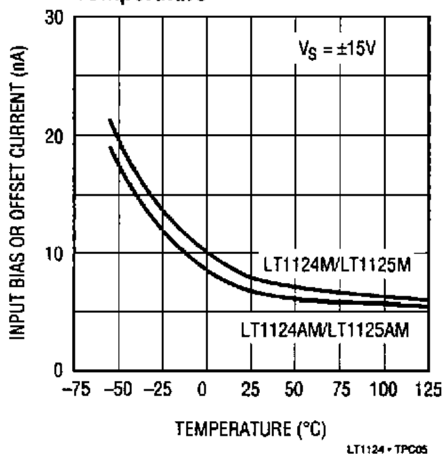
Voltage Noise vs Frequency



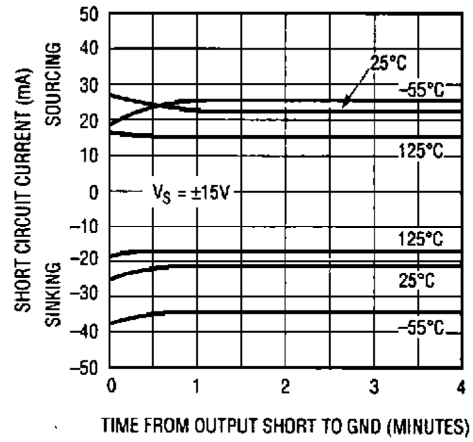
Current Noise vs Frequency



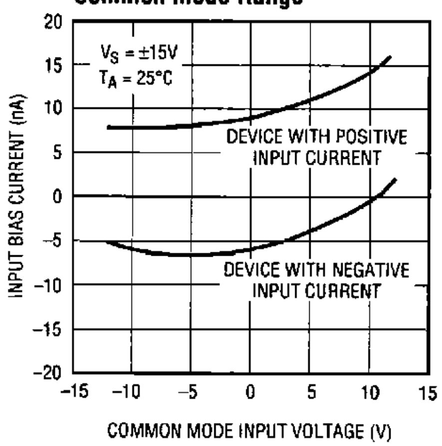
Input Bias or Offset Current vs Temperature



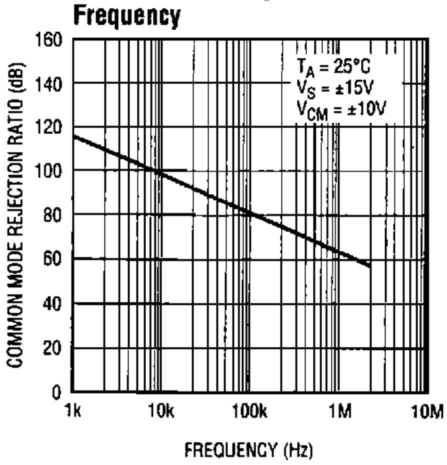
Output Short Circuit Current vs Time



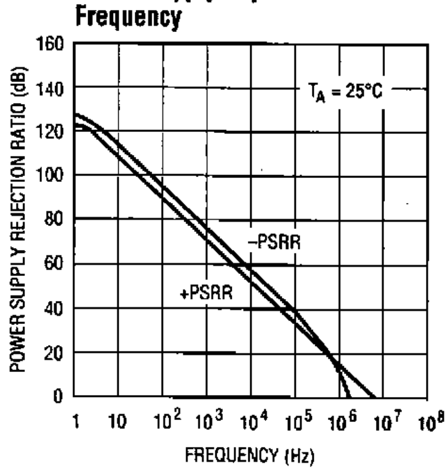
Input Bias Current Over the Common Mode Range



Common Mode Rejection Ratio vs Frequency

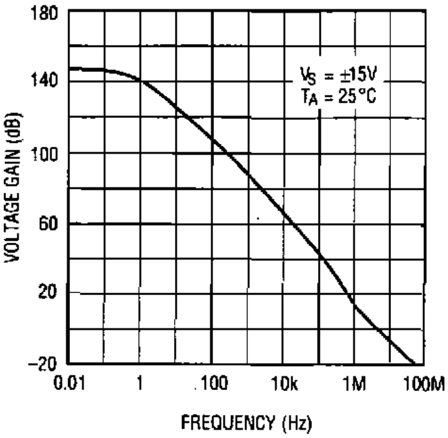


Power Supply Rejection Ratio vs Frequency

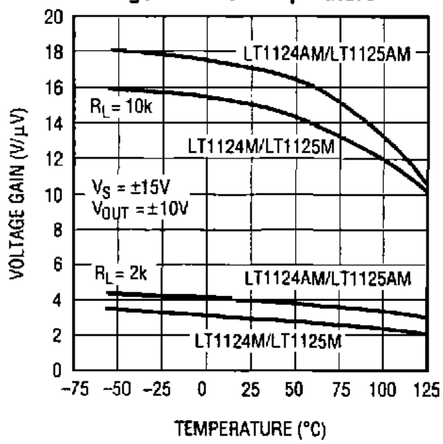


TYPICAL PERFORMANCE CHARACTERISTICS

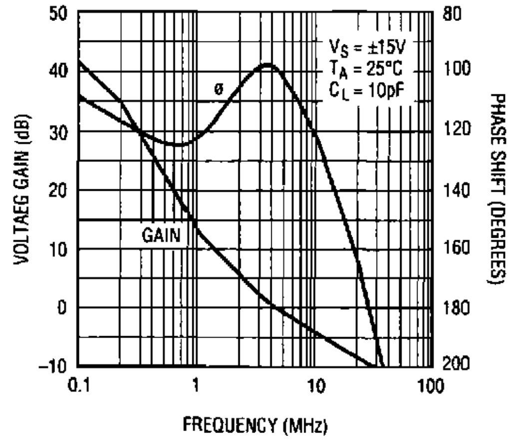
Voltage Gain vs Frequency



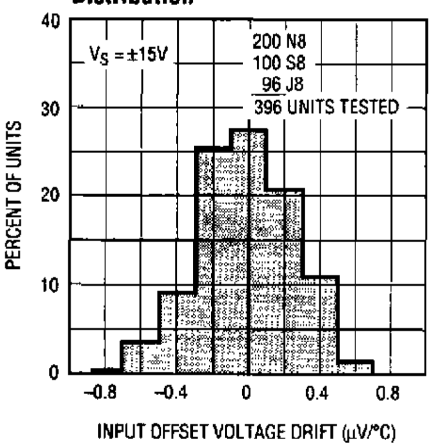
Voltage Gain vs Temperature



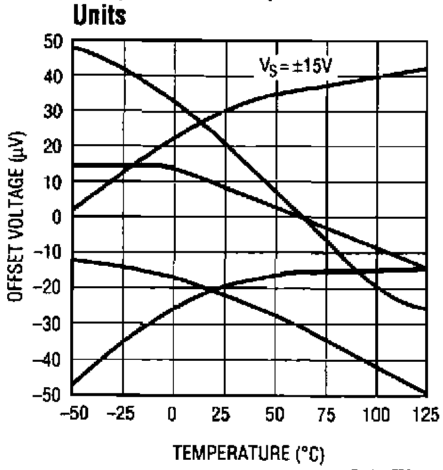
Gain, Phase Shift vs Frequency



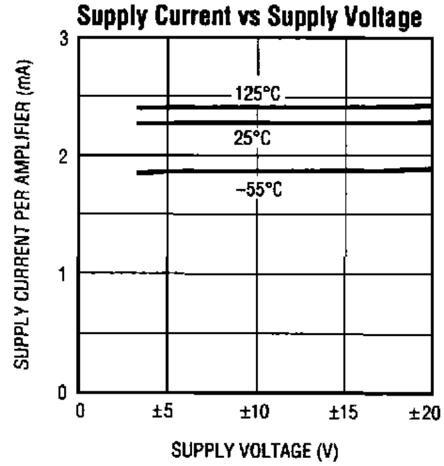
Input Offset Voltage Drift Distribution



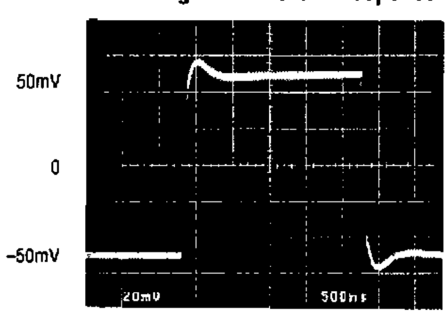
Offset Voltage Drift with Temperature of Representative Units



Supply Current vs Supply Voltage



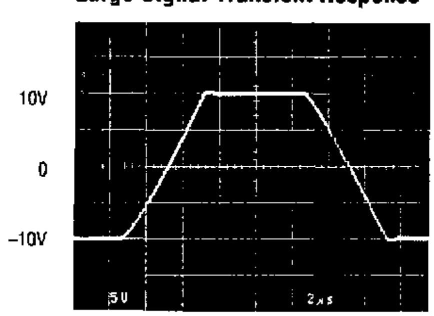
Small Signal Transient Response



A_{VCL} = +1, V_S = ±15V OR ±5V
C_L = 15pF

LT1124 • TPC16

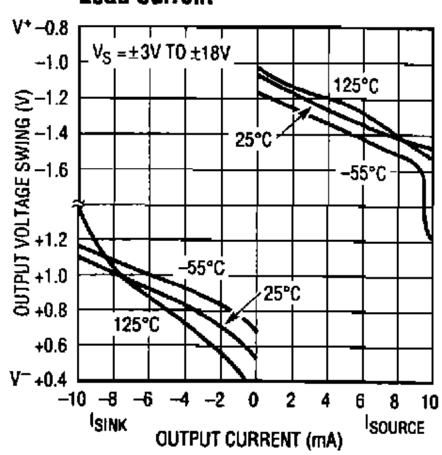
Large Signal Transient Response



A_{VCL} = −1, V_S = ±15V

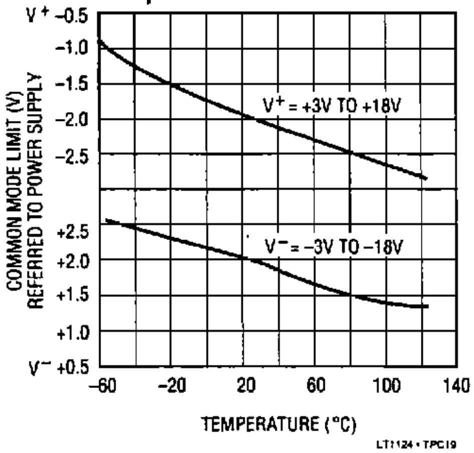
LT1124 • TPC17

Output Voltage Swing vs Load Current

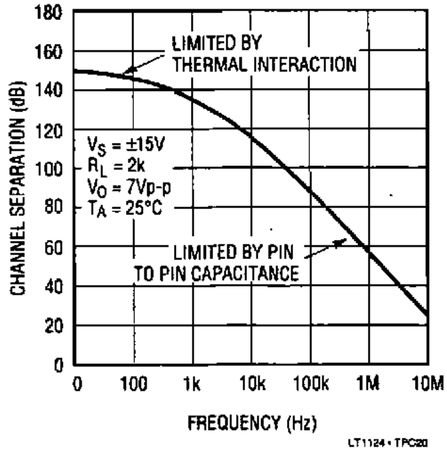


TYPICAL PERFORMANCE CHARACTERISTICS

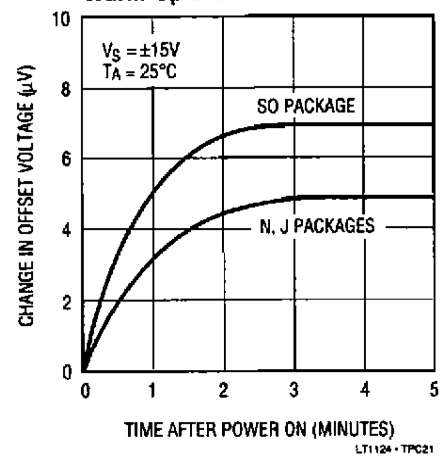
Common Mode Limit vs Temperature



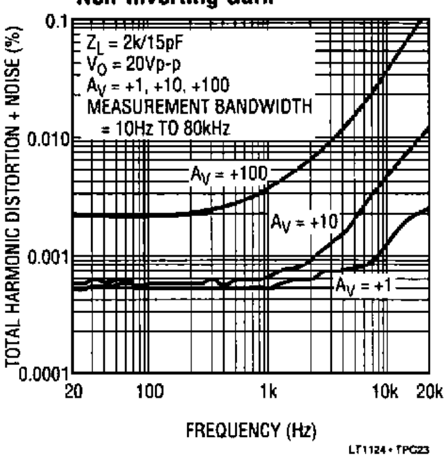
Channel Separation vs Frequency



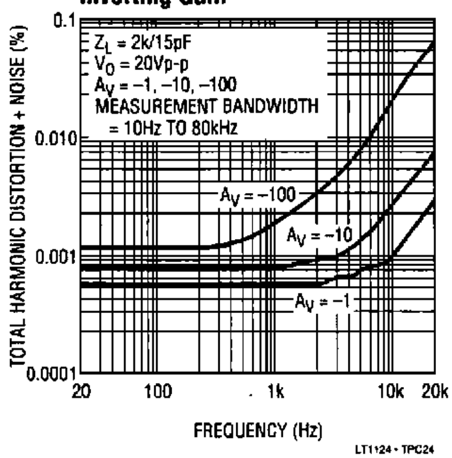
Warm-Up Drift



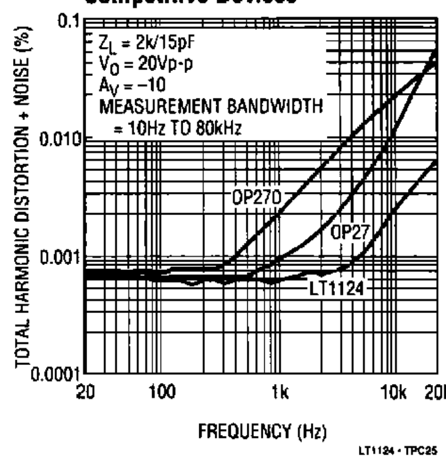
Total Harmonic Distortion and Noise vs Frequency for Non-Inverting Gain



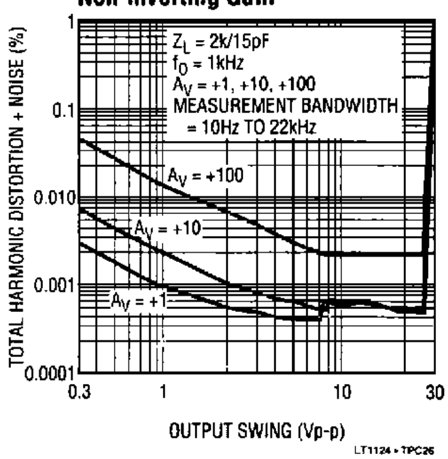
Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



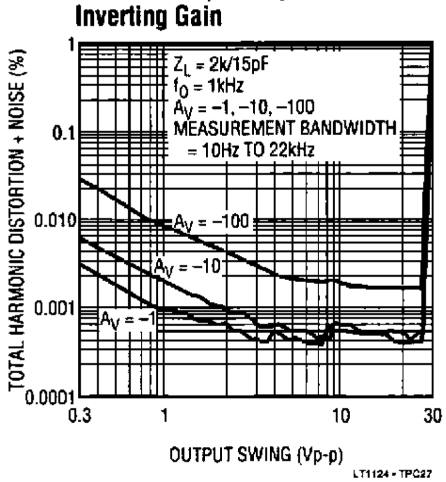
Total Harmonic Distortion and Noise vs Frequency for Competitive Devices



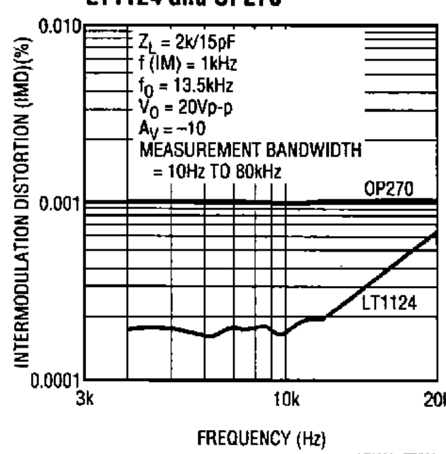
Total Harmonic Distortion and Noise vs Output Amplitude for Non-Inverting Gain



Total Harmonic Distortion and Noise vs Output Amplitude for Inverting Gain



Intermodulation Distortion (CCIF Method)* vs Frequency LT1124 and OP270



*See LT1115 data sheet for definition of CCIF testing

APPLICATIONS INFORMATION

The LT1124 may be inserted directly into OP-270 sockets. The LT1125 plugs into OP-470 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1124/LT1125.

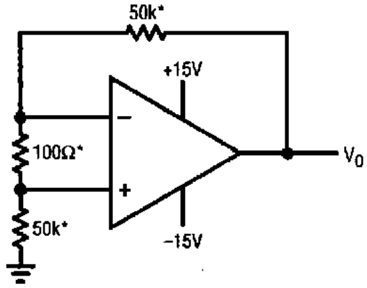
Some specifications are guaranteed by definition. For example, 70µV maximum offset voltage implies that mismatch cannot be more than 140µV. 112dB (= 2.5µV/V) CMRR means that worst case CMRR match is 106dB (5µV/V). However, the following table can be used to estimate the expected matching performance between the two sides of the LT1124, and between amplifiers A and D, and between amplifiers B and C of the LT1125.

Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1124/LT1125, with the supply voltages increased to ±16V.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



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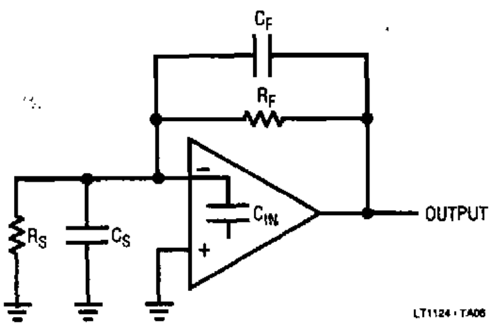
Expected Match

PARAMETER		LT1124AM/AC LT1125AM/AC 50% YIELD	98% YIELD	LT1124M/C LT1125M/C 50% YIELD	98% YIELD	UNITS
V_{OS} Match, ΔV_{OS}	LT1124	20	110	30	130	µV
	LT1125	30	150	50	180	µV
Temperature Coefficient Match		0.35	1.0	0.5	1.5	µV/°C
Average Non-Inverting I_B		6	18	7	25	nA
Match of Non-Inverting I_B		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

APPLICATIONS INFORMATION

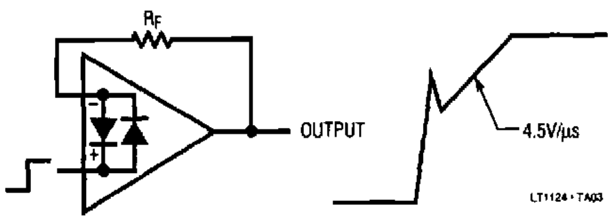
High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 2pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With R_S $(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



Unity Gain Buffer Applications

When $R_F \leq 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_F \geq 500\Omega$, the output is capable of handling the current requirements ($I_L \leq 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

Noise Testing

Each individual amplifier is tested to $4.2nV/\sqrt{Hz}$ voltage noise; i.e., for the LT1124 two tests, for the LT1125 four tests are performed. Noise testing for competing multiple op amps, if done at all, may be sample tested or tested using the circuit below.

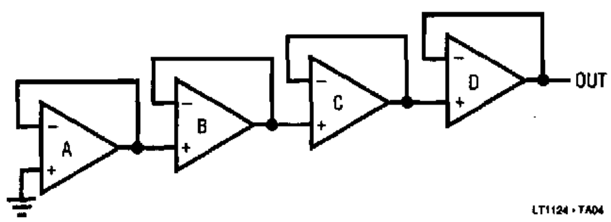
$$e_{n\,OUT} = \sqrt{(e_{nA})^2 + (e_{nB})^2 + (e_{nC})^2 + (e_{nD})^2}$$

If the LT1125 were tested this way, the noise limit would be $\sqrt{4 \times (4.2nV/\sqrt{Hz})^2} = 8.4nV/\sqrt{Hz}$. But is this an effective screen? What if three of the four amplifiers are at a typical $2.7nV/\sqrt{Hz}$, and the fourth one was contaminated and has $6.9nV/\sqrt{Hz}$ noise?

$$\text{RMS Sum} = \sqrt{(2.7)^2 + (2.7)^2 + (2.7)^2 + (6.9)^2} = 8.33nV/\sqrt{Hz}$$

This passes an $8.4nV/\sqrt{Hz}$ spec, yet one of the amplifiers is 64% over the LT1125 spec limit. Clearly, for proper noise measurement, the op amps have to be tested individually.

Competing Quad Op Amp Noise Test Method



PERFORMANCE COMPARISON

The following table summarizes the performance of the LT1124/LT1125 compared to the low cost grades of alternate approaches.

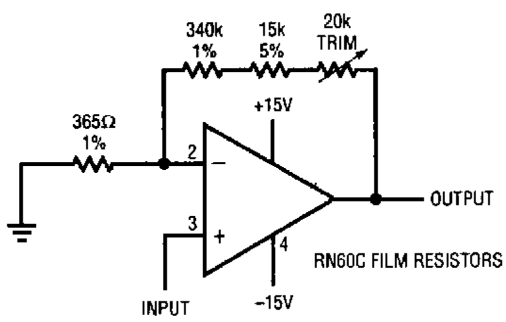
The comparison shows how the specs of the LT1124/LT1125 not only stand up to the industry standard OP-27, but in most cases are superior. Normally dual and quad performance is degraded when compared to singles, for the LT1124/LT1125 this is not the case.

Guaranteed performance, V_S = ±15V, T_A = 25°C, low cost devices.

PARAMETER/UNITS		LT1124CN8 LT1125CN	OP-27 GP	OP-270 GP	OP-470 GP	UNITS
Voltage Noise, 1kHz		4.2 100% Tested	4.5 Sample Tested	– No Limit	5.0 Sample Tested	nV/√Hz
Slew Rate		2.7 100% Tested	1.7 Not Tested	1.7	1.4	V/µs
Gain Bandwidth Product		8.0 100% Tested	5.0 Not Tested	– No Limit	– No Limit	MHz
Offset Voltage	LT1124	100	100	250	–	µV
	LT1125	140	–	–	1000	µV
Offset Current	LT1124	20	75	20	–	nA
	LT1125	30	–	–	30	nA
Bias Current		30	80	60	60	nA
Supply Current/Amp		2.75	5.67	3.25	2.75	mA
Voltage Gain, R_L = 2k		1.5	0.7	0.35	0.4	V/µV
Common Mode Rejection Ratio		106	100	90	100	dB
Power Supply Rejection Ratio		110	94	104	105	dB
S8 Package		Yes - LT1124	Yes	No	–	

TYPICAL APPLICATIONS

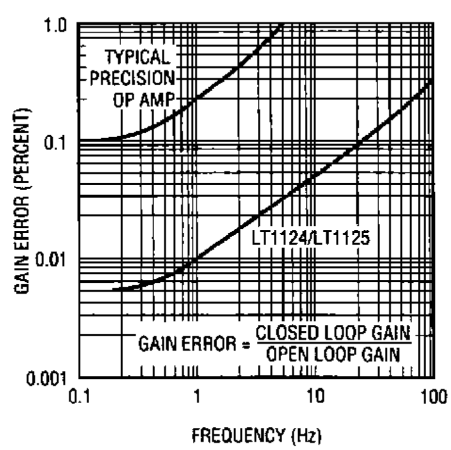
Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1124/LT1125, IS USEFUL IN LOW FREQUENCY HIGH CLOSED LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1124/LT1125 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 75 TIMES HIGHER, AS SHOWN.

LT1124 • TA07

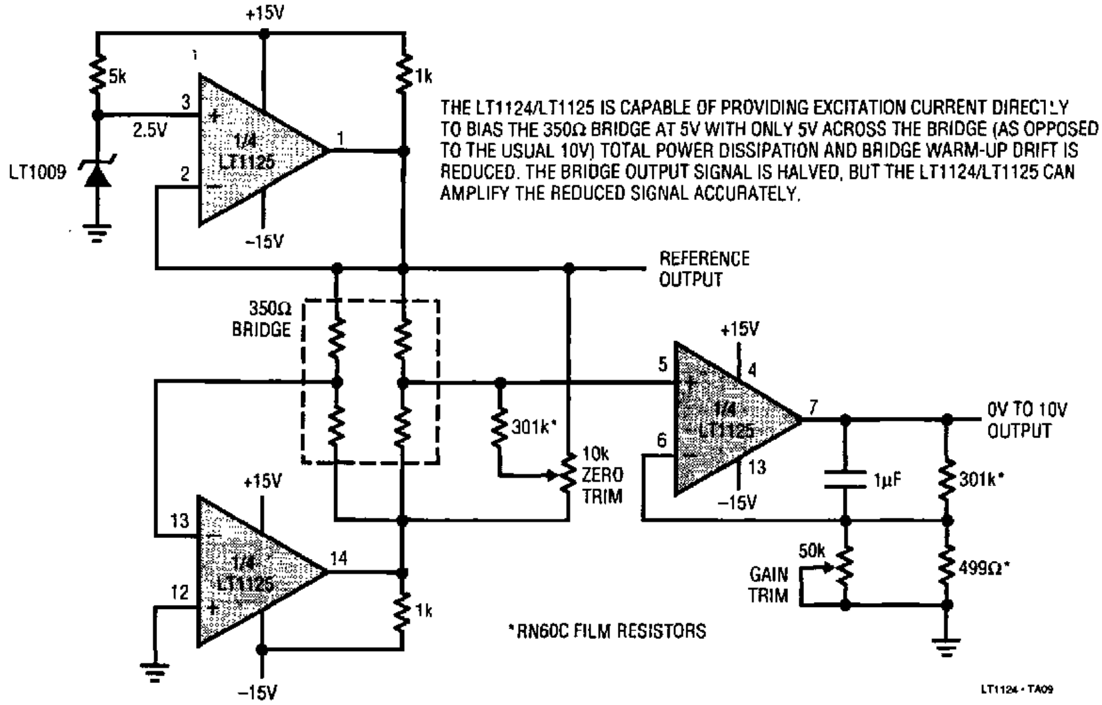
Gain Error vs Frequency Closed Loop Gain = 1000



LT1124 • TA08

TYPICAL APPLICATIONS

Strain Gauge Signal Conditioner with Bridge Excitation



SCHEMATIC DIAGRAM (1/2 LT1124, 1/4 LT1125)