

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC125FN TC74AC126FN

TC74AC125FN Quad Bus Buffer

TC74AC126FN Quad Bus Buffer

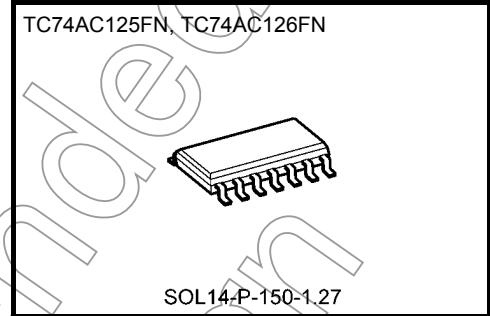
Note: xxxFN (JEDEC SOP) is not available in Japan.

The TC74AC125/126 are advanced high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74AC125 requires the 3-state control input \bar{G} to be set high to place the output into the high impedance state, whereas the TC74AC126 requires the control input to be set low to place the output into high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



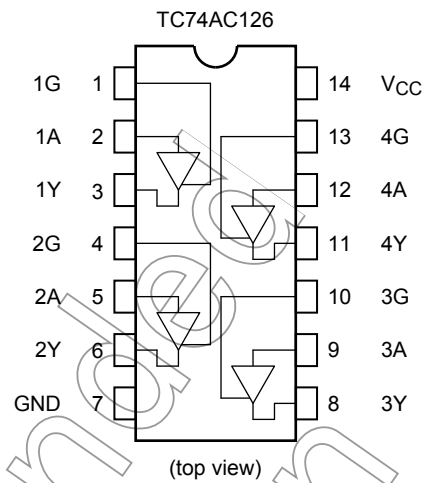
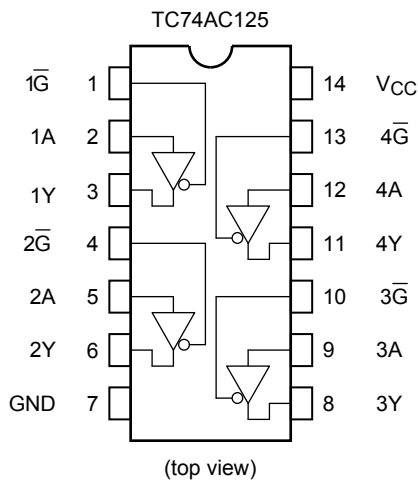
Weight
SOL14-P-150-1.27 : 0.12 g (typ.)

Features

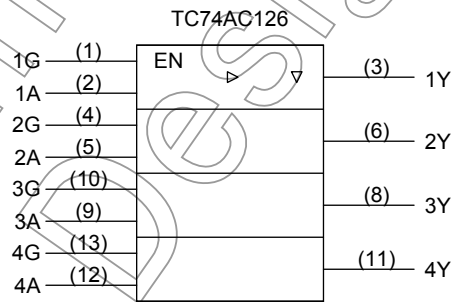
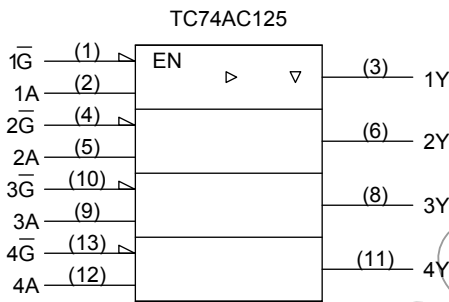
- High speed: $t_{pd} = 4.0$ ns (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 8$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min)
Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: $t_{pLH} = t_{pHL}$
- Wide operating voltage range: $V_{CC (opr)} = 2$ to 5.5 V
- Pin and function compatible with 74F125/126

Not Recommended for New Designs

Pin Assignment



IEC Logic Symbol



Truth Table

TC74AC125

Inputs		Output
\bar{G}	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care
Z: High impedance

TC74AC126

Inputs		Output
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't care
Z: High impedance

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	± 20	mA
Output diode current	I_{OK}	± 50	mA
DC output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}	± 100	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods), and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	$^{\circ}C$
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit			
				V _{CC} (V)	Min	Typ.	Max	Min		Max		
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	—	V		
				3.0	2.10	—	—	2.10	—			
				5.5	3.85	—	—	3.85	—			
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	0.50	V		
				3.0	—	—	0.90	—	0.90			
				5.5	—	—	1.65	—	1.65			
High-level output voltage	V _{OH}	V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V		
				3.0	2.9	3.0	—	2.9	—			
				4.5	4.4	4.5	—	4.4	—			
				3.0	2.58	—	—	2.48	—			
				4.5	3.94	—	—	3.80	—			
Low-level output voltage	V _{OL}	V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V		
				3.0	—	0.0	0.1	—	0.1			
				4.5	—	0.0	0.1	—	0.1			
				3.0	—	—	0.36	—	0.44			
				4.5	—	—	0.36	—	0.44			
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA		
				5.5	—		±0.1		—		±1.0	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	—		±0.1		—	±1.0	μA	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—		8.0		—	80.0	μA	

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Not for sale

AC Characteristics ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
			V _{CC} (V)	Min	Typ.	Max	Min	Max	
Propagation delay time	t _{pLH}	—	3.3 ± 0.3	—	6.4	10.5	1.0	12.0	ns
	t _{pHL}		5.0 ± 0.5	—	4.7	7.0	1.0	8.0	
Output enable time	t _{pZL}	—	3.3 ± 0.3	—	7.1	12.3	1.0	14.0	ns
	t _{pZH}		5.0 ± 0.5	—	5.0	7.9	1.0	9.0	
Output disable time	t _{pLZ}	—	3.3 ± 0.3	—	5.1	8.8	1.0	10.0	ns
	t _{pHZ}		5.0 ± 0.5	—	4.6	6.6	1.0	7.5	
Input capacitance	C _{IN}	—	—	—	5	10	—	10	pF
Output capacitance	C _{OUT}	—	—	—	10	—	—	—	pF
Power dissipation capacitance	C _{PD}	—	(Note)	—	24	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

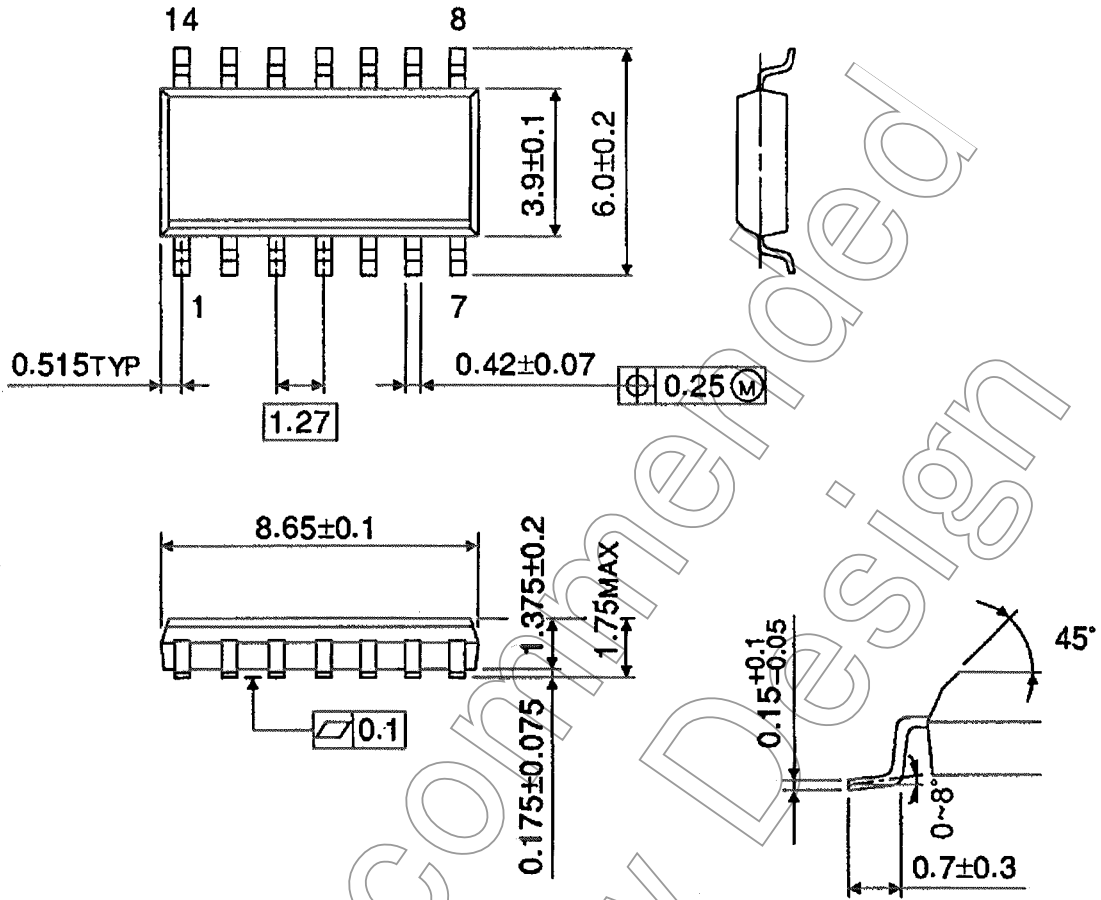
$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per gate)}$$

Not Recommended for New Designs

Package Dimensions (Note)

SOL14-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Not Recommended for New Design

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