

# 54AC/74AC353 • 54ACT/74ACT353

## Dual 4-Input Multiplexer With 3-State Outputs

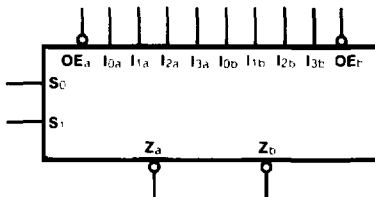
### Description

The 'AC/ACT353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable (OE) inputs, allowing the outputs to interface directly with bus-oriented systems.

- Inverted Version of the 'AC/ACT253
- Multifunction Capability
- Separate Enables for Each Multiplexer
- Outputs Source/Sink 24 mA
- 'ACT353 has TTL-Compatible Inputs

Ordering Code: See Section 6

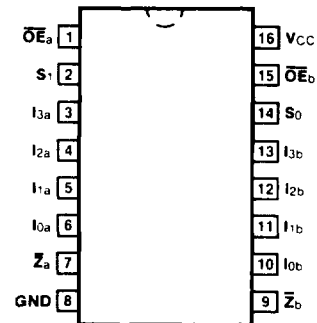
### Logic Symbol



### Pin Names

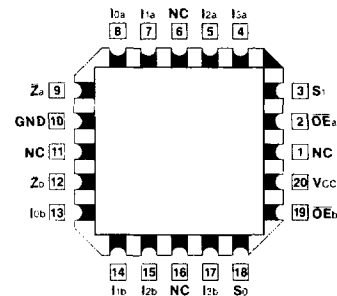
- I0a - I3a Side A Data Inputs
- I0b - I3b Side B Data Inputs
- S0, S1 Common Select Inputs
- OEa Side A Output Enable Input
- OEb Side B Output Enable Input
- Za, Zb 3-State Outputs

### Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

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Pin Assignment for LCC and PCC

# AC353 • ACT353

## Functional Description

The 'AC/ACT353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S<sub>0</sub>, S<sub>1</sub>). The 4-input multiplexers have individual Output Enable ( $\overline{OE}_a$ ,  $\overline{OE}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$\overline{Z}_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

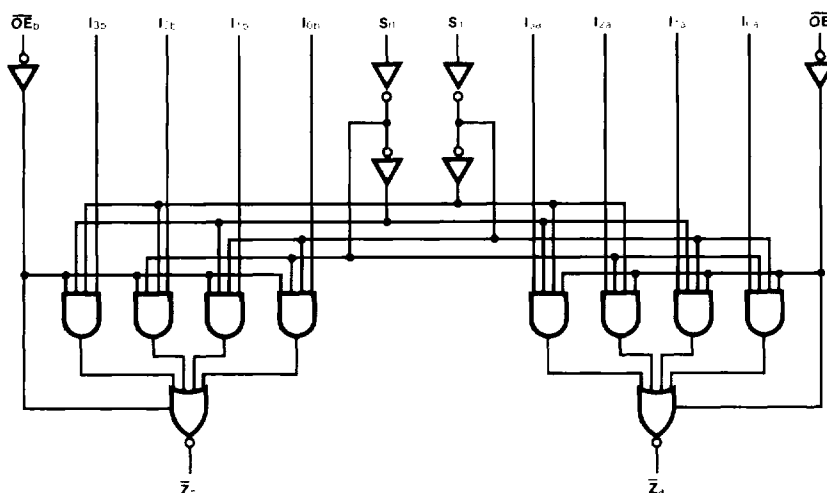
## Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S <sub>0</sub>	S <sub>1</sub>	I <sub>0</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

Address inputs S<sub>0</sub> and S<sub>1</sub> are common to both sections.

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**DC Characteristics** (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I <sub>CC</sub>	Maximum Quiescent Supply Current	160	80	μA	V <sub>IN</sub> = V <sub>CC</sub> or Ground, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = Worst Case
I <sub>CC</sub>	Maximum Quiescent Supply Current	8.0	8.0	μA	V <sub>IN</sub> = V <sub>CC</sub> or Ground, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = 25°C
I <sub>CC(T)</sub>	Maximum Additional I <sub>CC</sub> /Input (ACT353)	1.6	1.5	mA	V <sub>IN</sub> = V <sub>CC</sub> - 2.1 V, V <sub>CC</sub> = 5.5 V, T <sub>A</sub> = Worst Case

**AC Characteristics**

Symbol	Parameter	V <sub>CC</sub> * (V)	74AC			54AC		74AC		Units	Fig. No.
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	3.3 5.0	9.0 6.5							ns	3-6
t <sub>PHL</sub>	Propagation Delay S <sub>n</sub> to Z <sub>n</sub>	3.3 5.0	9.0 6.5							ns	3-6
t <sub>PLH</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3 5.0	6.5 5.0							ns	3-5
t <sub>PHL</sub>	Propagation Delay I <sub>n</sub> to Z <sub>n</sub>	3.3 5.0	6.5 5.0							ns	3-5
t <sub>PZH</sub>	Output Enable Time	3.3 5.0	5.5 4.0							ns	3-7
t <sub>PZL</sub>	Output Enable Time	3.3 5.0	6.0 4.5							ns	3-8
t <sub>PHZ</sub>	Output Disable Time	3.3 5.0	7.0 5.5							ns	3-7
t <sub>PLZ</sub>	Output Disable Time	3.3 5.0	5.5 4.0							ns	3-8

\*Voltage Range 3.3 is 3.3 V ± 0.3 V  
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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## AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay Sn to Z <sub>n</sub>	5.0		7.0					ns	3-6	
tPHL	Propagation Delay Sn to Z <sub>n</sub>	5.0		7.0					ns	3-6	
tPLH	Propagation Delay In to Z <sub>n</sub>	5.0		5.5					ns	3-5	
tPHL	Propagation Delay In to Z <sub>n</sub>	5.0		5.5					ns	3-5	
tpZH	Output Enable Time	5.0		4.5					ns	3-7	
tpZL	Output Enable Time	5.0		5.0					ns	3-8	
tpHZ	Output Disable Time	5.0		6.0					ns	3-7	
tPLZ	Output Disable Time	5.0		4.5					ns	3-8	

\*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

## Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C <sub>IN</sub>	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance		pF	Vcc = 5.5 V