

IH5148 - IH5151

High Reliability High-Level CMOS Analog Switches

GENERAL DESCRIPTION

The IH5148 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5148 CMOS technology has eliminated this problem.

Key performance advantages of the 5148 series are TTL compatibility and ultra low-power operation. $R_{DS(on)}$ switch resistance is typically in the 14Ω To 18Ω Area, for signals in the $-10V$ to $+10V$ range. Quiescent current is less than $10\mu A$. The 5148 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200nsec typ.) such that it exceeds t_{OFF} time (120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Many of the devices in the 5148 series are pin-for-pin compatible with other analog switches, and offer improved electrical characteristics.

FEATURES

- Low $R_{DS(ON)}$ — 25Ω
- Switches Greater Than 20Vpp Signals With $\pm 15V$ Supplies
- Quiescent Current Less Than $100\mu A$
- Break-Before-Make Switching t_{OFF} 120nsec Typ., t_{ON} 200nsec Typical
- TTL, CMOS Compatible
- Non-Latching With Supply Turn-Off
- Complete Monolithic Construction
- $\pm 5V$ to $\pm 15V$ Supply Range

CMOS ANALOG SWITCH PRODUCT CONDITIONING

- The Following Processes Are Performed 100% in Accordance With MIL-STD-883
- Precap Visual — Method 2010, Cond. B
- Stabilization Bake — Method 1008
- Temperature Cycle — Method 1010
- Centrifuge — Method 2001, Cond. E
- Hermeticity — Method 1014, Cond. A, C
- (Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range	Harris Equivalent
IH5148MJE IH5148MFD	Dual SPST Dual SPST	16 Pin Cerdip 14 Pin Flat Pack	$-55^{\circ}C$ to $125^{\circ}C$ $-50^{\circ}C$ to $125^{\circ}C$	HI-5048 HI-5048
IH5149MJE IH5149MFD	Dual DPST Dual DPST	16 Pin Cerdip 14 Pin Flat Pack	$-55^{\circ}C$ to $125^{\circ}C$ $-50^{\circ}C$ to $125^{\circ}C$	HI-5049 HI-5049
IH5150MJE IH5150MFD	SPDT SPDT	16 Pin Cerdip 14 Pin Flat Pack	$-55^{\circ}C$ to $125^{\circ}C$ $-50^{\circ}C$ to $125^{\circ}C$	HI-5050 HI-5050
IH5151MJE IH5151MFD	Dual SPDT Dual SPDT	16 Pin Cerdip 14 Pin Flat Pack	$-55^{\circ}C$ to $125^{\circ}C$ $-50^{\circ}C$ to $125^{\circ}C$	HI-5051 HI-5051

- NOTES: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

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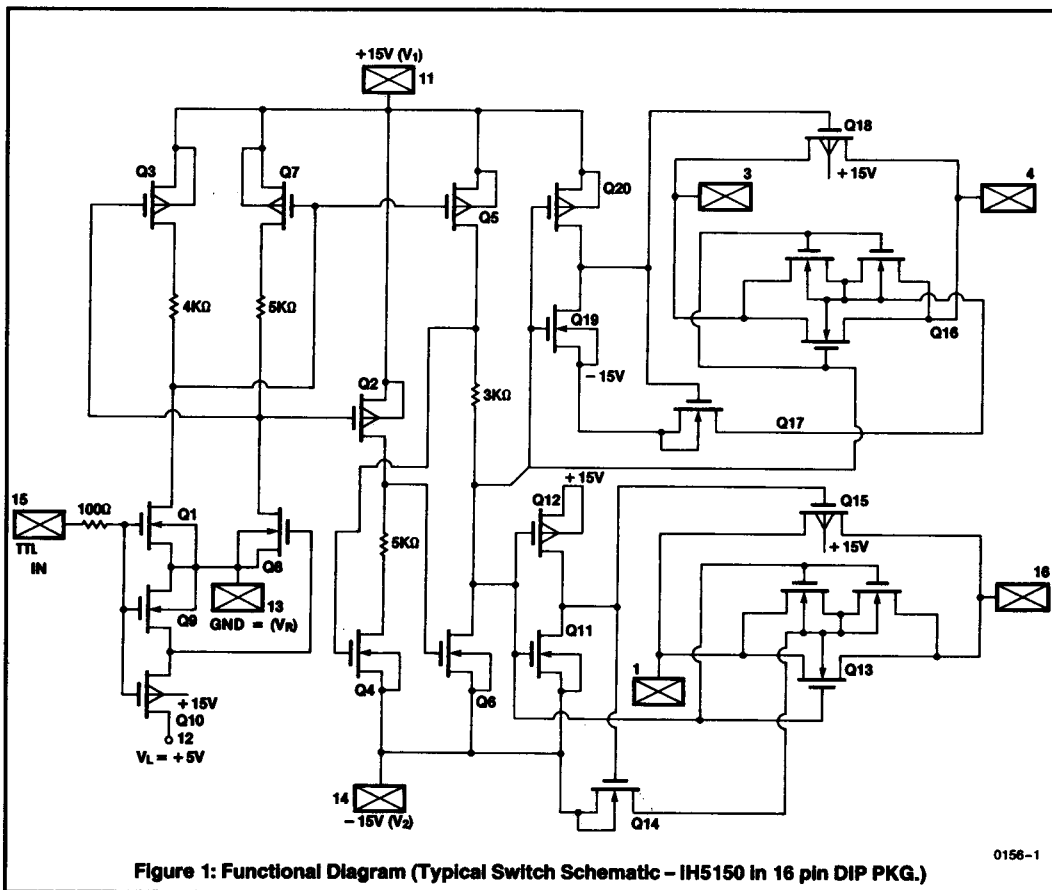
ABSOLUTE MAXIMUM RATINGS

V ⁺ , V ⁻	<36V
V ⁺ , V _D	<30V
V _D , V ⁻	<30V
V _D , V _S	< ±22V
V _L , V ⁻	<33V
V _L , V _{IN}	<30V
V _I	<20V
V _{IN}	<20V
Current (Any Terminal)	<50mA
Storage Temperature	-65°C to +150°C

Operating Temperature -55°C to +125°C
 Lead Temperature (Soldering, 10sec) 300°C
 Power Dissipation 450mW
 (All Leads Soldered to a P.C. Board)
 Derate 6mW/°C Above 70°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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IH5148-IH5151**ELECTRICAL CHARACTERISTICS** ($T_A @ 25^\circ\text{C}$, $V^+ = +15\text{V}$, $V^- = -15\text{V}$, $V_L = +5\text{V}$)

Per Channel		Test Conditions	Min/Max Limits			Units
Symbol	Characteristic		Military			
			-55°C	+25°C	+125°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4\text{V}$ (Note 1)	± 1	± 1	± 10	μA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8\text{V}$ (Note 1)	± 1	± 1	± 10	μA
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = \pm 10\text{V}$, $I_S = -10\text{mA}$	25	25	50	Ω
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			10 (Typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			± 14 (Typ)		V
$I_{D(OFF)}$ $I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10\text{V}$ to $+10\text{V}$		± 1.0	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10\text{V}$ to $+10\text{V}$		± 1.0	100	nA
$Q_{(INJ)}$	Charge Injection	See Figure 4		(10) (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1\text{MHz}$, $R_L = 100\Omega$, $C_L \leq 5\text{pF}$, See Figure 5		54 (Typ)		dB
SUPPLY						
I^+	+ Power Supply Quiescent Current	$V_1 = +15\text{V}$, $V_2 = -15\text{V}$, $V_L = +5\text{V}$, $V_R = 0$	10	10	100	μA
I^-	- Power Supply Quiescent Current		10	10	100	μA
I_L	+5V Supply Quiescent Current		10	10	100	μA
I_{GND}	Gnd Supply Quiescent Current		10	10	100	μA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)	

NOTE 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

**SWITCHING TIME SPECIFICATION
IH5148 SPST SWITCH**

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1\text{K}\Omega$; $V_{ANALOG} = -10\text{V}$		250	ns
t_{off}	Switch "off" time	$T_O + 10\text{V}$; See Figures 3 and 6		200	ns

IH5149 DPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1\text{K}\Omega$, $V_{ANALOG} = -10\text{V}$		350	ns
t_{off}	Switch "off" time	$T_O + 10\text{V}$; See Figures 3 and 6		250	ns

IH5150 & IH5151 SPDT SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1\text{K}\Omega$, $V_{ANALOG} = -10\text{V}$		500	ns
t_{off}	Switch "off" time	$T_O + 10\text{V}$; See Figures 3 and 6		250	ns

NOTE 2. For IH5150 & IH5151 devices, channels which are off for logic input $\geq 2.4\text{V}$ (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower t_{on} time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

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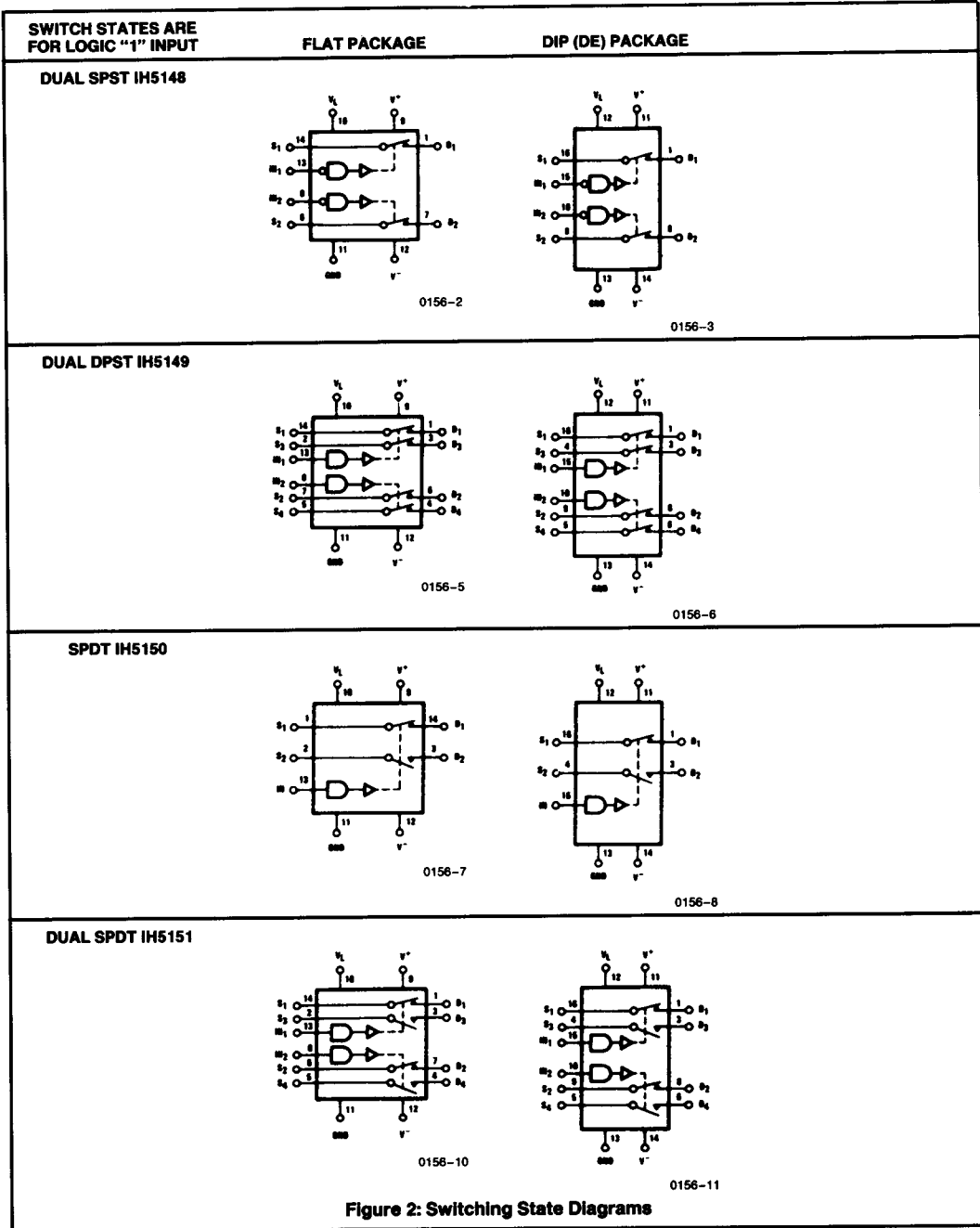


Figure 2: Switching State Diagrams

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TEST CIRCUITS

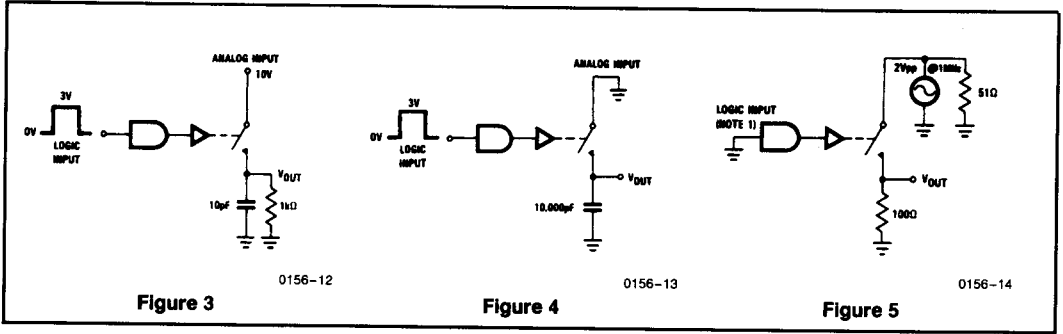


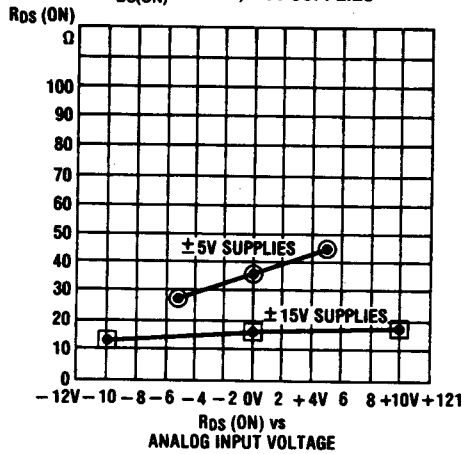
Figure 3

Figure 4

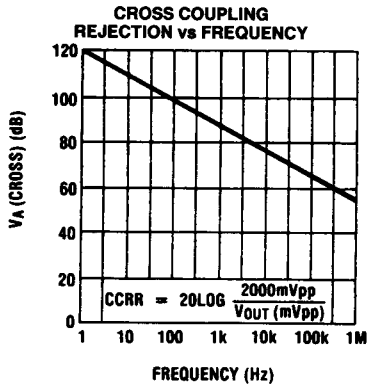
Figure 5

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

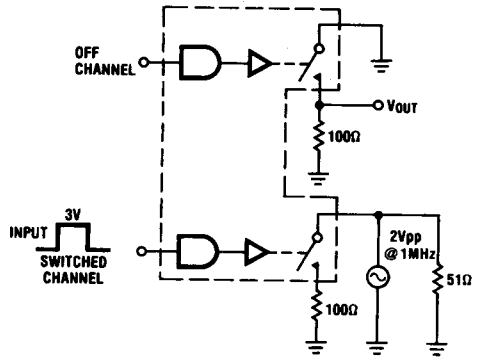
$R_{DS(ON)} @ \pm 15V, \pm 5V \text{ SUPPLIES}$



0156-15



0156-16

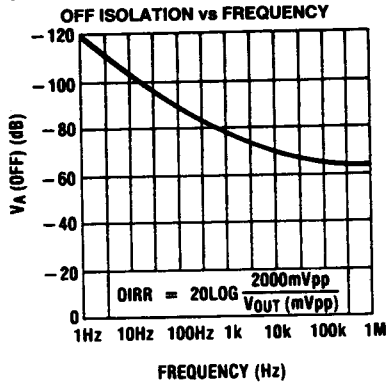


CROSS COUPLING REJECTION TEST CIRCUIT

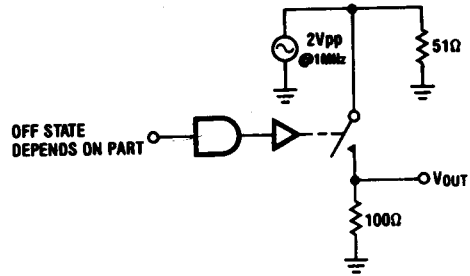
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TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)



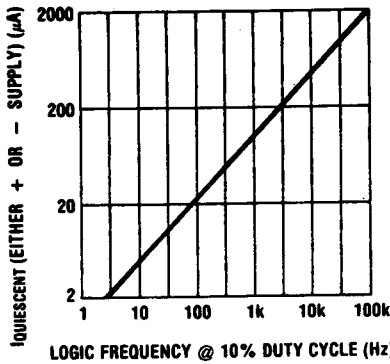
0156-18



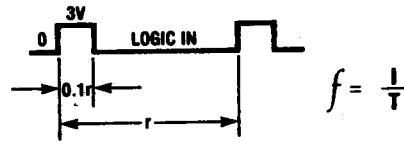
OFF ISOLATION TEST CIRCUIT

0156-19

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE



0156-20



LOGIC INPUT WAVEFORM

0156-21

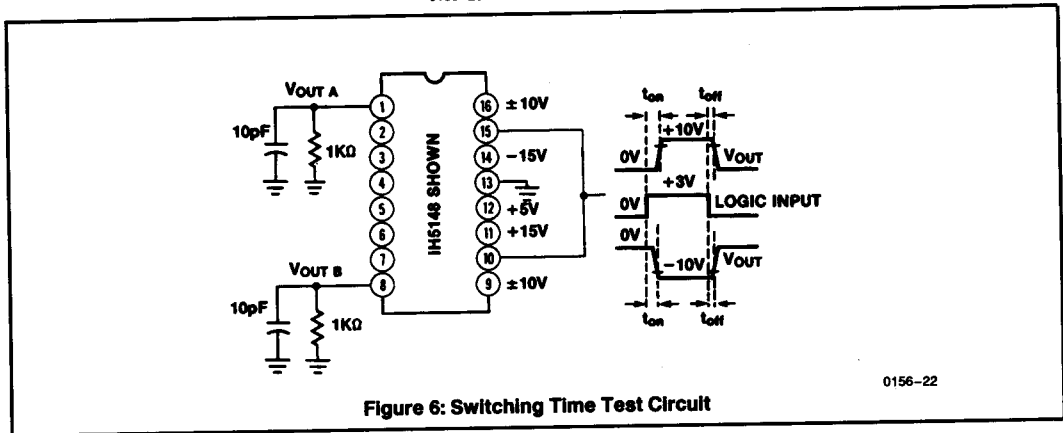


Figure 6: Switching Time Test Circuit

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Nulling Out Charge Injection:

Charge injection (Q_{inj} , on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from $-15V$ to $+15V$ as a rapidly changing pulse; thus this $30V_{pp}$ pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Q_{inj}(V_{pp}) = \frac{C_{gate}}{C_{Load}} \times 30V \text{ step.}$$

i.e.

$C_{gate} = 1.5pF$, $C_{Load} = 1000pF$, then

$$Q_{inj}(V_{pp}) = \frac{1.5pF}{1000pF} \times 30V \text{ step} = 45mV_{pp}$$

Thus if you are using switch in a Sample & Hold application with $C_{sample} = 1000pF$, a $45mV_{pp}$ "Sample to Hold error step" will occur.

To null this error step out to zero the following circuit can be used:

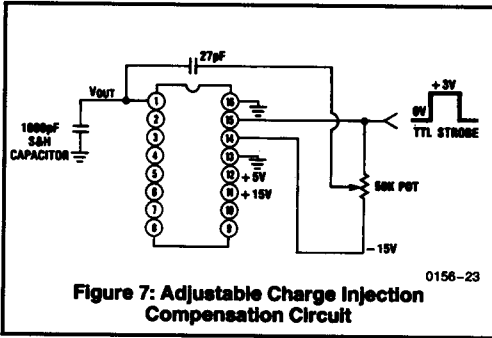


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until $V_{OUT} = 0mV_{pp}$ pulse, with $V_{ANALOG} = 0V$.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:

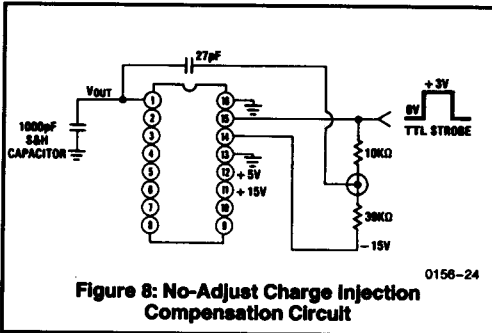


Figure 8: No-Adjust Charge Injection Compensation Circuit

This configuration will produce a typical charge injection of $V_{OUT} \leq 10mV_{pp}$ into the $1000pF$ S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the $\pm 15V$ (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:

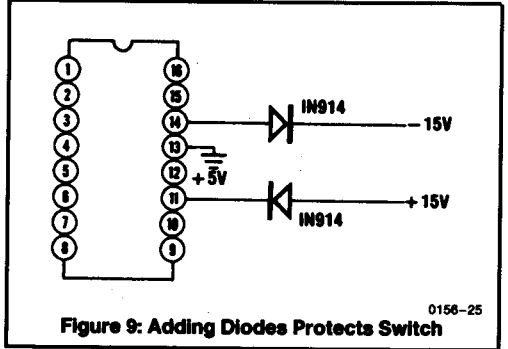


Figure 9: Adding Diodes Protects Switch

If the analog input levels are below $\pm 15V$, the pn junctions of Q13 & Q15 are reversed biased. However if the $\pm 15V$ supplies are shut off and analog levels are still present, the configuration becomes:

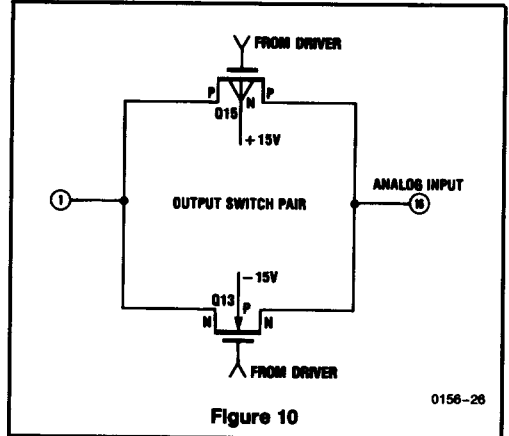
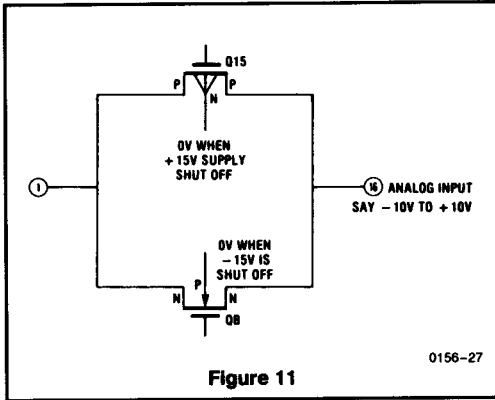


Figure 10

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The need for these diodes, in this circumstance, is shown below:



If ANALOG in is greater than 1V, then the pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to -1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about $\pm 18V$ ANALOG overvoltages. Beyond this drain(N) to body(P) breakdown VOLTAGE of Q13 limits overvoltage protection.

