

N-CHANNEL ENHANCEMENT MOS FET

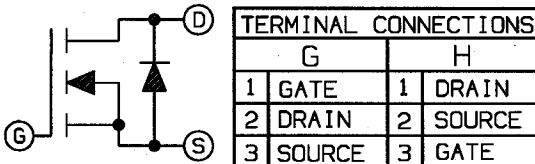
100V, 9.2A, 0.27Ω

SDF120 JAA
SDF120 JAB
SDF120 JDA

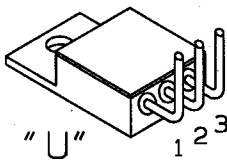
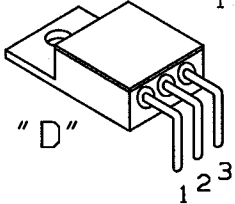
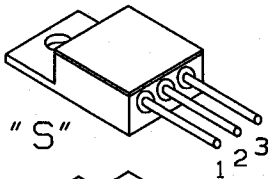
FEATURES

- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS: JAA, JAB
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-S-19500 SCREENING

SCHEMATIC



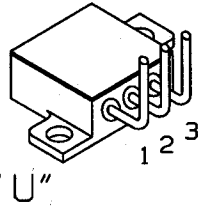
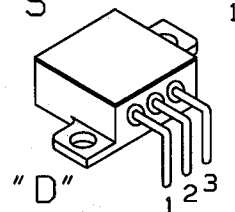
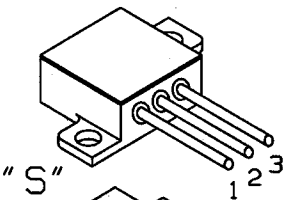
STANDARD BEND CONFIGURATIONS



JAA
JDA

(CUSTOM BEND OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATIONS



JAB

(CUSTOM BEND OPTIONS AVAILABLE)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
Drain-source Volt.(1)	V _{DSS}	100	V _{dc}
Drain-Gate Voltage (R _{GS} =1.0MΩ) (1)	V _{DGR}	100	V _{dc}
Gate-Source Voltage Continuous	V _{GS}	±20	V _{dc}
Drain Current Continuous (T _c = 25°C)	I _D	9.2	A _{dc}
Drain Current Pulsed(3)	I _{DM}	37	A
Total Power Dissipation	PD	50	W
Power Dissipation Derating > 25°C		0.4	W/°C
Operating & Storage Temp.	T _J /T _{sig}	-55 TO +150	°C
Thermal Resistance	R _{thJc}	2.5	°C/W
Max. Lead temperature	TL	300	°C

ELECTRICAL CHARACTERISTICS T_c = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V _{(BR)DSS}	V _{GS} =0V I _D =250 μA	100	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _D =V _{GS} I _D =250 μA	2.0	-	4.0	V
Gate Source Leakage	I _{GSS}	V _{GS} =±20 V	-	-	100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _D =MAX. RATING V _{GS} =0	-	-	250	μA
Static Drain-Source On-State Resistance(1)	R _{DS(ON)}	V _{GS} =10 V I _D =5.6A	-	-	.27	Ω
Forward Trans-Conductance (2)	g _{fs}	V _D ≥ 50 V I _D =8.3A	4.6	-	-	S(O)
Input Capacitance	C _{ISS}	V _{GS} =0V V _D =25 V f=1.0 MHz	-	650	-	pF
Output Capacitance	C _{OSS}	V _{GS} =0V V _D =25 V f=1.0 MHz	-	240	-	pF
Reverse Transfer Capacitance	C _{RSS}	V _{GS} =0V V _D =25 V f=1.0 MHz	-	44	-	pF
Turn-On Delay	t _{d(on)}	V _D =50V R _G =12 n I _D =14A R _D =3.6 n	-	-	14	ns
Rise Time	t _r	(MOSFET switching times are essentially independent of operating temp.)	-	-	63	ns
Turn-Off Delay	t _{d(off)}	(MOSFET switching times are essentially independent of operating temp.)	-	-	33	ns
Fall Time	t _f	(MOSFET switching times are essentially independent of operating temp.)	-	-	38	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q _g	V _{GS} =10V, I _D =14A	-	-	26	nC
Gate-Source Charge	Q _{gs}	V _D =0.8 MAX. RATING (Gate charge is essentially independent of the operating temperature)	-	-	5.5	nC
Gate-Drain ("Miller") Charge	Q _{gd}	V _D =0.8 MAX. RATING (Gate charge is essentially independent of the operating temperature)	-	-	11	nC

SOURCE-DRAIN DIODE RATINGS & CHARACT. T_c = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier (See schematic)	-	-	14	A
Pulse Source Current (Body Diode) (1)	I _{SM}	Modified MOSFET symbol showing the integral reverse P-N junction rectifier (See schematic)	-	-	56	A
Diode Forward Voltage (2)	V _{SD}	I _F =14A V _{GS} =0V T _c =+25°C	-	-	2.5	V
Reverse Recovery Time	t _{rr}	T _c =+25° C I _F =14A	-	-	250	ns
Reverse Recovery Charge	Q _{rr}	I _F =14A di/dt=100A/μS	-	.58	-	μC

REV. 10/93

- (1) T_J = 25°C to 150°C.
(2) Pulse test: Pulse Width < 300μS, Duty Cycle < 2%.
(3) Repetitive Rating: Pulse Width limited By Max. junction Temperature.