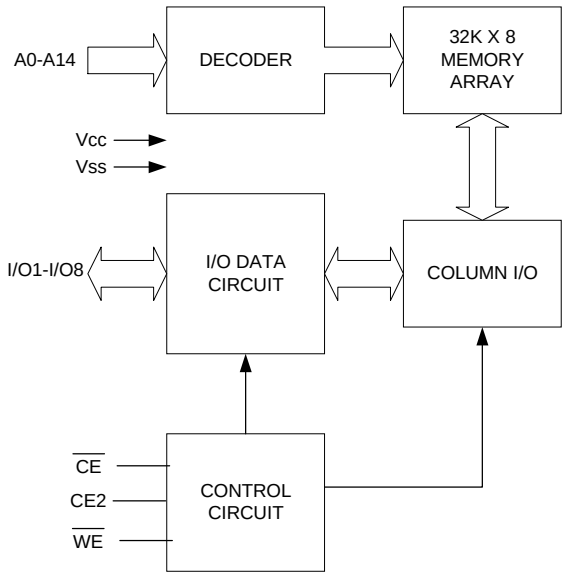
REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original.	Jun 7,2001
Rev. 1.0	1.TRUTH TABLE 2.DC ELECTRICAL CHARACTERISTICS	Jul 19,2001
Rev. 1.1	Add order information for lead free product	May15,2003

FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
  Operating : 40 mA (typical.)
  Standby : 3mA (typical) normal
  2uA (typical) L-version
  1uA (typical) LL-version
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 28-pin 600 mil PDIP
  28-pin 330 mil SOP
  28-pin 8mmx13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$、CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
V_{CC}	Power Supply
V_{SS}	Ground

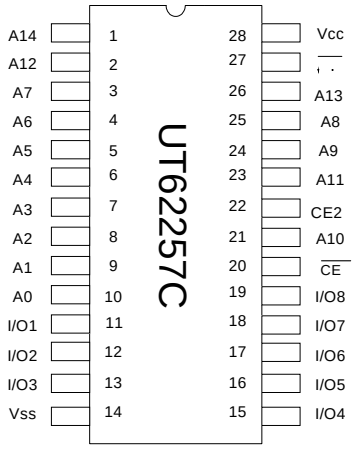
GENERAL DESCRIPTION

The UT62257C is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

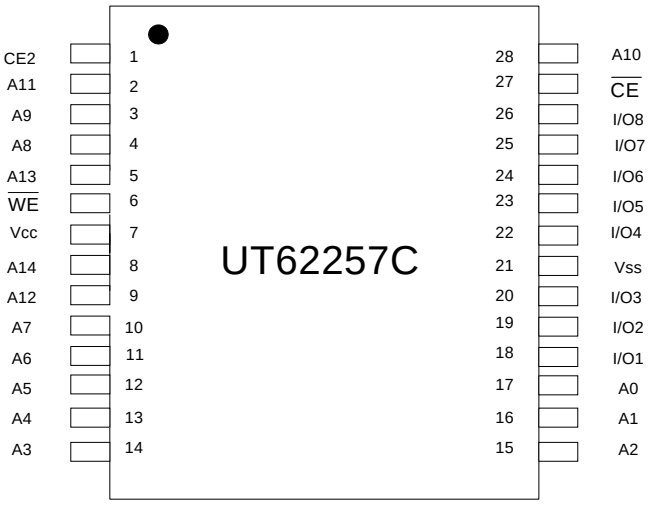
The UT62257C is designed for high-speed and low power application. With 2 chip controls ($\overline{CE}$、CE2), it is easy to design memory systems with power-down and capacity expansion in the application circuits. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62257C operates from a single 5V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



PDIP/SOP



STSOP

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	CE2	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I_{SB}, I_{SB1}
	X	L	X	High - Z	I_{SB}, I_{SB1}
Read	L	H	H	D_{OUT}	I_{CC}, $I_{CC}1$, $I_{CC}2$
Write	L	H	L	D_{IN}	I_{CC}, $I_{CC}1$, $I_{CC}2$

Note: H = VIH, L=VIL, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}*1			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}*2			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$, $\overline{CE}$ =V_{IH} or CE2 = V_{IL}		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min., $I_{I/O}$ = 0mA , $\overline{CE}$ =V_{IL} , CE2 = V_{IH}	- 35	-	40	50	mA
			- 70	-	30	40	mA
	$I_{CC}1$	Cycle time=1µs,100%duty,$I_{I/O}$=0mA, $\overline{CE}$ = 0.2V ; CE2 = V_{CC}-0.2V , other pins at 0.2V or V_{CC}-0.2V		-	-	10	mA
	$I_{CC}2$	Cycle time=500ns,100%duty,$I_{I/O}$=0mA, $\overline{CE}$ = 0.2V ; CE2 = V_{CC}-0.2V , other pins at 0.2V or V_{CC}-0.2V		-	-	20	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}$ =V_{IH} or CE2 = V_{IL}	normal	-	1	10	mA
	I_{SB1}	$\overline{CE} \geqq V_{CC}$-0.2V, CE2$\geqq V_{CC}$-0.2V			0.3	5	mA
	I_{SB}	$\overline{CE}$ =V_{IH} or CE2 = V_{IL}	-L/-LL	-	-	3	mA
	I_{SB1}	$\overline{CE} \geqq V_{CC}$-0.2V	-L	-	2	100	µA
		CE2$\geqq V_{CC}$-0.2V	-LL	-	1	40	µA

Notes:
1. Overshoot : Vcc+2.0v for pulse width less than 10ns.
2. Undershoot : Vss-2.0v for pulse width less than 10ns.
3. Overshoot and Undershoot are sampled, not 100% tested.

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10% , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62257C-35		UT62257C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	25	-	35	ns
Output Disable to Output in High Z	t_{OHZ*}	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

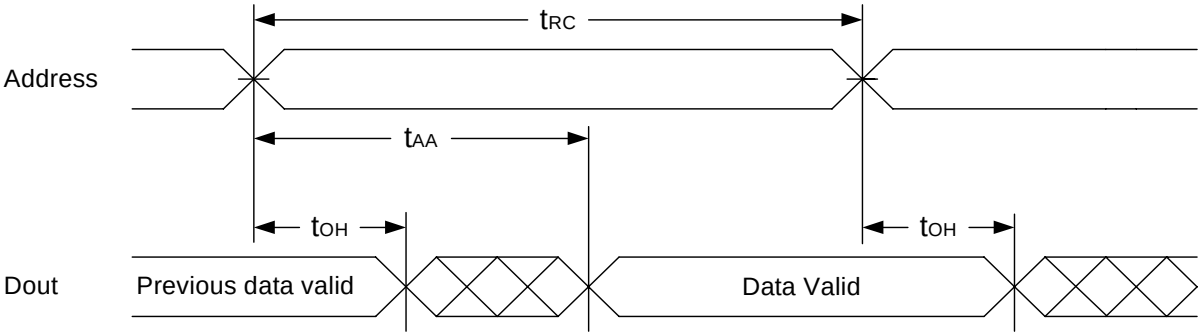
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62257C-35		UT62257C-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	50	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	15	-	25	ns

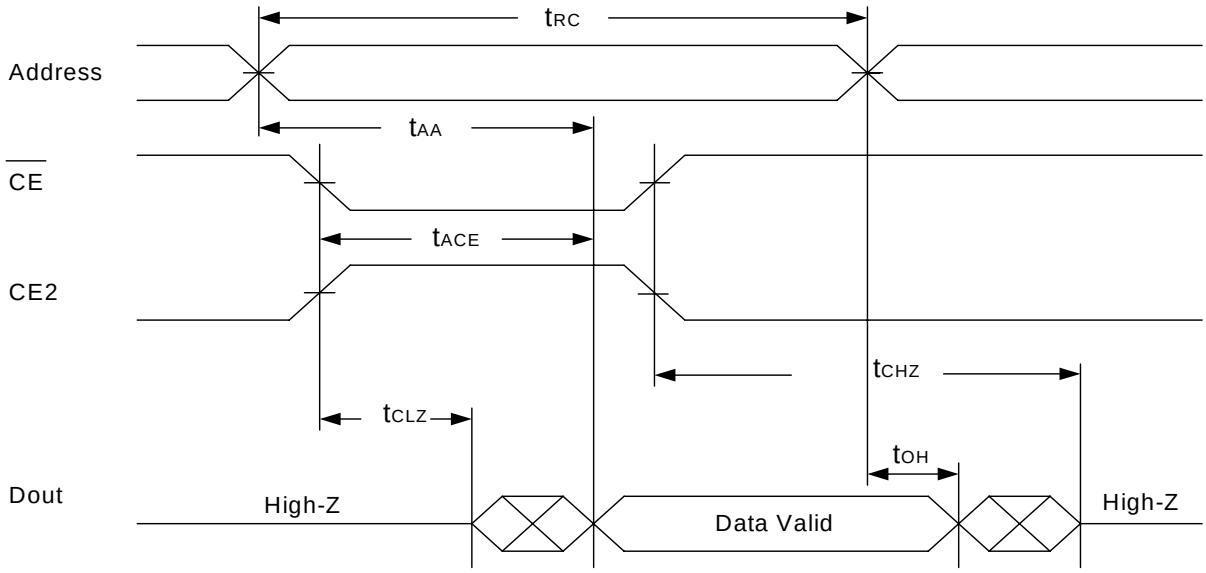
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



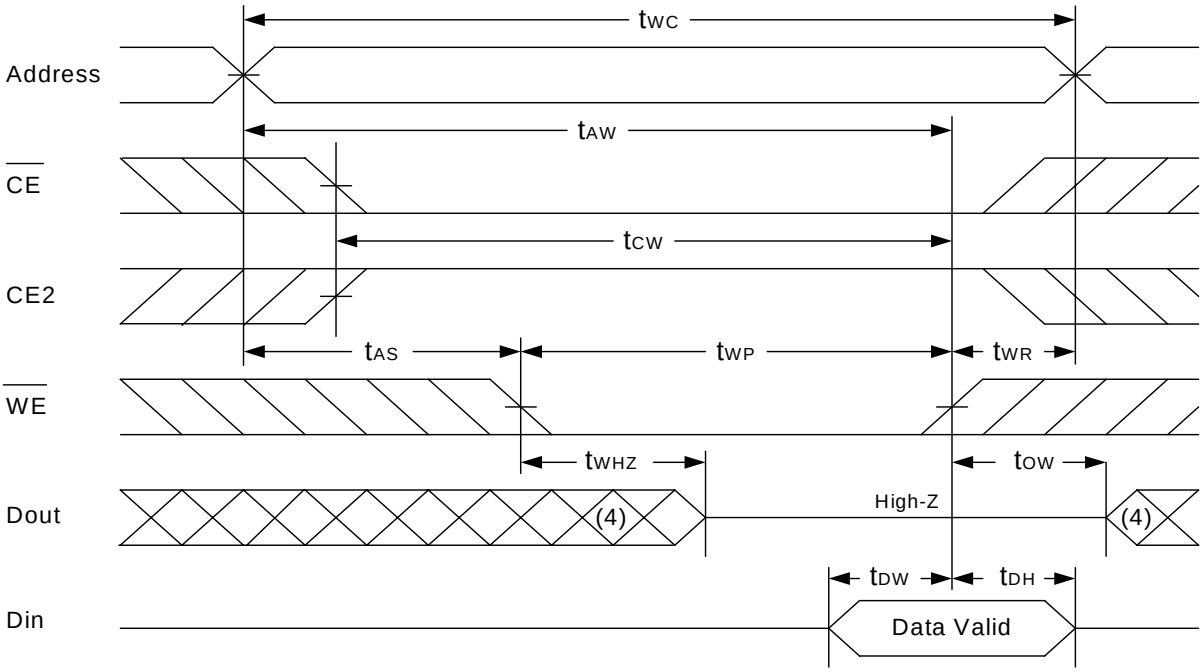
READ CYCLE 2 ($\overline{CE}$ and CE2 Controlled) (1,3,4,5)



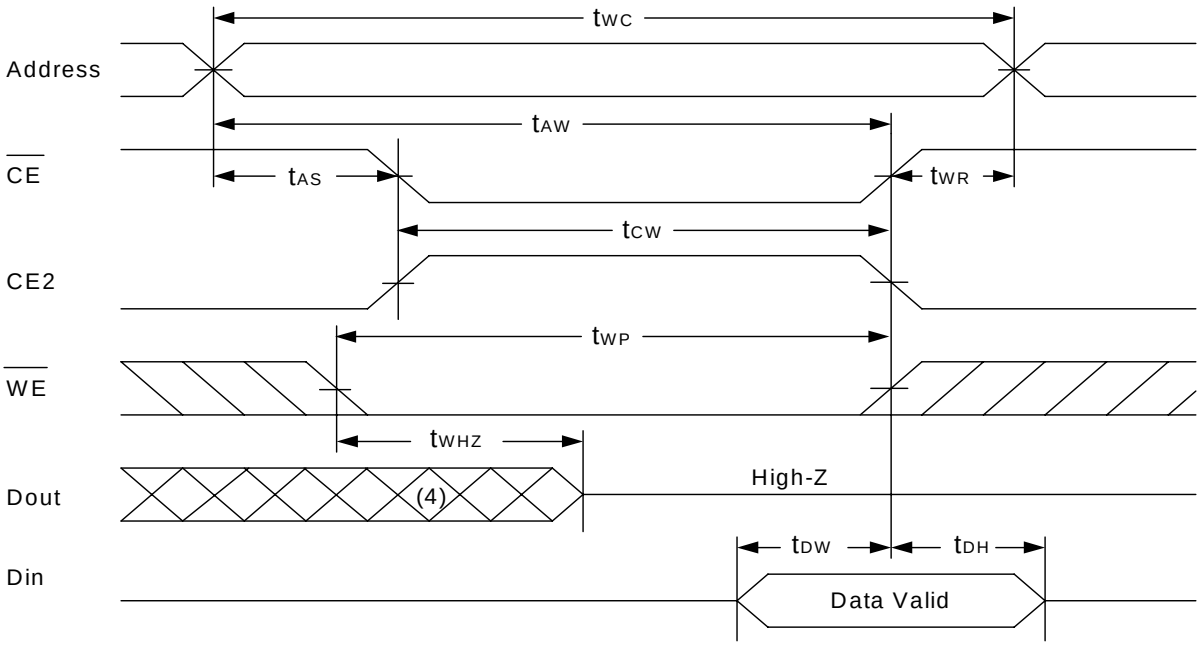
Notes :

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CE}$ =low, CE2=high.
3. Address must be valid prior to or coincident with $\overline{CE}$ =low, CE2=high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L=5pF. Transition is measured±500mV from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5,6)



WRITE CYCLE 2 ($\overline{CE}$ and CE2 Controlled) (1,2,5,6)



Notes :

1. $\overline{WE}$, $\overline{CE}$ must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$, high CE2, low $\overline{WE}$.
3. During a $\overline{WE}$ controlled write cycle, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition and CE2 high transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

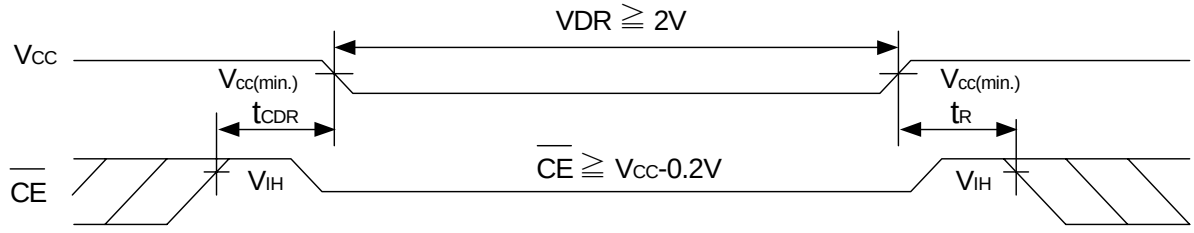
DATA RETENTION CHARACTERISTICS (T_A = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V or CE2 ≤ 0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc=3V, CE2 ≤ 0.2V	- L	-	1	50	µA
		or $\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC*}	-	-	ns

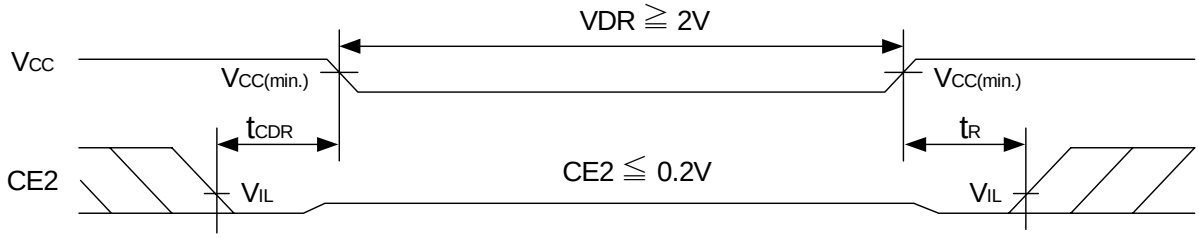
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) ($\overline{CE}$ controlled)

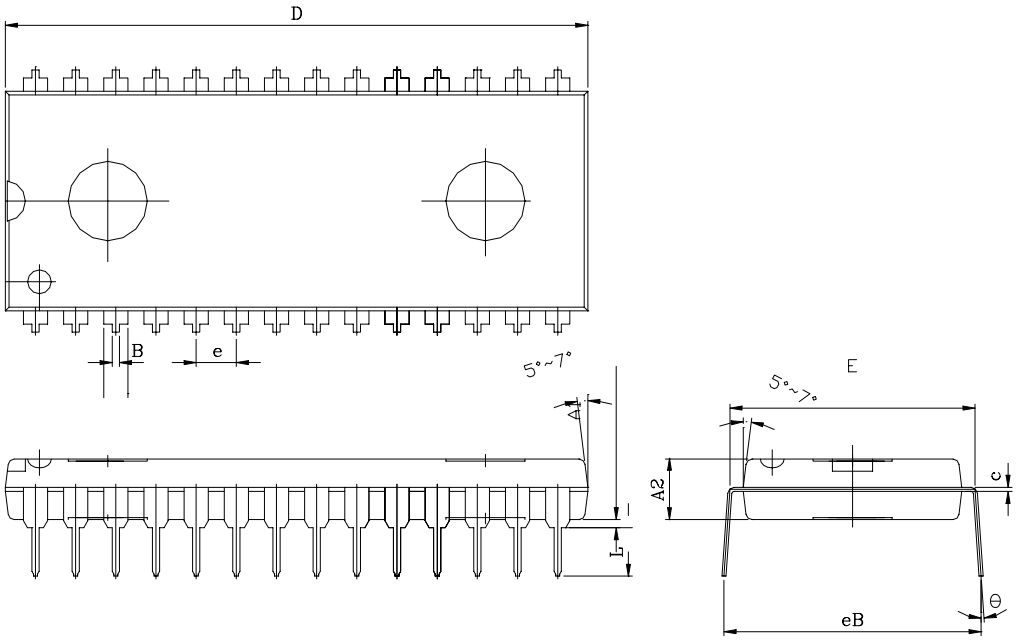


Low Vcc Data Retention Waveform (2) (CE2 controlled)



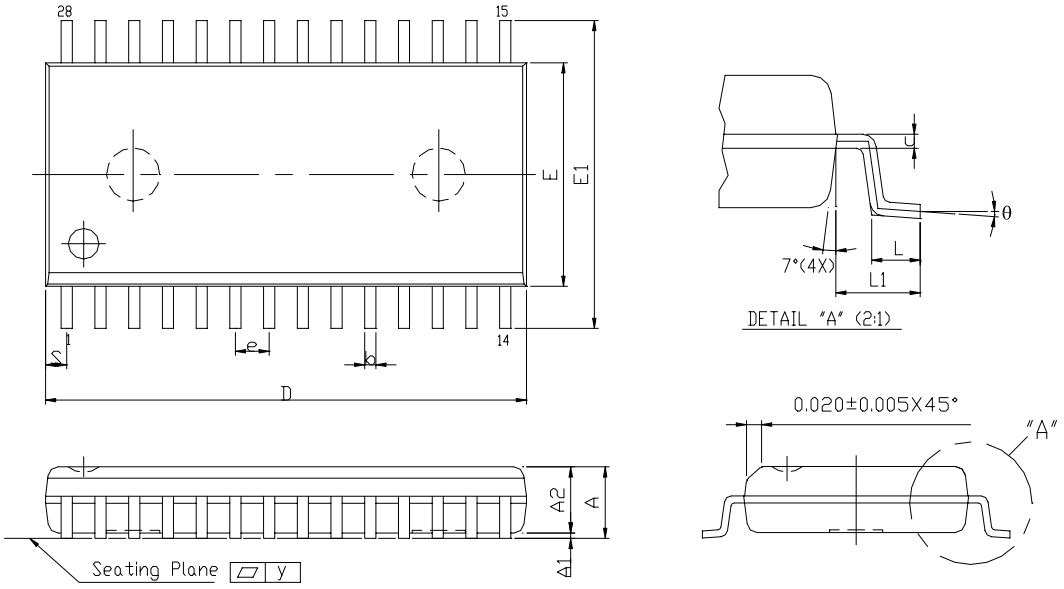
PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



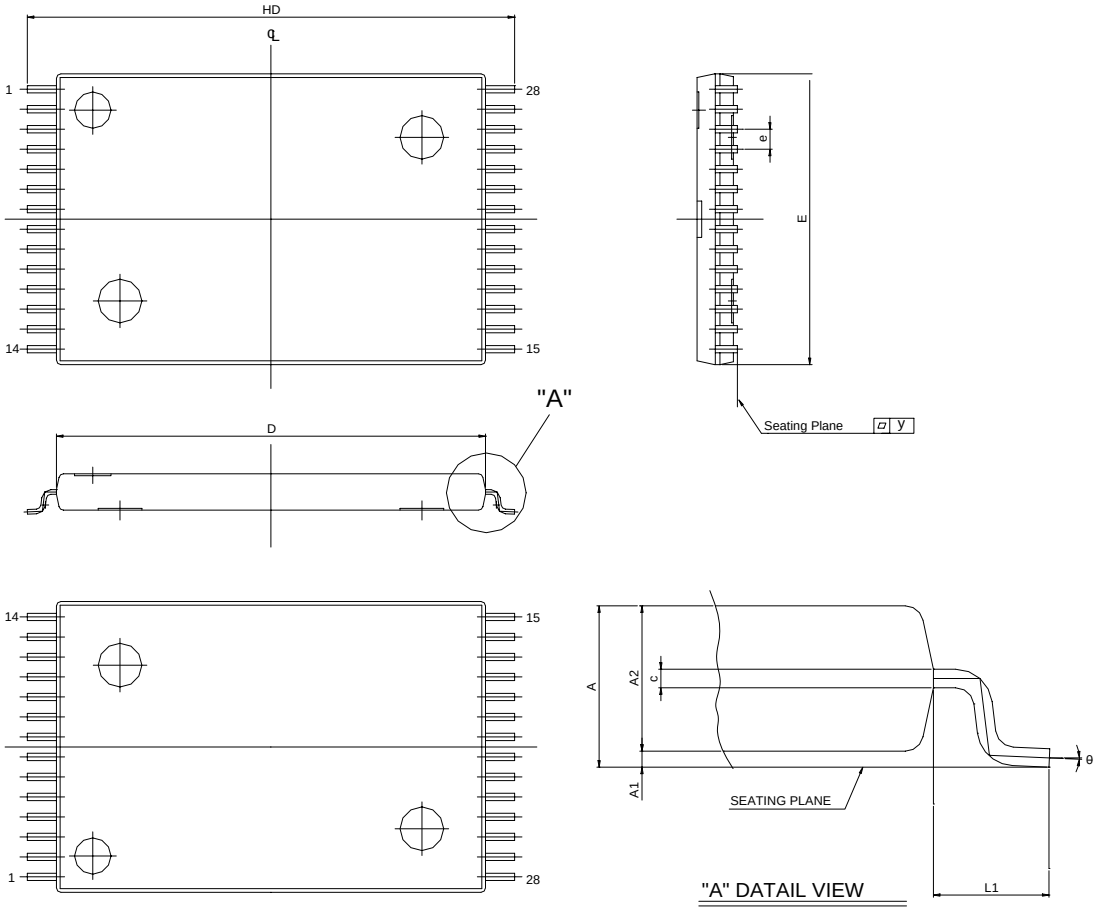
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.150±0.001	3.810±0.254
B	0.018±0.005	0.457±0.127
c	0.010±0.004	0.254±0.102
D	1.460±0.005	37.084±0.127
E	0.600±0.010	15.240±0.254
e	0.100 (TYP)	2.540(TYP)
eB	0.640±0.03	16.256±0.762
L	0.130±0.010	3.302±0.254
θ	0°~15°	0°~15°

28 pin 330 mil SOP Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.112 (MAX)	2.845 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016 (TYP)	0.406(TYP)
c	0.010 (TYP)	0.254(TYP)
D	0.713±0.005	18.110±0.127
E	0.331±0.005	8.407±0.127
E1	0.465±0.012	11.811±0.305
e	0.050 (TYP)	1.270(TYP)
L	0.0404±0.008	1.0255±0.203
L1	0.067±0.008	1.702 ±0.203
S	0.047 (MAX)	1.194 (MAX)
y	0.003(MAX)	0.076(MAX)
θ	0^o 10^o	0^o 10^o

28 pin 8x13.4mm STSOP Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
D	0.465 ±0.004	11.800 ±0.100
E	0.315 ±0.004	8.000 ±0.100
e	0.022 (TYP)	0.55 (TYP)
HD	0.528 ±0.008	13.40 ±0.20.
L1	0.0315 ±0.004	0.80 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0^o 5^o	0^o 5^o

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA)	PACKAGE
UT62257CPC-70	70	5 mA	28 PIN PDIP
UT62257CPC-70L	70	100 μA	28 PIN PDIP
UT62257CPC-70LL	70	40 μA	28 PIN PDIP
UT62257CSC-35	35	5 mA	28 PIN SOP
UT62257CSC-35L	35	100 μA	28 PIN SOP
UT62257CSC-35LL	35	40 μA	28 PIN SOP
UT62257CSC-70	70	5 mA	28 PIN SOP
UT62257CSC-70L	70	100 μA	28 PIN SOP
UT62257CSC-70LL	70	40 μA	28 PIN SOP
UT62257CLS-35L	35	100 μA	28 PIN STSOP
UT62257CLS-35LL	35	50 μA	28 PIN STSOP
UT62257CLS-70L	70	100 μA	28 PIN STSOP
UT62257CLS-70LL	70	40 μA	28 PIN STSOP

ORDERING INFORMATION (for lead free product)

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA)	PACKAGE
UT62257CPCL-70	70	5 mA	28 PIN PDIP
UT62257CPCL-70L	70	100 μA	28 PIN PDIP
UT62257CPCL-70LL	70	40 μA	28 PIN PDIP
UT62257CSCL-35	35	5 mA	28 PIN SOP
UT62257CSCL-35L	35	100 μA	28 PIN SOP
UT62257CSCL-35LL	35	40 μA	28 PIN SOP
UT62257CSCL-70	70	5 mA	28 PIN SOP
UT62257CSCL-70L	70	100 μA	28 PIN SOP
UT62257CSCL-70LL	70	40 μA	28 PIN SOP
UT62257CLSL-35L	35	100 μA	28 PIN STSOP
UT62257CLSL-35LL	35	50 μA	28 PIN STSOP
UT62257CLSL-70L	70	100 μA	28 PIN STSOP
UT62257CLSL-70LL	70	40 μA	28 PIN STSOP

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