N-CHANNEL SILICON FET

Symmetrical n-channel silicon epitaxial planar junction field-effect transistor in a microminiature plastic envelope. The transistor is intended for low level general purpose amplifiers in thick and thin-film circuits.

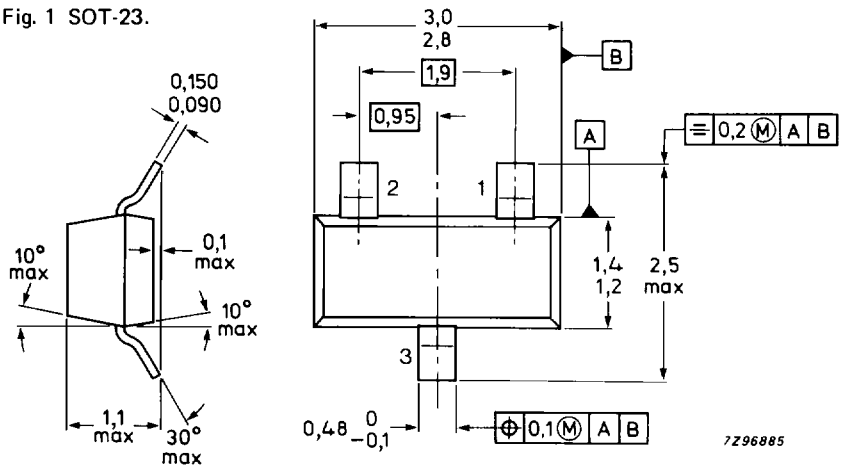
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Total power dissipation up to T_{amb} = 40 °C	P_{tot}	max.	250 mW
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	> <	0,2 mA 1,5 mA
Transfer admittance (common source) I_D = 0,2 mA; V_{DS} = 10 V; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5 mS
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; B = 0,6 to 100 Hz	V_n	<	0,5 μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-23.



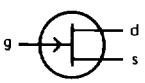
TOP VIEW

Marking code

BFT46 = M3

Pinning

1 = drain
2 = source
3 = gate



Note : Drain and source are interchangeable.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Drain current	I_D	max.	10 mA
Gate current	I_G	max.	5 mA
Total power dissipation up to T_{amb} = 40 °C *	P_{tot}	max.	250 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient*	$R_{th\ j\text{-}a}$	=	430 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Gate cut-off current			
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0,2 nA
Drain current			
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,2 mA
		<	1,5 mA
Gate-source voltage			
I_D = 50 μA; V_{DS} = 10 V	$-V_{GS}$	>	0,1 V
		<	1,0 V
Gate-source cut-off voltage			
I_D = 0,5 nA; V_{DS} = 10 V	$-V_{(P)GS}$	<	1,2 V
y-parameters at f = 1 kHz;			
V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	1,0 mS
Output admittance	$\lvert y_{os} \rvert$	<	10 μS
V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C			
Transfer admittance	$\lvert y_{fs} \rvert$	>	0,5 mS
Output admittance	$\lvert y_{os} \rvert$	<	5 μS

* Mounted on a ceramic substrate of 8 mm x 10 mm x 0,7 mm.

Input capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{is}	<	5 pF
Feedback capacitance at f = 1 MHz; V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C	C_{rs}	<	1,5 pF
Equivalent noise voltage V_{DS} = 10 V; I_D = 200 μA; T_{amb} = 25 °C B = 0,6 to 100 Hz	V_n	<	0,5 μV

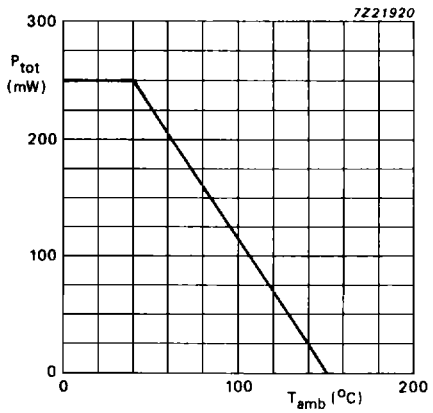


Fig.2 Power derating curve.

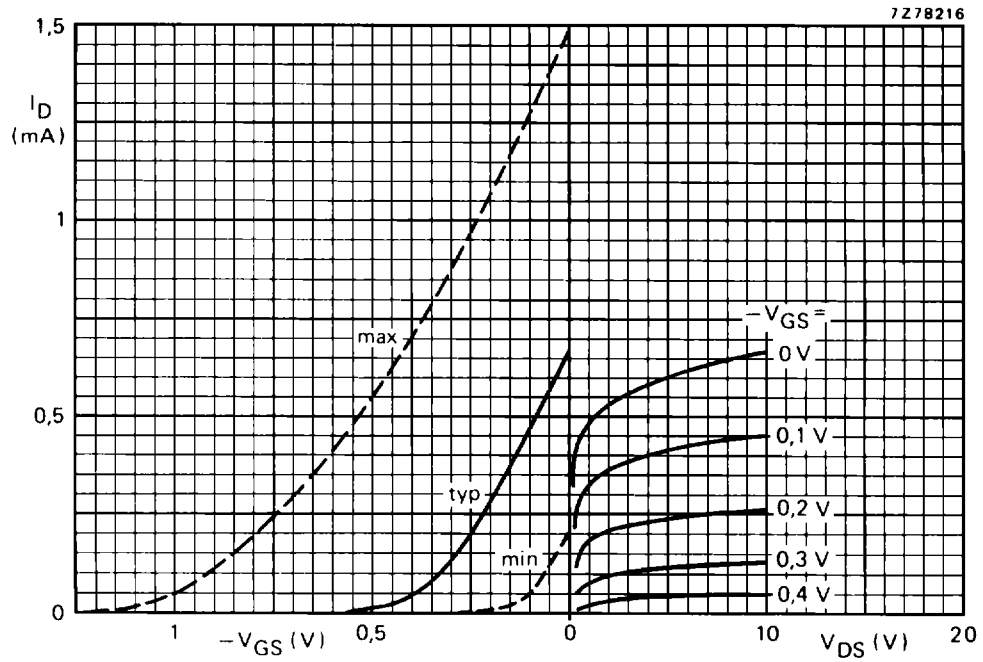


Fig. 3 Typical values. V_{DS} = 10 V; T_j = 25 °C.

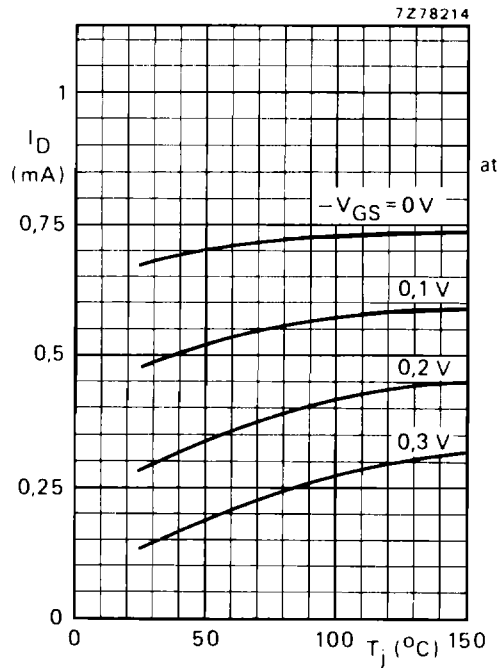


Fig. 4 Typical values. V_{DS} = 10 V.

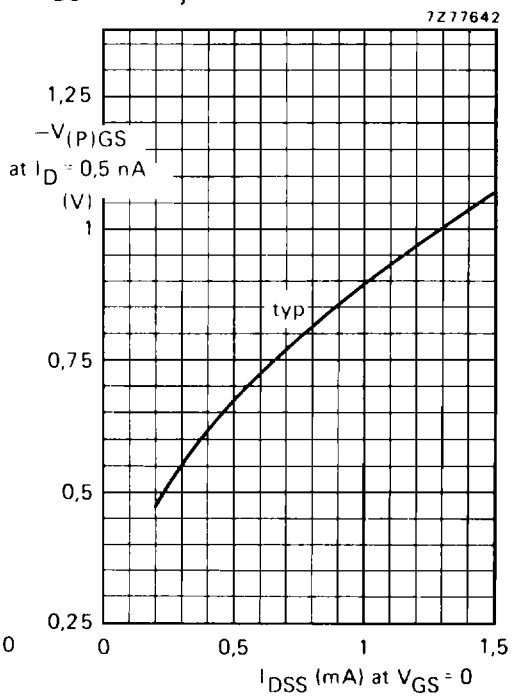


Fig. 5 Correlation between $-V_{(P)GS}$ and I_{DSS}. V_{DS} = 10 V; T_j = 25 °C.

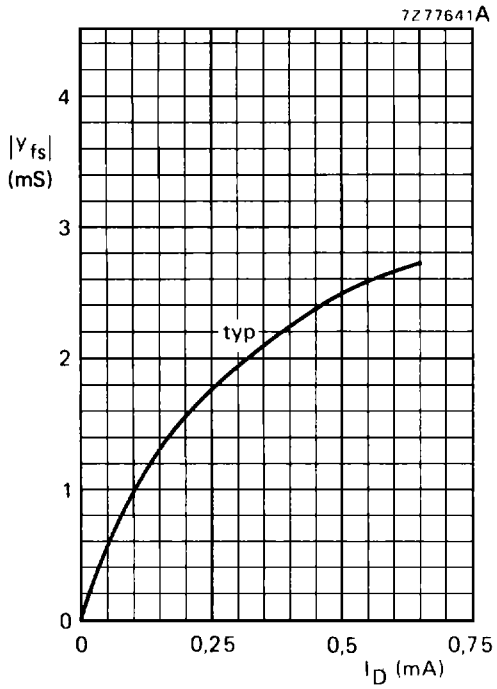


Fig. 6

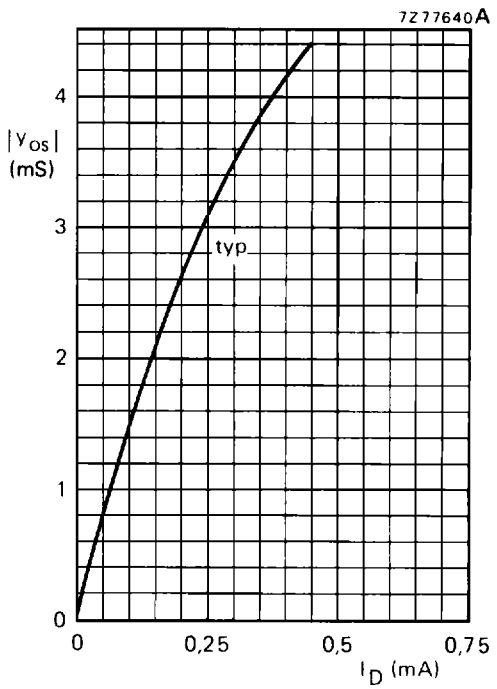


Fig. 7

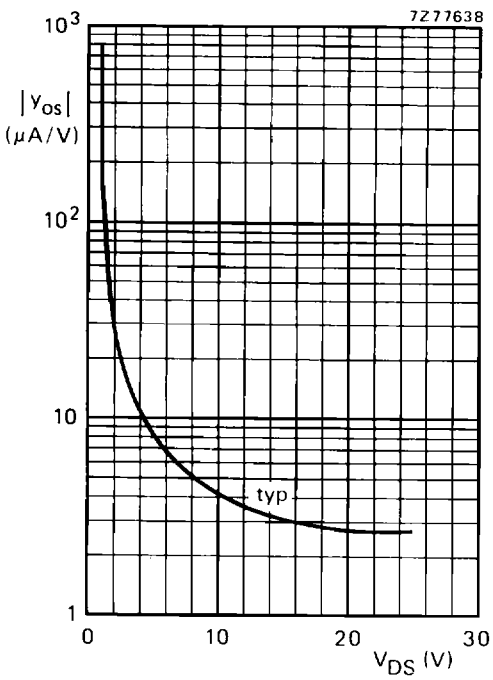


Fig. 8

Fig. 6 $|y_{fs}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 7 $|y_{os}|$ versus I_D.
V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C.

Fig. 8 $|y_{os}|$ versus V_{DS}.
I_D = 0,4 mA; f = 1 kHz; T_{amb} = 25 °C.

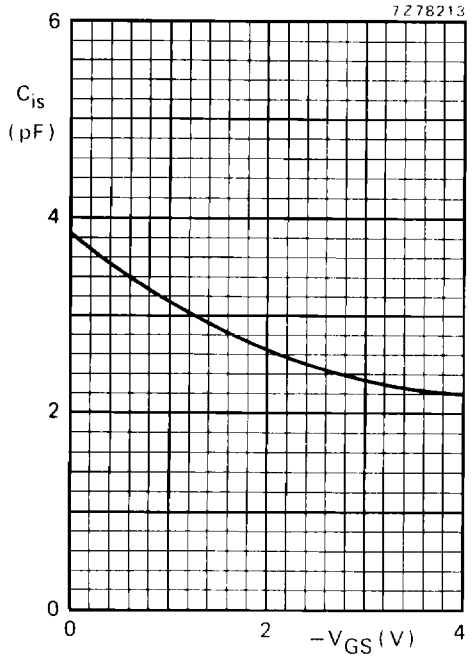


Fig. 9

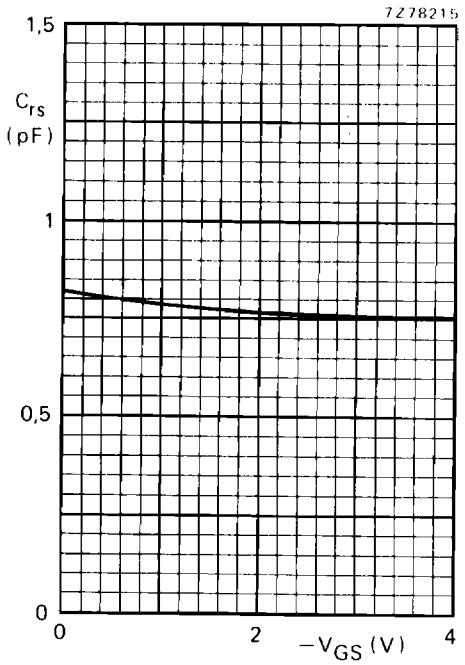


Fig. 10

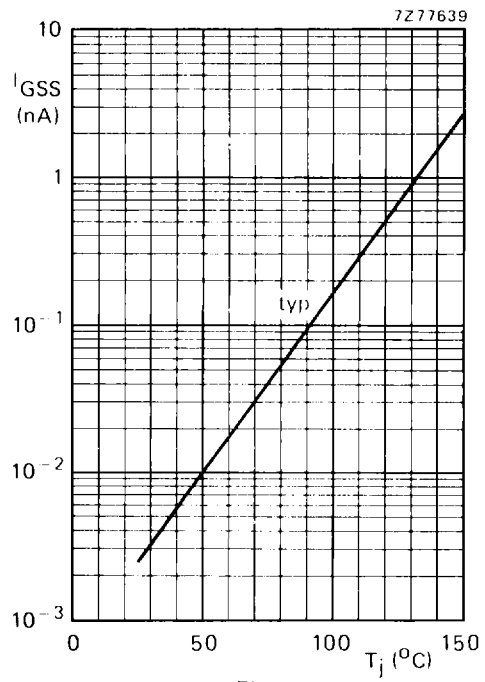


Fig. 11

Fig. 9 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 10 Typical values.
V_{DS} = 10 V, T_{amb} = 25 °C.

Fig. 11 I_{GSS} versus T_j.
$-V_{GSS}$ = 10V; V_{DS} = 0.

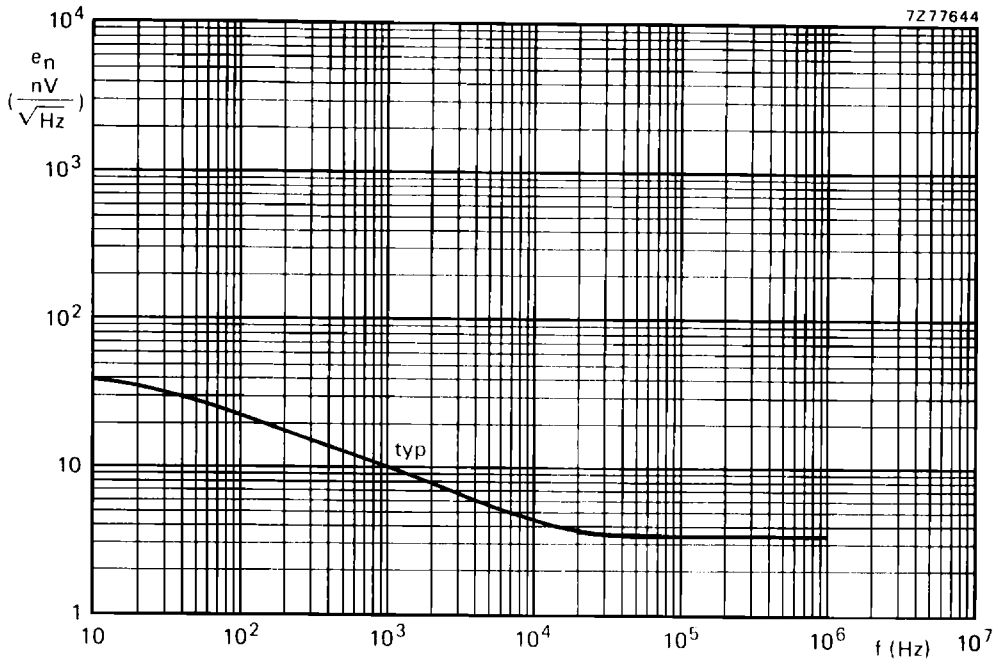


Fig. 12 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.

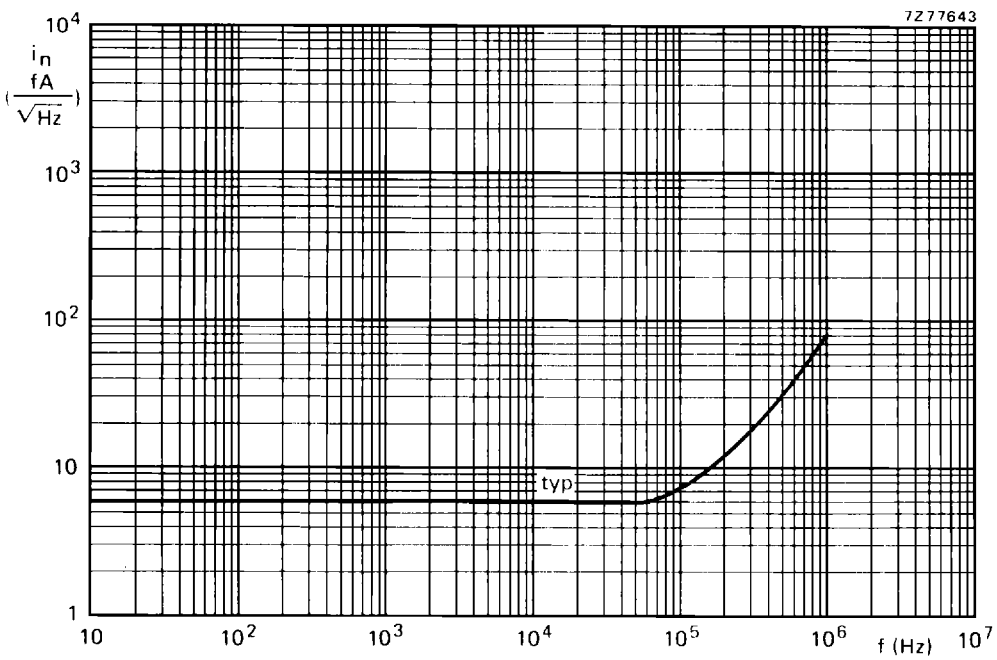


Fig. 13 V_{DS} = 10 V; I_D = 0,2 mA; T_{amb} = 25 °C.