MIL-M-38510/208C
31 January 1984
SUPERSEDING
MIL-M-38510/208B
16 August 1982

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, 4096-BIT SCHOTTKY, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, PROM microcircuits which employ thin film nichrome resistors or titanium-tungsten as the fusible link or programming element. Three product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the part number. Special test requirements are included in this specification to evaluate the quality of the passivation layer (see group B water drop test of 4.4.2a) and to screen against devices which may contain excess moisture in the package materials or internal atmosphere (see freeze-out test of 4.2d).

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	512 word/8 bits per word PROM with uncommitted collector
02	512 word/8 bits per word PROM with active pull-up and a choice third high-impedance state output
03	512 word/8 bits per word PROM with active pull-up and a third high-impedance state output
04	512 word/8 bits per word PROM with uncommitted collector
05	512 word/8 bits per word PROM with active pull-up and a third high-impedance state output

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
J	D-3 (24-lead, 1/2" x 1-1/4"), dual-in-line package
K	F-6 (24-lead, 3/8" x 5/8"), flat package
X	See figure 1 (24-lead, 3/8" x 3/8"), flat package
Y	See figure 2 (20-lead, 5/16" x 1.0"), dual-in-line package
Z	C-3 (24 terminal, .400" x .400"), chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range - - - - - - - - - - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range- - - - - - - - - - - - - - -	-1.5 V dc at -10 mA to +5.5 V dc
Storage temperature range- - - - - - - - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds) - - -	+300°C

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

Thermal resistance, junction-to-case (θ_{JC}) 1/:
  Cases J, K, and Y- - - - - - - - - - - - - - 30°C/W
  Cases X and Z- - - - - - - - - - - - - - - - 36°C/W
Output voltage - - - - - - - - - - - - - - - - -0.5 V dc to $+V_{CC}$
Output sink current- - - - - - - - - - - - - 100 mA
Maximum power dissipation (P_D) 2/- - - - - - 1.02 W
Maximum junction temperature (T_J)- - - - - - 175°C

1.4 Recommended operating conditions.

Supply voltage - - - - - - - - - - - - - - - 4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage - - - - - 2.0 V dc
Maximum low-level input voltage- - - - - - 0.8 V dc
Normalized fanout (each output)- - - - - - 8 mA 3/
Case operating temperature range - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein. When manufacturer programmed devices are delivered to the user, an altered item drawing shall be prepared by the contracting activity to specify the required program configuration.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.2 Truth table.

1/ Heat sinking is recommended to reduce the junction temperature.

2/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).

3/ 16 mA for circuit F devices.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/2/	Device type	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2 mA	02,03,05	2.4	---	V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA 3/	All	---	0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V, I_{IN} = -10 mA, T_C = 25°C	All	---	-1.5	V
Maximum collector cut-off current	I_{CEX}	V_{CC} = 5.5 V, V_O = 5.2 V	01,04	---	100	µA
High-impedance (off-state) output high current	I_{OHZ}	V_{CC} = 5.5 V, V_O = 5.2 V	02,03,05	---	100	µA
High-impedance (off-state) output low current	I_{OLZ}	V_{CC} = 5.5 V, V_O = 0.5 V	02,03,05		-100	µA
High-level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 5.5 V	All	---	50	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 4.5 V, special programming pin	All	---	100	µA
Low-level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V	All	-1.0	-250	µA
	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.5 V, for CE_3 and CE_4	01,02	-1.0	-1000	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V, V_O = 0.0 V 4/	02,03,05	-10	-100	mA
Supply current	I_{CC}	V_{CC} = 5.5 V, V_{IN} = 0, outputs = open	01,02,03	---	185	mA
			04,05	---	155	mA
Propagation delay time, high-to-low level logic, address to output	t_{PHL1}	V_{CC} = 4.5 V and 5.5 V, C_L = 30 pF (see figure 7)	01,02,03	---	90	ns
			04,05	---	80	ns
Propagation delay time, low-to-high level logic, address to output	t_{PLH1}		01,02,03	---	90	ns
			04,05	---	80	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 2/	Device type	Limits Min	Limits Max	Unit
Propagation delay time, high-to-low level logic, enable to output	t_{PHL2}	V_{CC} = 4.5 V and 5.5 V, C_L = 30 pF (see figure 7)	01,02,03	---	50	ns
			04,05	---	40	ns
Propagation delay time, low-to-high level logic, enable to output	t_{PLH2}		01,02,03	---	50	ns
			04,05		40	ns

1/ Complete terminal conditions shall be as specified on table III.

2/ For device type 03, the fusing pins FE_1 and FE_2 may be grounded or floating during operation.

3/ I_{OL} = 16 mA for circuit F devices.

4/ Not more than one output shall be grounded at one time. Output shall be at high logic level prior to test.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III) Class S devices	Class B devices	Class C devices
Interim electrical tests (pre burn-in) (method 5004)	1	1	None
Final electrical tests (method 5004) for unprogrammed devices	1*,2,3,7*, 8	1*,2,3,7*, 8	1
Final electrical tests (method 5004) for programmed devices	1*,2,3,7*, 8,9,10,11	1*,2,3,7*, 8,9	1,7,9
Group A electrical tests (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11	1,2,3,7,8,9, 10,11
Group B electrical tests (method 5005, subgroup 5)	1,2,3,7,8, 9,10,11	N/A	N/A
Group C end-point electrical tests (method 5005)	N/A	1,2,3,7,8	1,2,3,7
Group D end-point electrical tests (method 5005)	1,2,3,7,8	1,2,3,7,8	1,2,3,7

NOTES:
1. * indicates PDA applies to subgroups 1 and 7 (see 4.2c).
2. Any or all subgroups may be combined when using high-speed testers.
3. Subgroups 7 and 8 shall consist of verifying the pattern specified.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 4. When required in group A, B, or C inspection (see 4.4), the devices shall be programmed by the manufacturer prior to test in a checkerboard pattern (a minimum of 50 percent of the total number of bits programmed) or to any altered item drawing pattern which includes at least 25 percent of the total number of bits programmed.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by the altered item drawing.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 5.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics of table I apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be as indicated by the subgroups shown in table II and, where applicable, by the altered item drawing. The subgroup tests shall be as specified in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. For programmed devices, the altered item drawing number shall be added to the marking by the programming activity. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container.

3.7 Processing options. Since the PROM is an unprogrammed device capable of being programmed by either the manufacturer or the user in a wide variety of configurations, two processing options are provided for selection in the contract, using an altered item drawing.

3.7.1 Unprogrammed PROM delivered to the user. All testing shall be verified through group A testing as defined in 3.2.2.1 and tables II and III. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.7.2 Manufacturer-programmed PROM delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 14 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspections. The following additional criteria shall apply:

a. Interim and final electrical tests shall be as specified in table II; the interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

b. Burn-in test (method 1015 of MIL-STD-883, test condition D or E), using the circuit shown on figure 6 or equivalent.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. The freeze-out test shall be conducted as a 100-percent screen on all class S devices having nichrome as the fusible link. Within no more than 24 hours after completion of burn-in and prior to the final electrical test, all devices having nichrome as the fusing link shall be subjected to a freeze-out test. If more than 24 hours have elapsed subsequent to the 125°C burn-in exposure, devices shall be conditioned with at least 125°C for a minimum of 5 hours immediately prior to the freeze-out test. When the freeze-out test is performed, the 25°C final electrical tests shall be completed within 96 hours after the freeze-out test. The freeze-out test shall be conducted as follows:

Step 1. Connect devices in the electrical configuration of figure 9 or in the burn-in configuration of figure 6 with the bias cycled, 3 minutes on and 3 minutes off, throughout the duration of test.

Step 2. Reduce device temperature to T_A = -10°C ±2°C with bias cycled and maintain at that temperature for a minimum of 5 hours.

Step 3. With the cycled bias maintained, allow T_A to go to room temperature (by removal from the cold chamber or termination of forced cooling but with no forced heating) and retain for a minimum of 19 hours subsequent to the completion of the 5-hour cold soak. T_A shall not exceed 35°C during this period.

Step 4. Remove bias and subject all devices to subgroup 1 final electrical tests to establish continuity of the nichrome resistors and remove all failed devices from the lot. Count them as screening rejects subject to the PDA requirements of 4.2c.

e. Class B devices processed to an altered item drawing may be programmed either before or after burn-in at the manufacturer's discretion. The required electrical testing shall include, as a minimum, the final electrical tests for programmed devices as specified in table II herein. Class S devices processed by the manufacturer to an altered item drawing shall be programmed prior to burn-in.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Qualification data for subgroups 7 through 11 shall be by attributes only.

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, then the slower device type may be part I qualified by conducting only group A electrical tests and any electricals specified as additional group C subgroups and submitting data in accordance with MIL-M-38510, appendix D (i.e. groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 shall be omitted.

c. For unprogrammed devices, a sample shall be selected to satisfy the programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming (see 3.2.2.1). If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowed.

d. For unprogrammed devices, 10 devices from the programmability sample shall be subjected to the requirements of group A, subgroups 9, 10, and 11. If more than 2 total devices fail in all three subgroups, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowed.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Electrical tests shall be as specified in table II herein. Class S devices selected for testing in subgroup 5, table IIa of method 5005 of MIL-STD-883, shall be programmed in accordance with 3.2.2.

b. Steady state life test for class S devices shall be in accordance with subgroup 5, table IIa of method 5005 of MIL-STD-883, using a circuit submitted to the qualifying activity for approval. If the alternate burn-in conditions are used, the circuit on figure 6 or equivalent shall be used.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

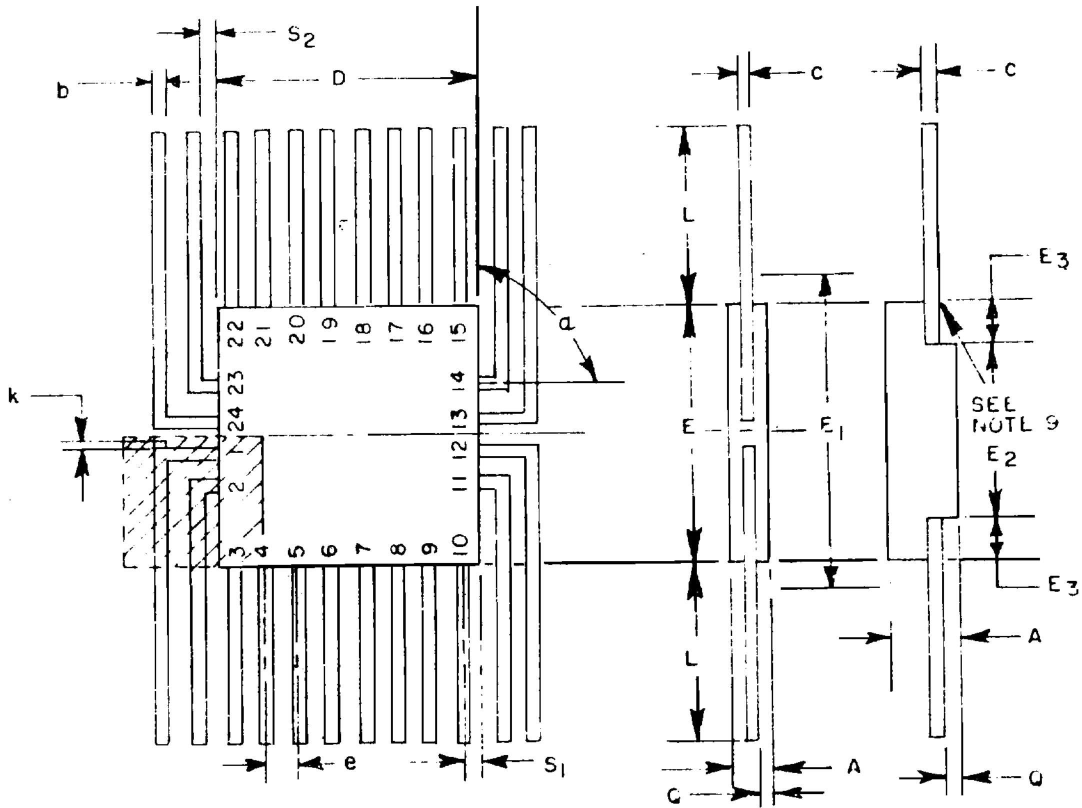
a. End-point electrical tests shall be as specified in table II herein.

b. Steady state life test (method 1005 of MIL-STD-883, test condition D or E), using the circuit shown on figure 6 or equivalent.

(1) T_A = 125°C minimum.

(2) Test duration = 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. For qualification inspection, at least 25 percent of the sample selected for testing in subgroup 1 shall be programmed (see 3.2.2). For quality conformance inspection, the programmability sample (see 4.4.1c) shall be included in the subgroup 1 tests.



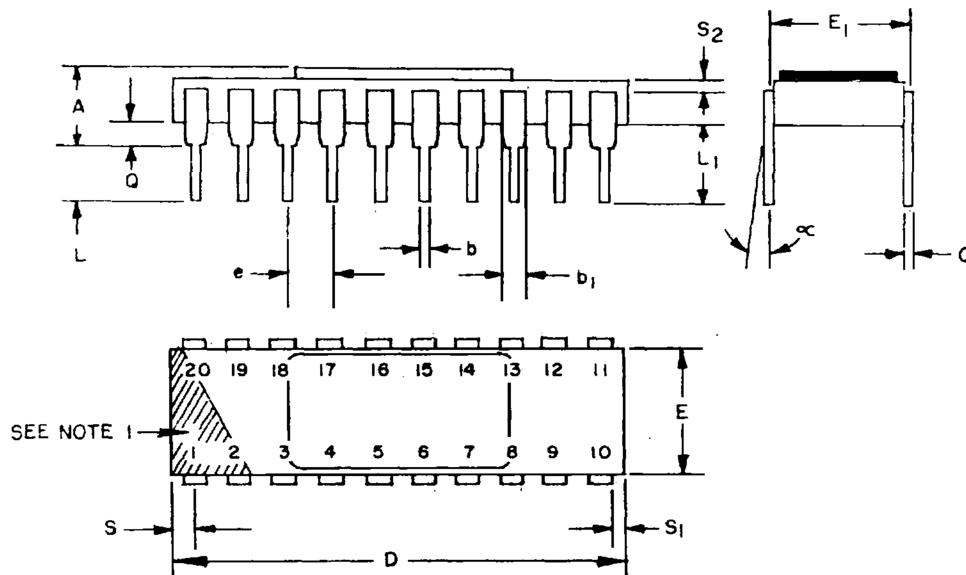
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.045	.090	1.14	2.29	
b	.015	.019	.38	.48	5
c	.003	.006	.08	.15	5
D	---	.400	---	10.16	3
E	.340	.385	8.64	9.78	
E_1	---	.400	---	10.16	3
E_2	.125	---	3.18	---	
E_3	.030	---	.76	---	14
e	.050 BSC		1.27 BSC		4,6
k	.008	.015	.20	.38	10
L	.250	.370	6.35	9.40	
Q	.010	.040	.25	1.02	2
S_1	.005	---	.13	---	7,8
S_2	.005	---	.13	---	11
α	30°	90°	30°	90°	12,13

FIGURE 1. Case outline X (24-lead, 3/8" x 3/8").

NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternatively, a tab (dimension k) may be used to identify pin one.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within ±.005 (.13 mm) of its exact longitudinal position relative to pins 1 and 24.
5. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Twenty-two spaces.
7. Applies to all four corners (leads number 3, 10, 15, and 22).
8. Dimension S_1 may be .000 (.00 mm) if leads number 3, 10, 15, and 22 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body or if the leads are brazed to the metallized ceramic body (see 40.3 of appendix C, MIL-M-38510).
9. Optional configuration; if this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Optional, see note 1. If a pin one identification mark is used in addition to this tab, the minimum limit of dimension k does not apply.
11. Applies to leads number 2, 11, 14 and 23.
12. Lead configuration is optional within dimension E except dimensions b and c apply (see 40.2 of appendix C, MIL-M-38510).
13. Applies to leads number 1, 2, 11, 12, 13, 14, 23, and 24.
14. Applies to all edges.

FIGURE 1. Case outline x (24-lead, 3/8" x 3/8") - Continued.



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	---	.175	---	4.44	
b	.016	.020	.41	.51	11,8
b_1	.040	.060	1.02	1.52	8,2
C	.008	.012	.20	.30	11,8
D	.970	1.010	24.64	25.65	4
E	.280	.300	7.11	7.62	4
E_1	.290	.320	7.37	8.13	7
e	.090	.110	2.29	2.79	5,9
L	.125	.180	3.18	4.58	
L_1	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
S	---	.098	---	2.49	6
S_1	.005	---	.13	---	6
S_2	.005	---	.13	---	8
α	0°	15°	0°	15°	

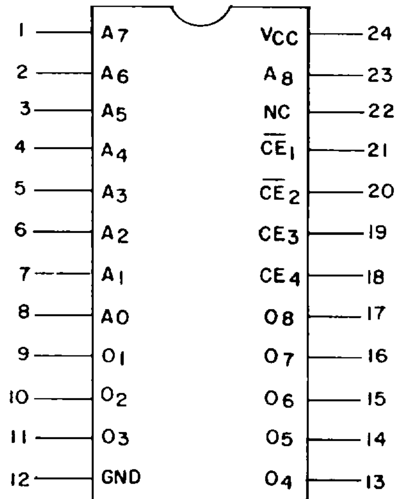
NOTES:

1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minimum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 10, 11, and 20 only.
3. Dimension Q shall be measrued from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 20.
6. Applies to all four corners (leads number 1, 10, 11, and 20) (see 40.5 of appendix C, MIL-M-38510).
7. Lead center when α is 0°. E_1 shall be measured at the centerline of the leads (see 40.4 of appendix C, MIL-M-38510).
8. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
9. Eighteen spaces.
10. No organic or polymeric materials shall be molded to the bottom of the package.
11. Applies to all leads.

FIGURE 2. Case outline Y (20-lead, 5/16" x 1.0").

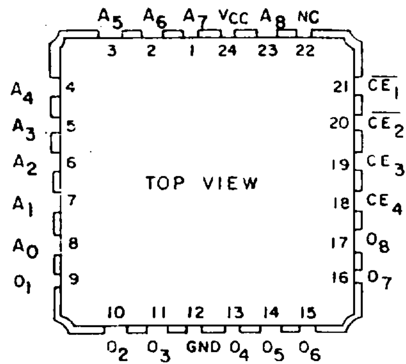
Device types 01, 02

Cases J, K and X



Device types 01, 02

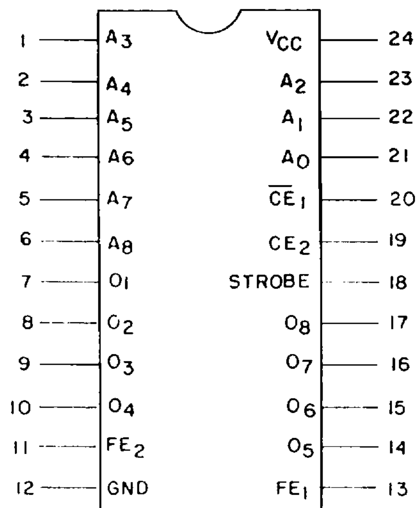
Case Z



OPTION A WITH ACTIVE TERMINALS ON PLANE 1.

Device type 03

Cases J, K and X



Device types 04 and 05

Case Y

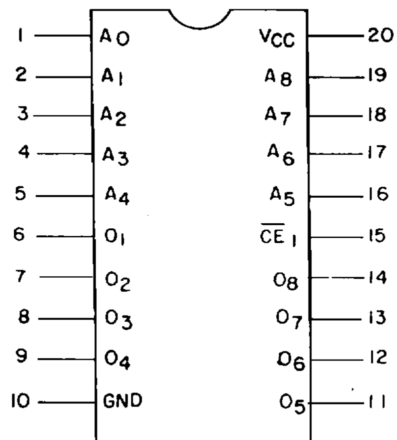


FIGURE 3. Terminal connections.

Device types 01 and 02

WORD NO.	ENABLE				ADDRESS									DATA							
	$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	L	L	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	L	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	H	L	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	L	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC

Device type 03

WORD NO.	ENABLE			ADDRESS									DATA							
	$\overline{CE}_1$	CE_2	STROBE	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	L	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	H	L	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	H	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/
NA	H	H	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	H	L	X	X	X	X	X	X	X	X	X		Last data is latched						

Device types 04 and 05

WORD NO.	ENABLE	ADDRESS									DATA							
	$\overline{CE}_1$	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
NA	H	X	X	X	X	X	X	X	X	X	OC	OC	OC	OC	OC	OC	OC	OC
NA	L	X	X	X	X	X	X	X	X	X	4/	4/	4/	4/	4/	4/	4/	4/

NOTES:
1. NA = Not applicable.
2. X = Input may be high level, low level, or open circuit.
3. OC = Open circuit (high resistance output).
4. The outputs for an unprogrammed device shall be high for circuits A, B, D, and F, and low for circuits C and G.

FIGURE 4. Truth table (unprogrammed).

LOGIC CIRCUIT A
(Device types 01 and 02)

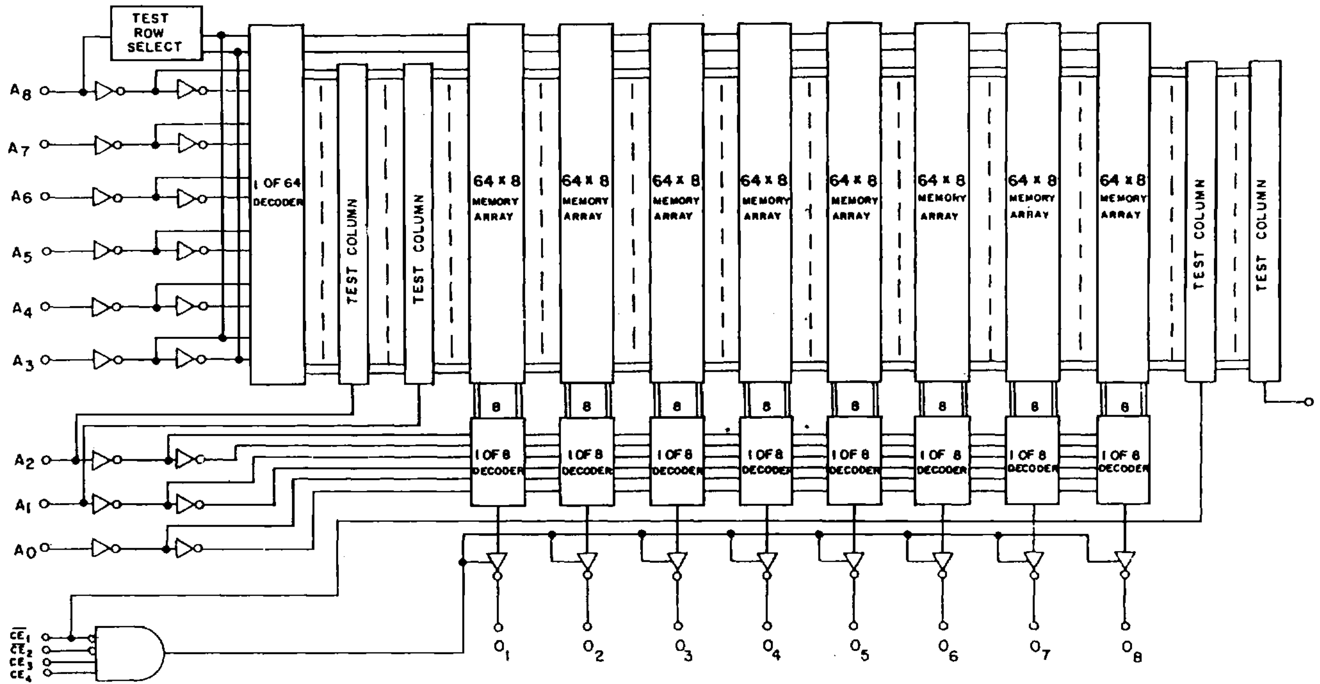


FIGURE 5. Logic diagrams.

LOGIC CIRCUIT B
(Device types 01, 02, 04, & 05) and
LOGIC CIRCUIT F
(Device type 05)

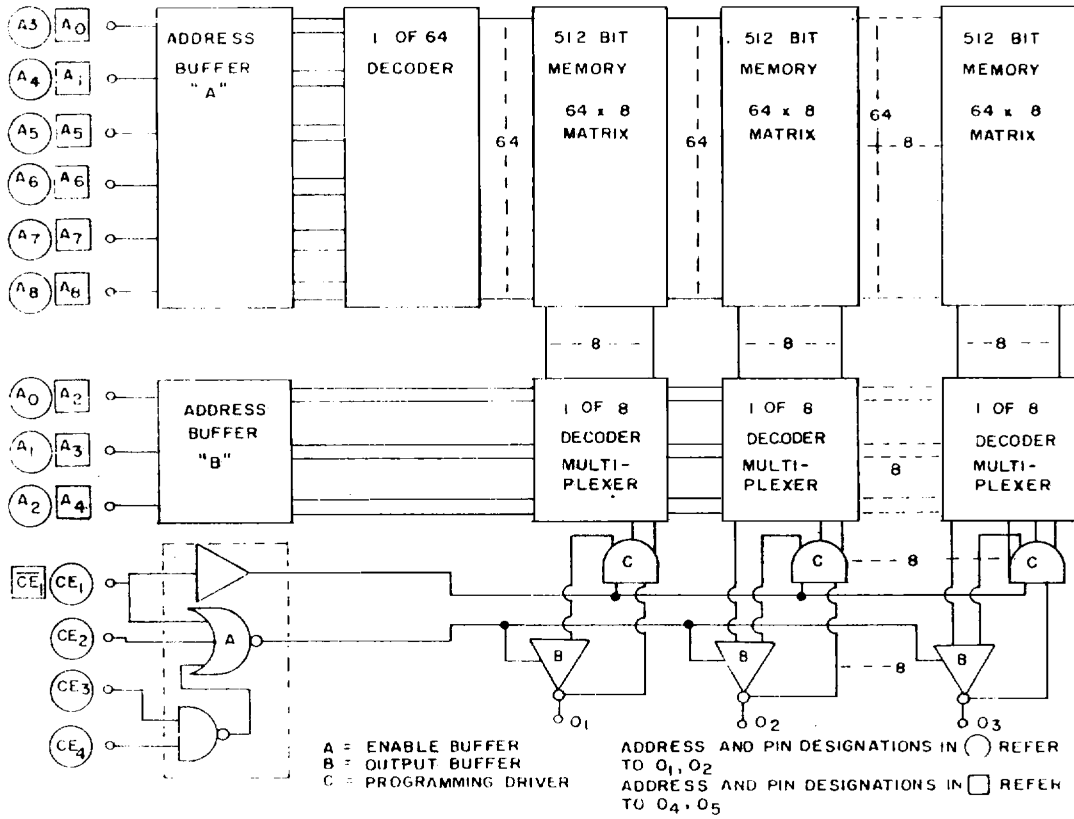


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT C

(Device types 01 and 02)

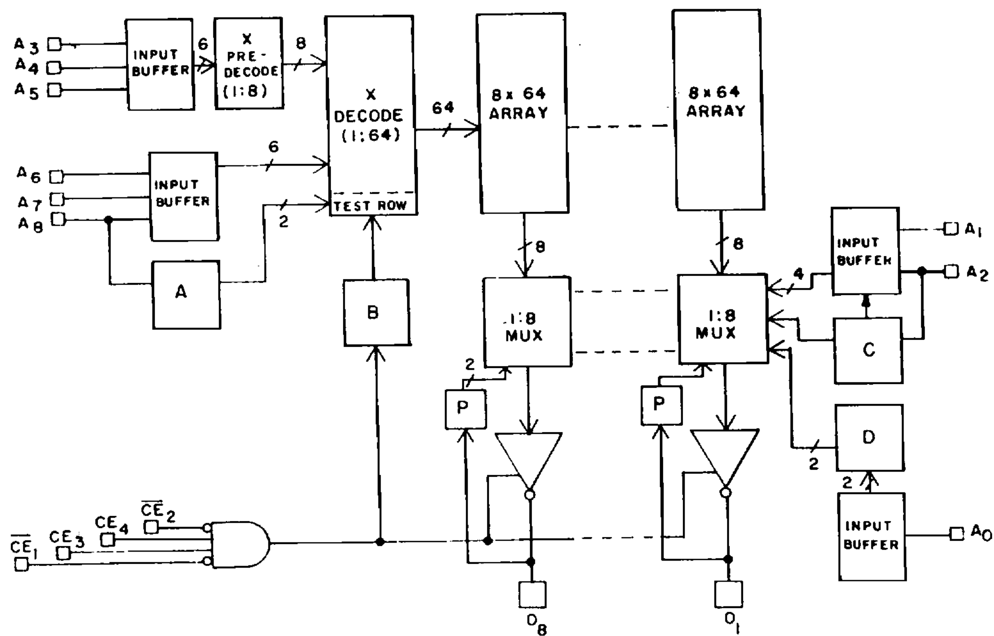


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT C
(Device type 03)

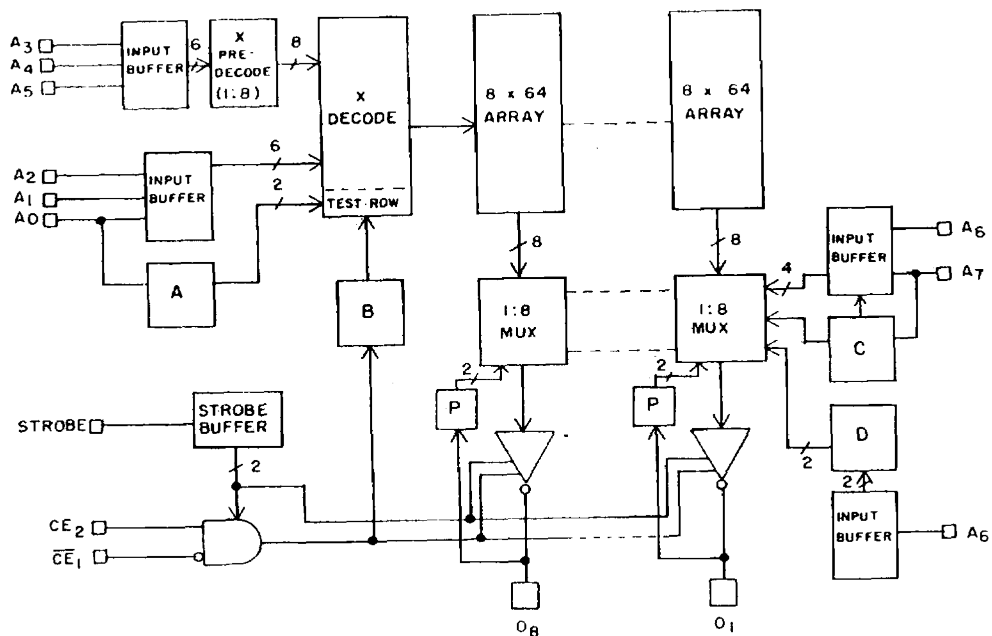


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT D
(Device types 01 and 02)

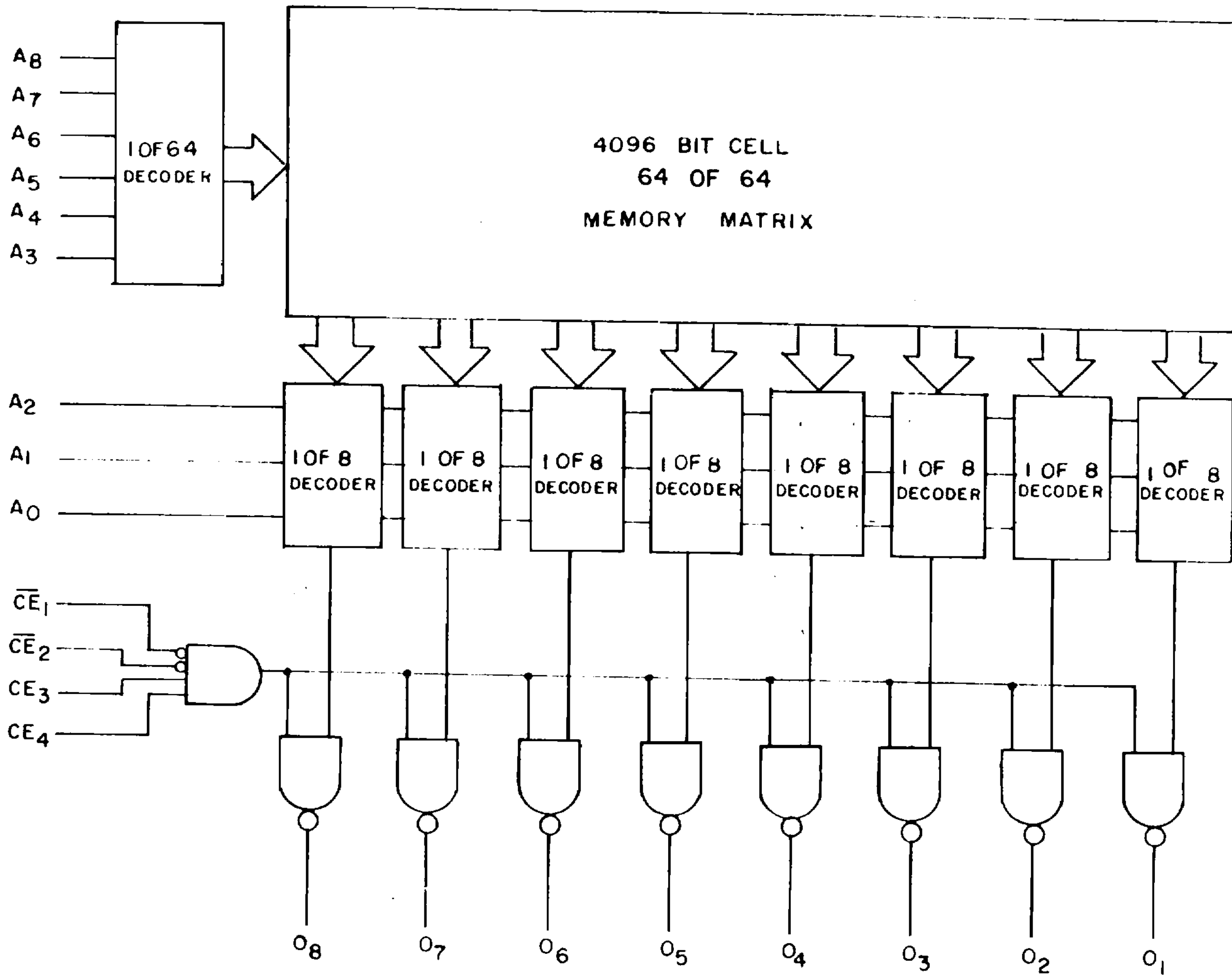


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device type 01)

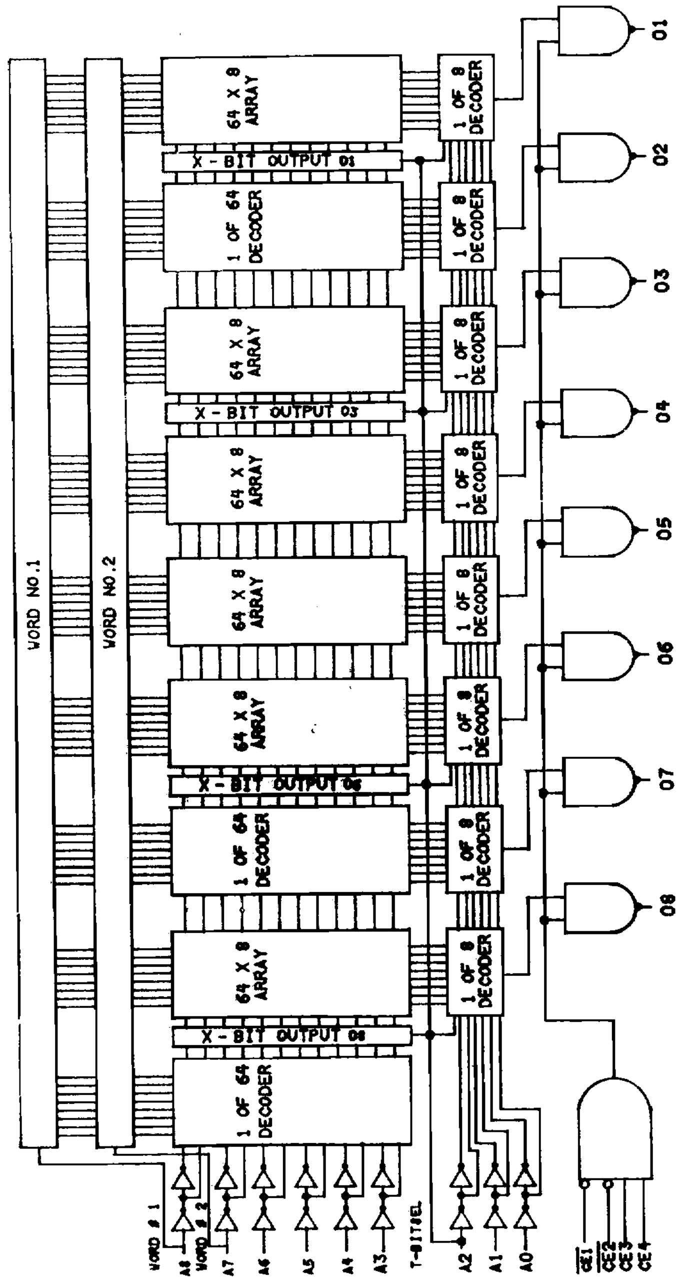


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device type 02)

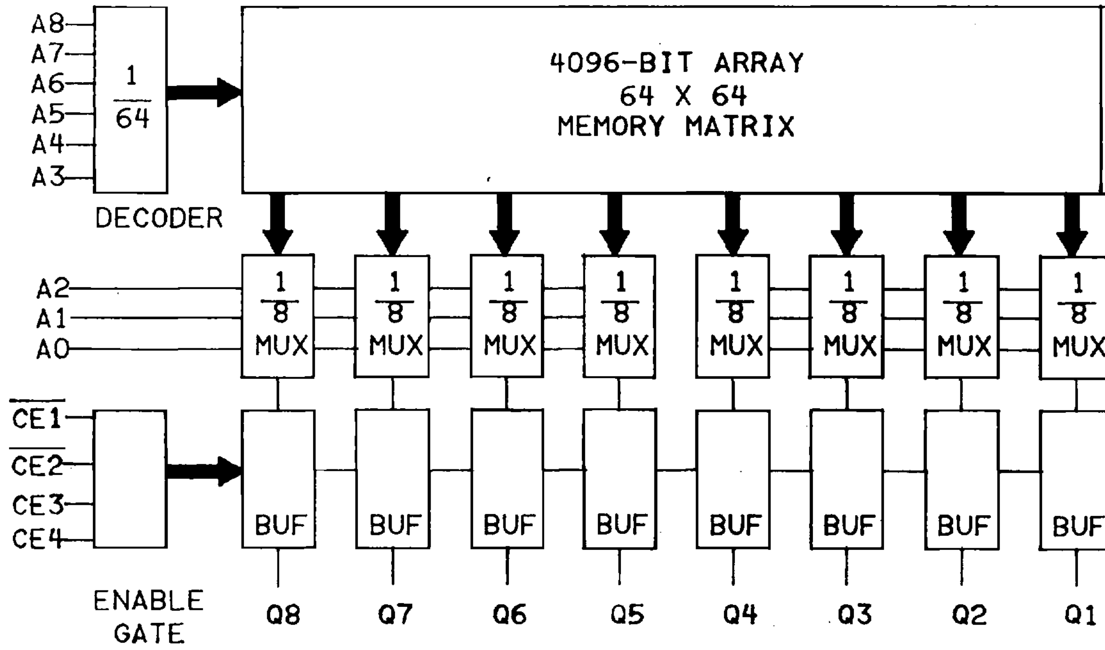


FIGURE 5. Logic diagrams - Continued.

LOGIC CIRCUIT G (Device types 04 and 05)

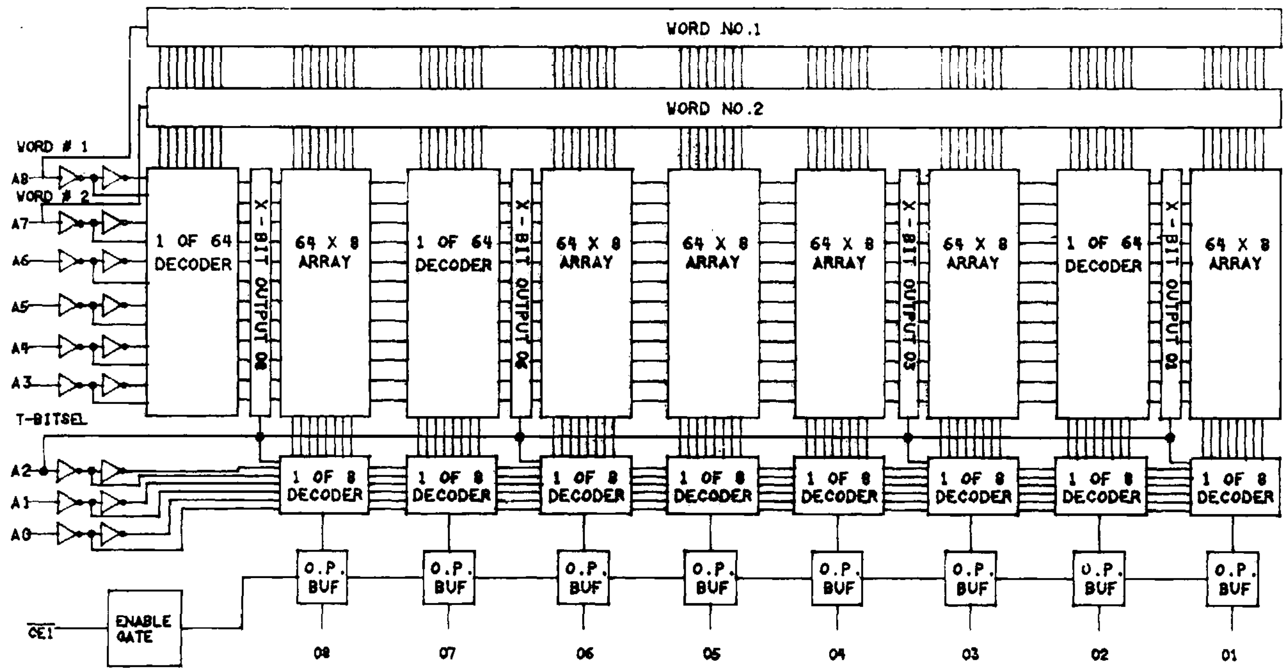
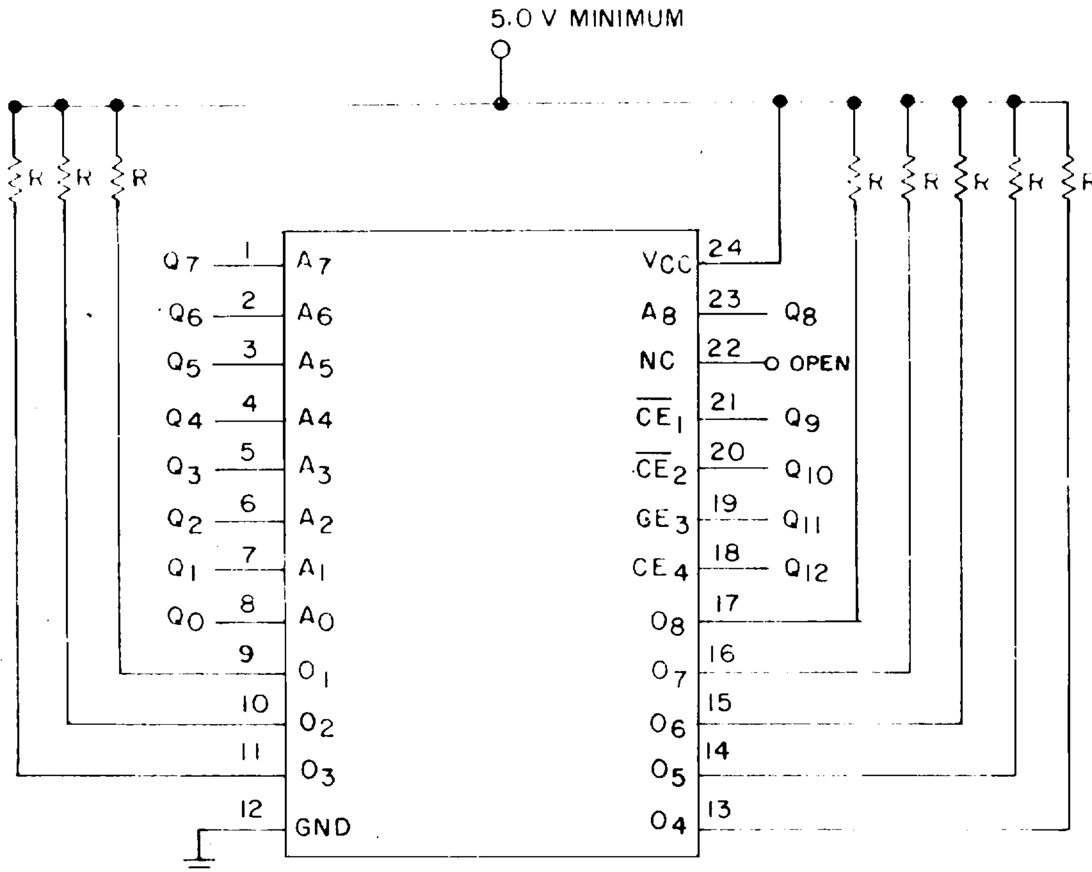


FIGURE 5. Logic diagrams - Continued.

Device types 01 and 02.

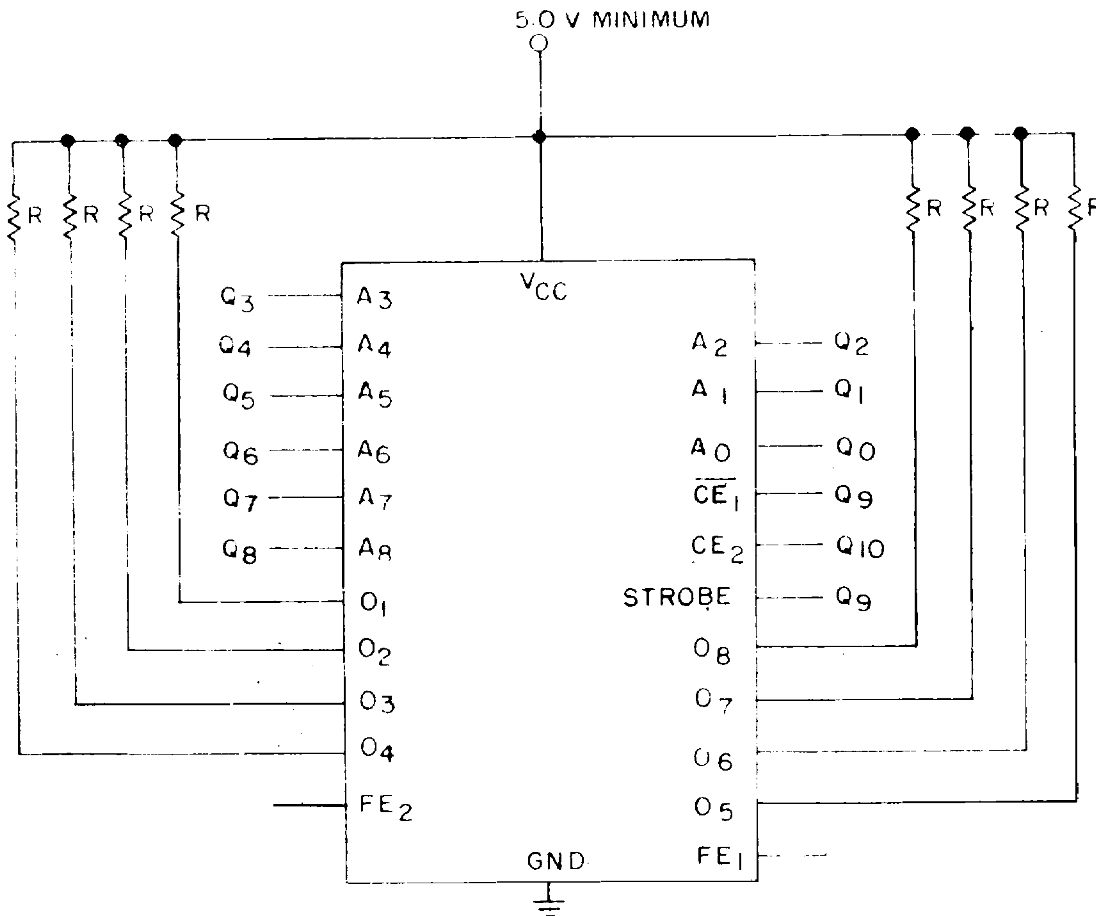


NOTES:
1. R = 560Ω ±5%. All outputs shall have separate identical loads.
2. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
3. All pulse generators have the following characteristics: V_{IL} = -1.5 V minimum to 0.8 V maximum; V_{IH} = 2.0 V minimum to 5.5 V maximum; 50% ±15% duty cycle; and input frequencies as follows:

Input	Frequency (±50%)
Q_0	f_0 = 100 kHz min.
Q_1	$f_1 = 1/2\ f_0$
Q_2	$f_2 = 1/2\ f_1$
Q_3	$f_3 = 1/2\ f_2$
Q_4	$f_4 = 1/2\ f_3$
Q_5	$f_5 = 1/2\ f_4$
Q_6	$f_6 = 1/2\ f_5$
Q_7	$f_7 = 1/2\ f_6$
Q_8	$f_8 = 1/2\ f_7$
Q_9	$f_9 = 1/2\ f_8$
Q_{10}	$f_{10} = 1/2\ f_9$
Q_{11}	$f_{11} = 1/2\ f_{10}$
Q_{12}	$f_{12} = 1/2\ f_{11}$

FIGURE 6. Burn-in and steady state life test circuit.

Device type 03



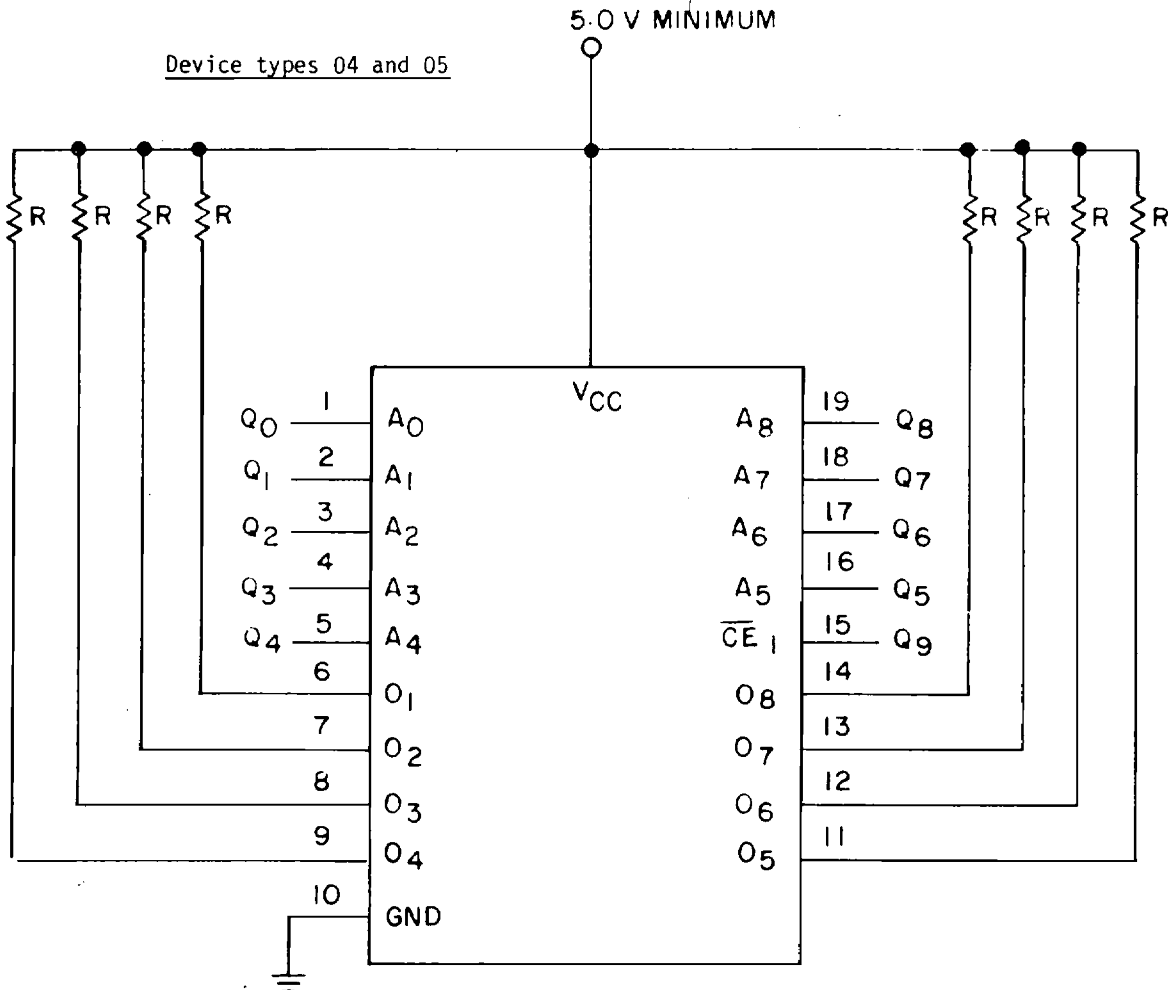
NOTES:

1. R = 560Ω ±5%. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: V_{IL} = -1.5 V minimum to 0.8 V maximum; V_{IH} = 2.0 V minimum to 5.5 V maximum; 50% ±15% duty cycle and frequencies as specified in note 5.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. FE_1 and FE_2 should be GND or open.
5. Input frequencies are as follows:

Input	Frequency (±50%)
Q_0	f_0 = 100 kHz min.
Q_1	f_1 = 1/2 f_0
Q_2	f_2 = 1/2 f_1
Q_3	f_3 = 1/2 f_2
Q_4	f_4 = 1/2 f_3
Q_5	f_5 = 1/2 f_4
Q_6	f_6 = 1/2 f_5
Q_7	f_7 = 1/2 f_6
Q_8	f_8 = 1/2 f_7
Q_9	f_9 = 1/2 f_8
Q_{10}	f_{10} = 1/2 f_9

FIGURE 6. Burn-in and steady state life test circuit - Continued.

Device types 04 and 05

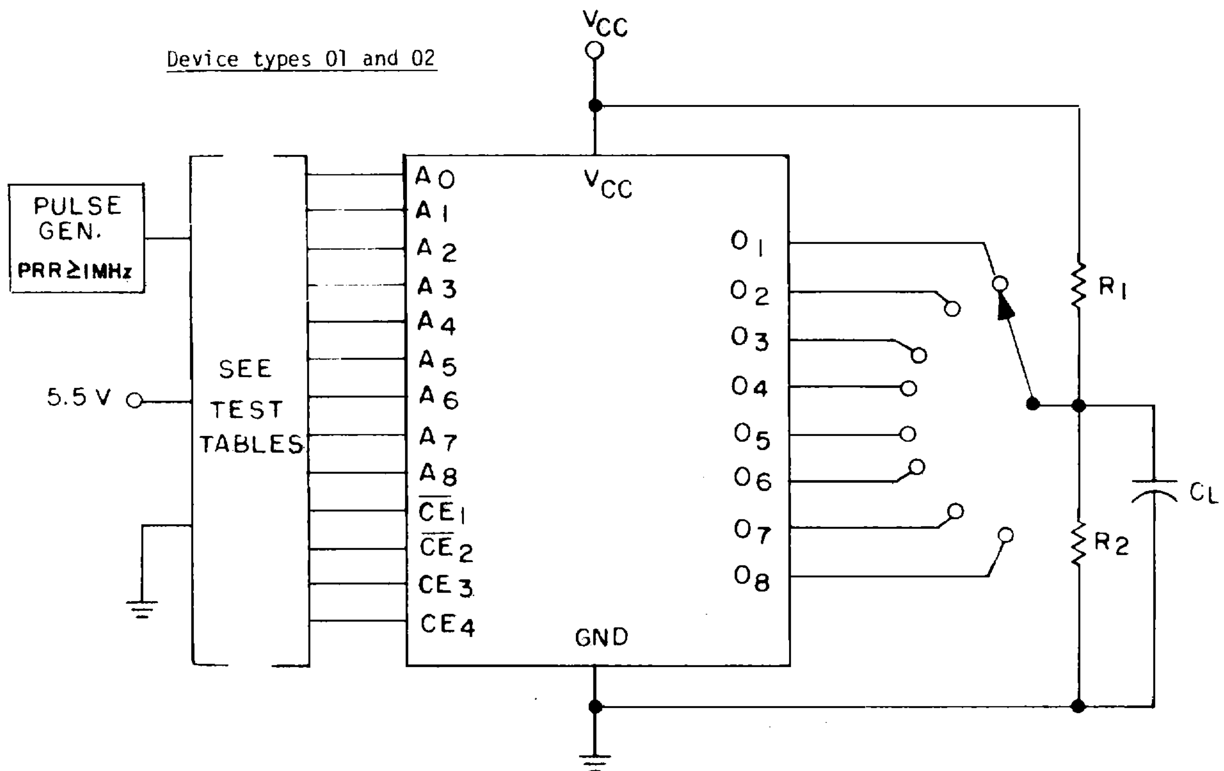


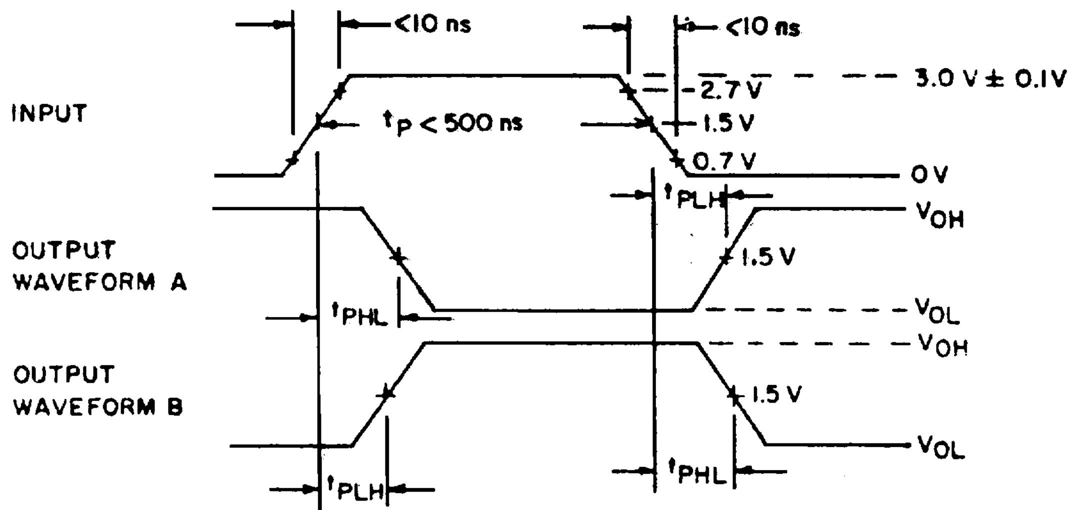
NOTES:

1. R = 560Ω ±5%. All outputs shall have separate identical loads.
2. All pulse generators have the following characteristics: V_{IL} = -1.5 V minimum to 0.8 V maximum; V_{IH} = 2.0 V minimum to 5.5 V maximum; 50% ±15% duty cycle and frequencies as specified in note 4.
3. V_{CC} shall be high enough to insure 5.0 V at the device V_{CC} terminal.
4. Input frequencies are as follows:

Input	Frequency (±50%)
Q_0	f_0 = 100 kHz min.
Q_1	f_1 = 1/2 f_0
Q_2	f_2 = 1/2 f_1
Q_3	f_3 = 1/2 f_2
Q_4	f_4 = 1/2 f_3
Q_5	f_5 = 1/2 f_4
Q_6	f_6 = 1/2 f_5
Q_7	f_7 = 1/2 f_6
Q_8	f_8 = 1/2 f_7
Q_9	f_9 = 1/2 f_8
Q_{10}	f_{10} = 1/2 f_9
Q_{11}	f_{11} = 1/2 f_{10}
Q_{12}	f_{12} = 1/2 f_{11}

FIGURE 6. Burn-in and steady state life test circuit - Continued.

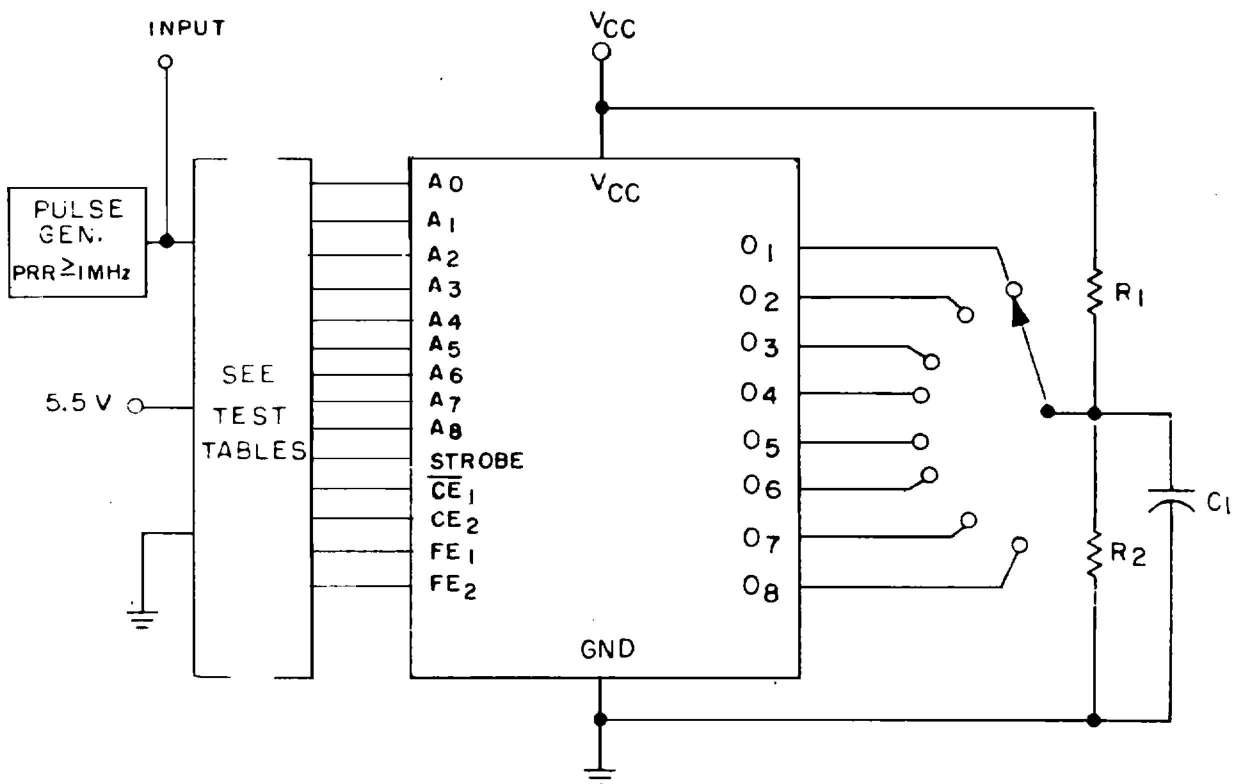


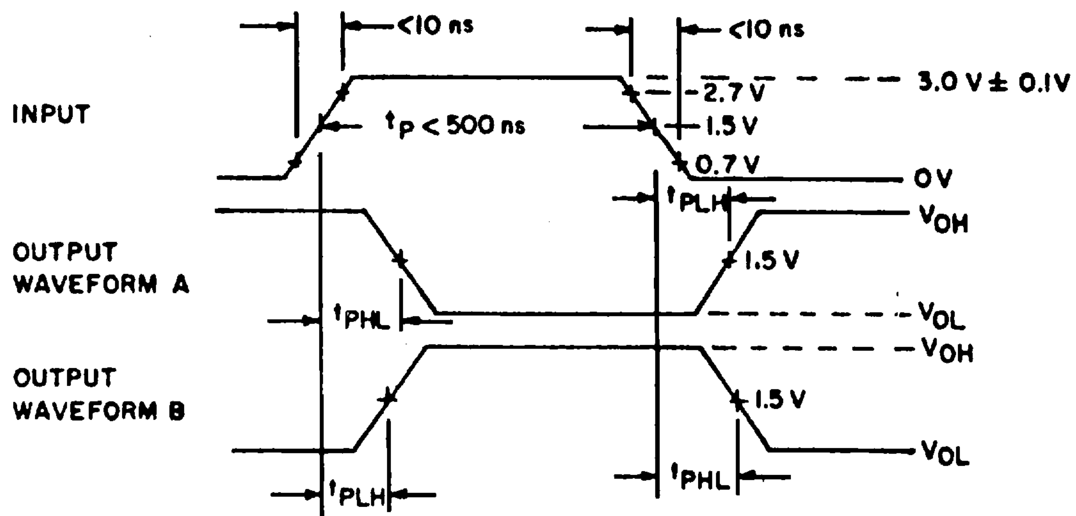


NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance; R_1 = 330Ω ±25% and R_2 = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 7. Switching time test circuit.

Device type 03

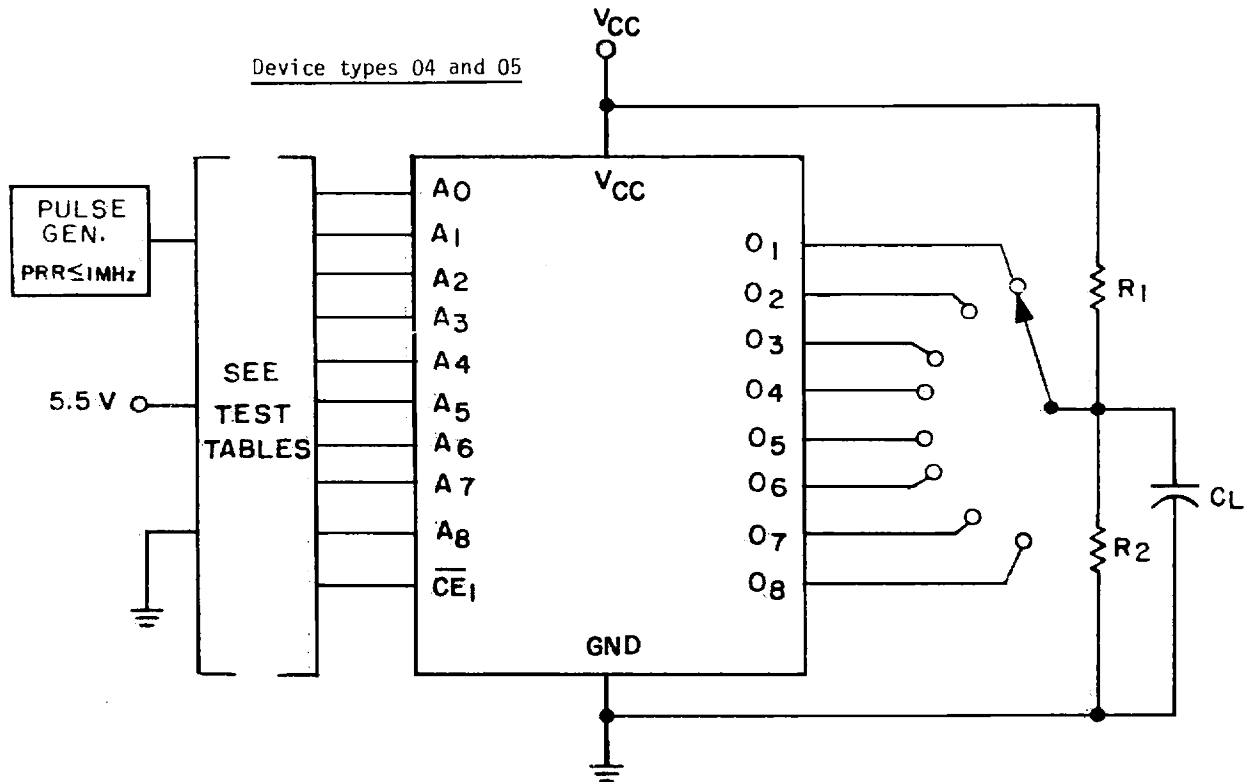


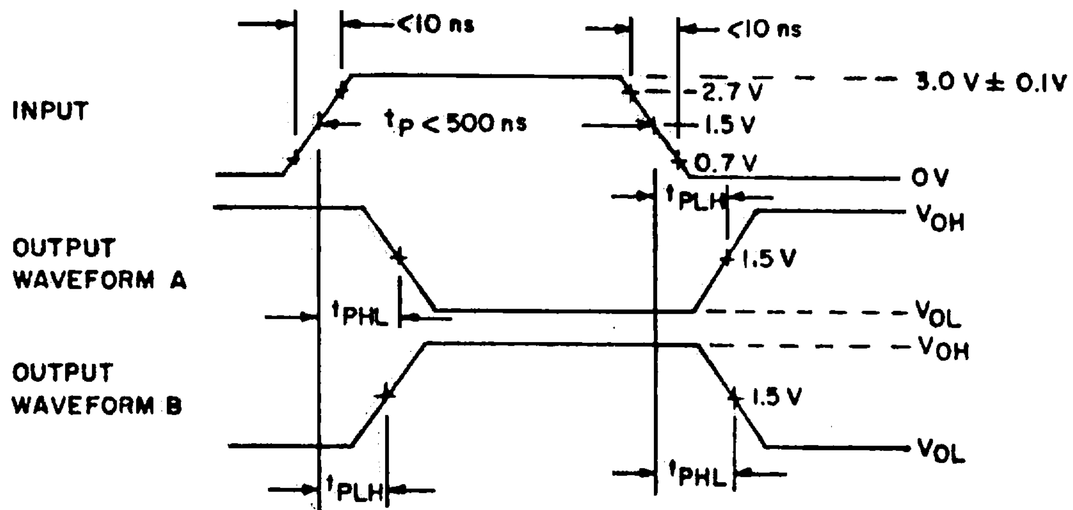


NOTES:
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance; R_1 = 330Ω ±25% and R_2 = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 7. Switching time test circuit - Continued.

Device types 04 and 05

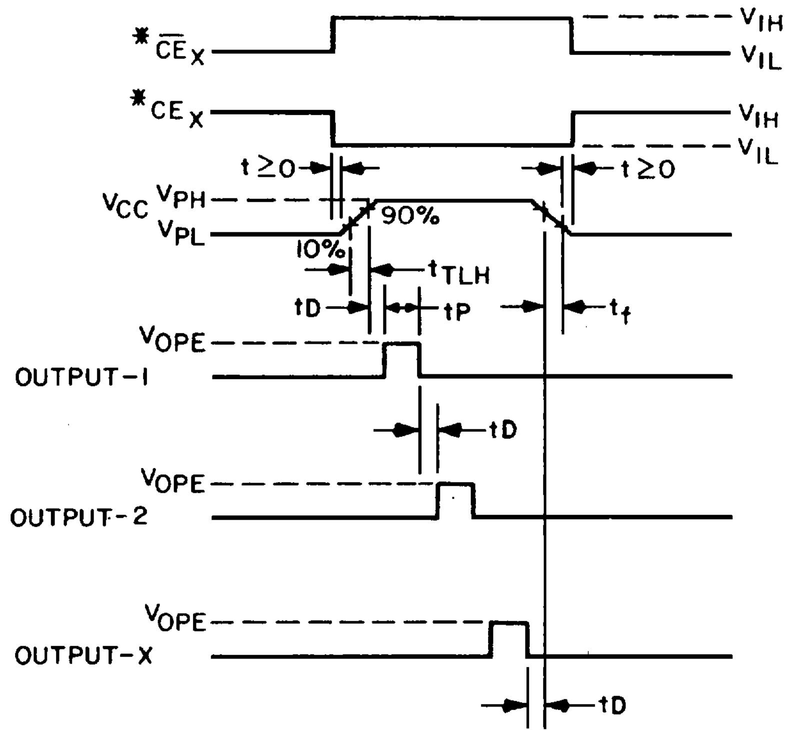




NOTES:

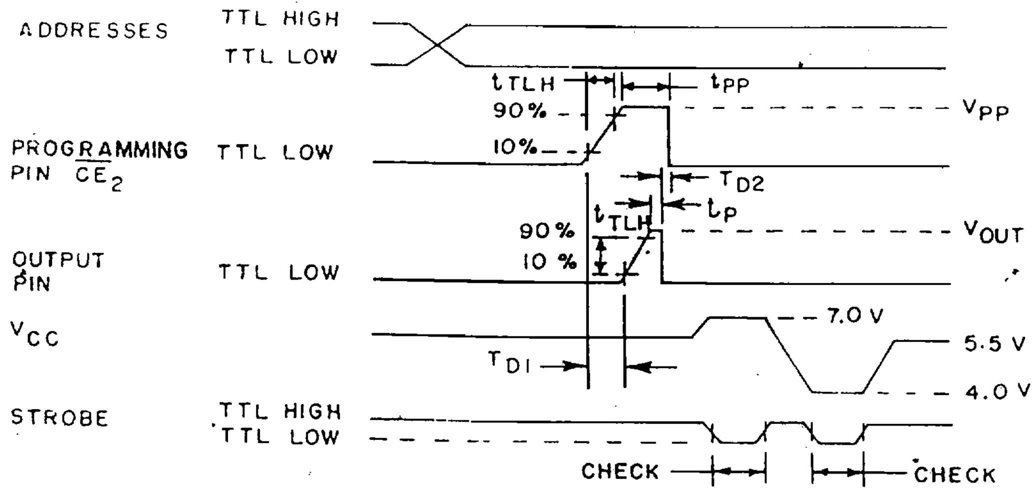
1. Test table for devices programmed in accordance with an altered item drawing may be replaced by the equivalent tests which apply to the specific program configuration for the resulting read-only memory.
2. C_L = 30 pF minimum, including jig and probe capacitance; R_1 = 330Ω ±25% and R_2 = 680Ω ±20%.
3. Outputs may be under load simultaneously.

FIGURE 7. Switching time test circuit - Continued.



NOTES:
1. (*) Disregard for devices with no chip enable inputs.
2. All other waveform characteristics shall be as specified in table IVA.

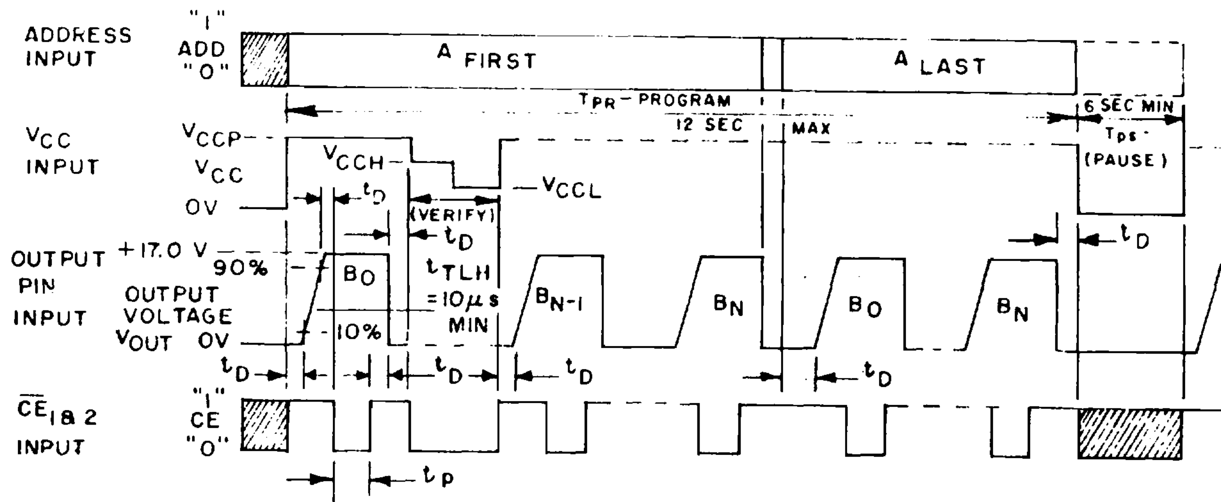
FIGURE 8a. Programming voltage waveforms during programming for circuit A.



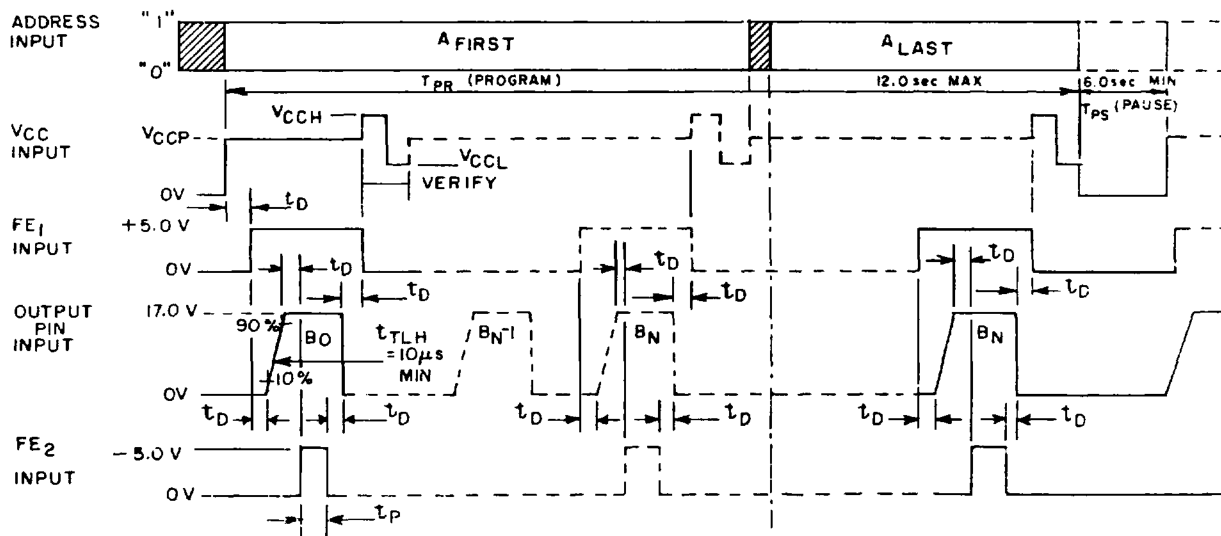
NOTES:
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in IVB.
3. $\overline{CE}_1$ is the programming pin for device types 04 and 05.

FIGURE 8b. Programming voltage waveforms during programming for circuit B.

Device types 01 and 02

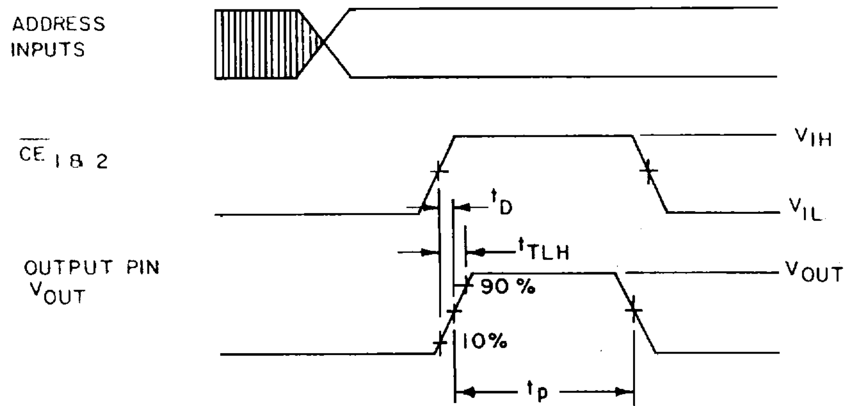


Device type 03



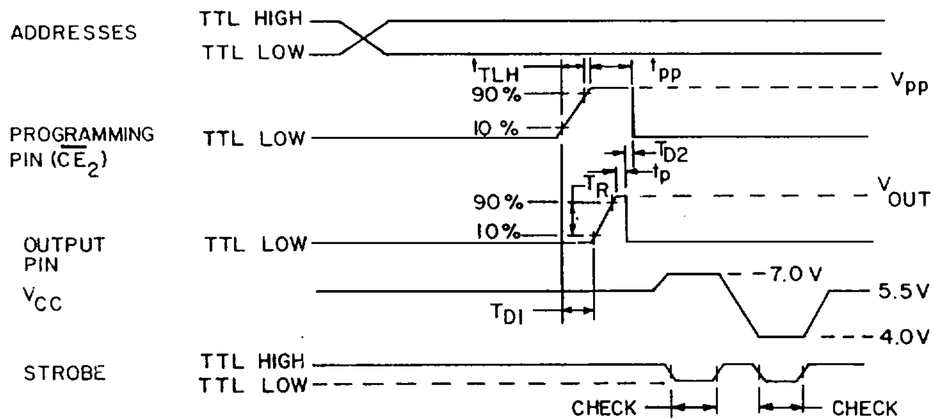
NOTE: All other waveform characteristics shall be as specified in tabel IVC.

FIGURE 8c. Programming voltage waveforms during programming for circuit C.



NOTE: All other waveform characteristics shall be as specified in table IVD.

FIGURE 8d. Programming voltage waveforms during programming for circuit D.



NOTES:
1. Output load is 0.2 mA and 12 mA during 7.0 V and 4.0 V check, respectively.
2. All other waveform characteristics shall be as specified in table IVF.

FIGURE 8e. Programming voltage waveforms during programming for circuit F.

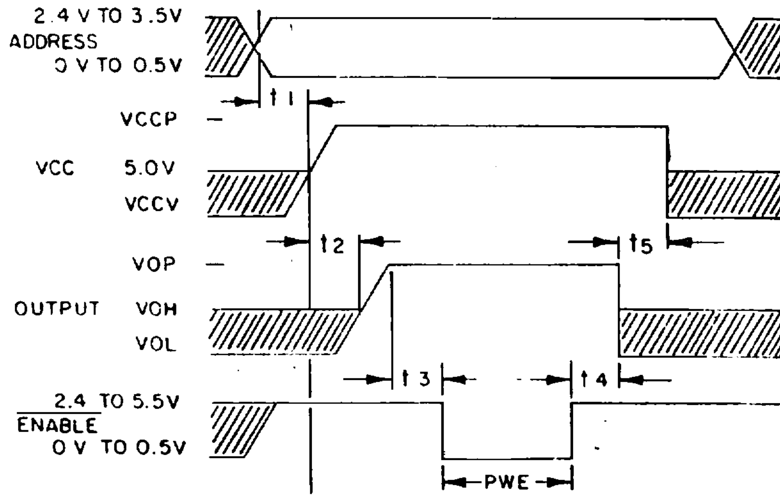
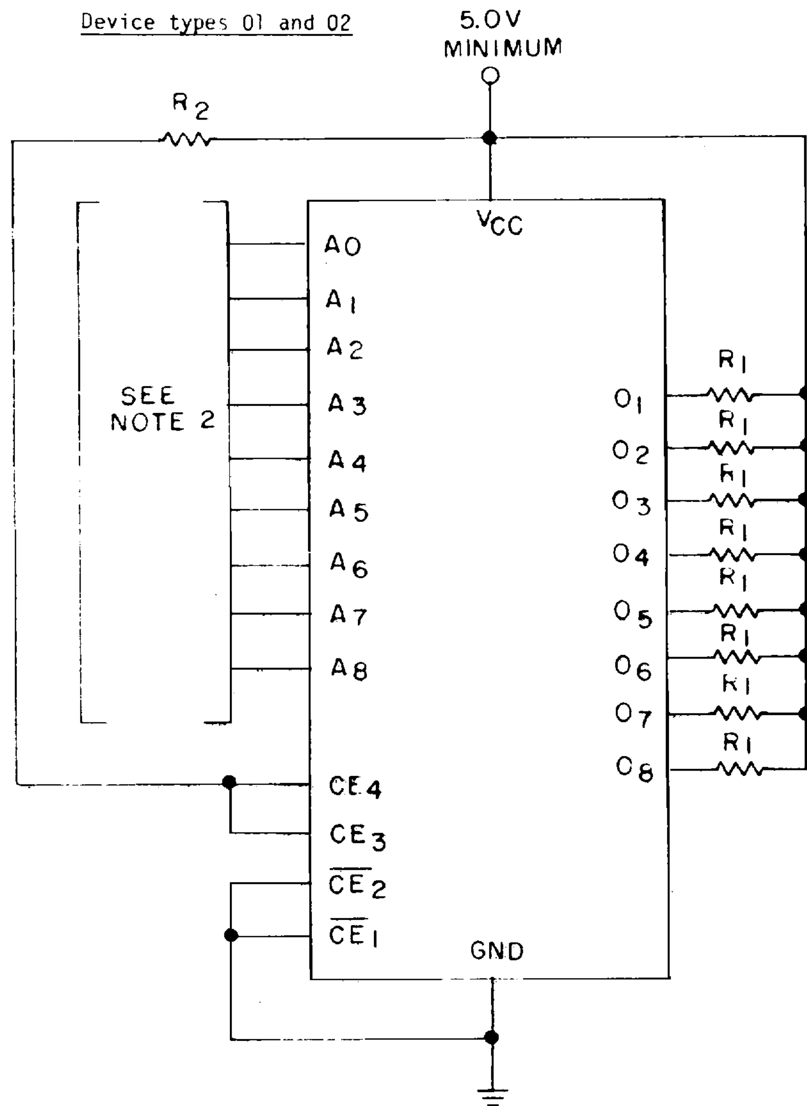


FIGURE 8g. Programming voltage waveforms during programming for circuit G.

Device types 01 and 02

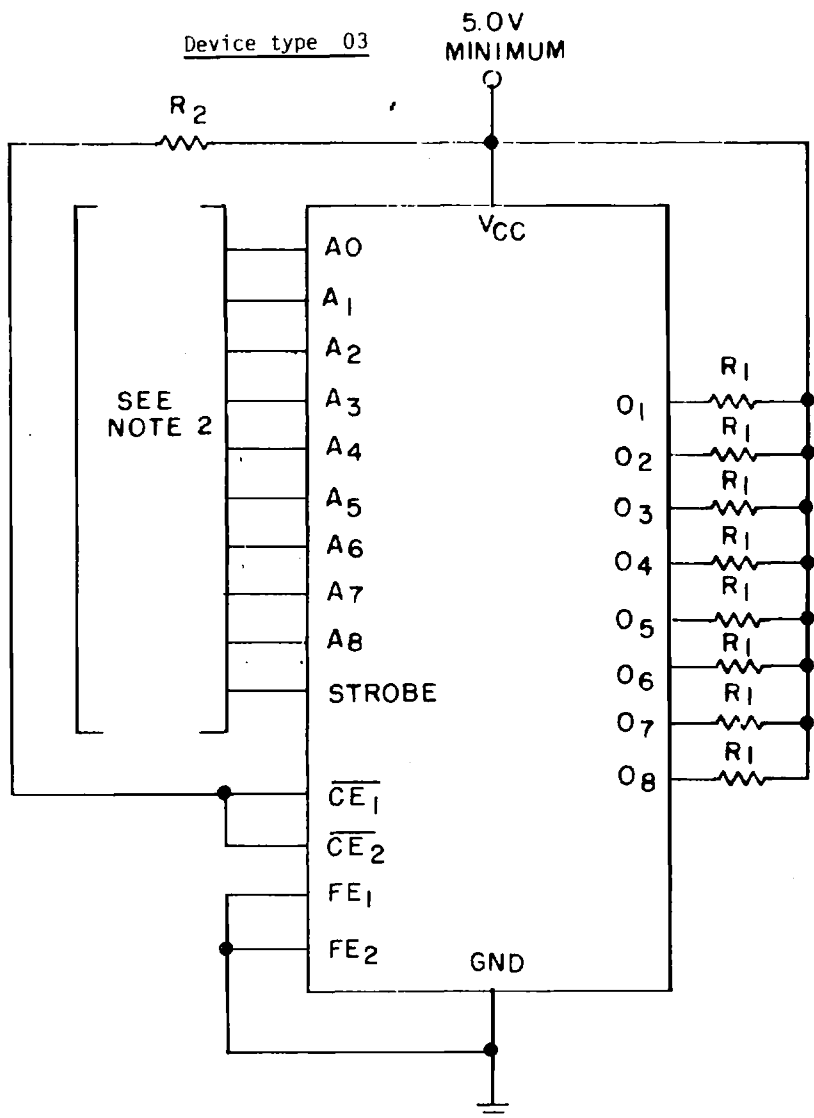


NOTES:

1. R_1 = 4.7 kΩ ±5%. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. R_2 = 1 kΩ ±5%.
4. Burn-in circuit may be used to perform this test. (see 4.2d).

FIGURE 9. Freeze-out test bias configuration.

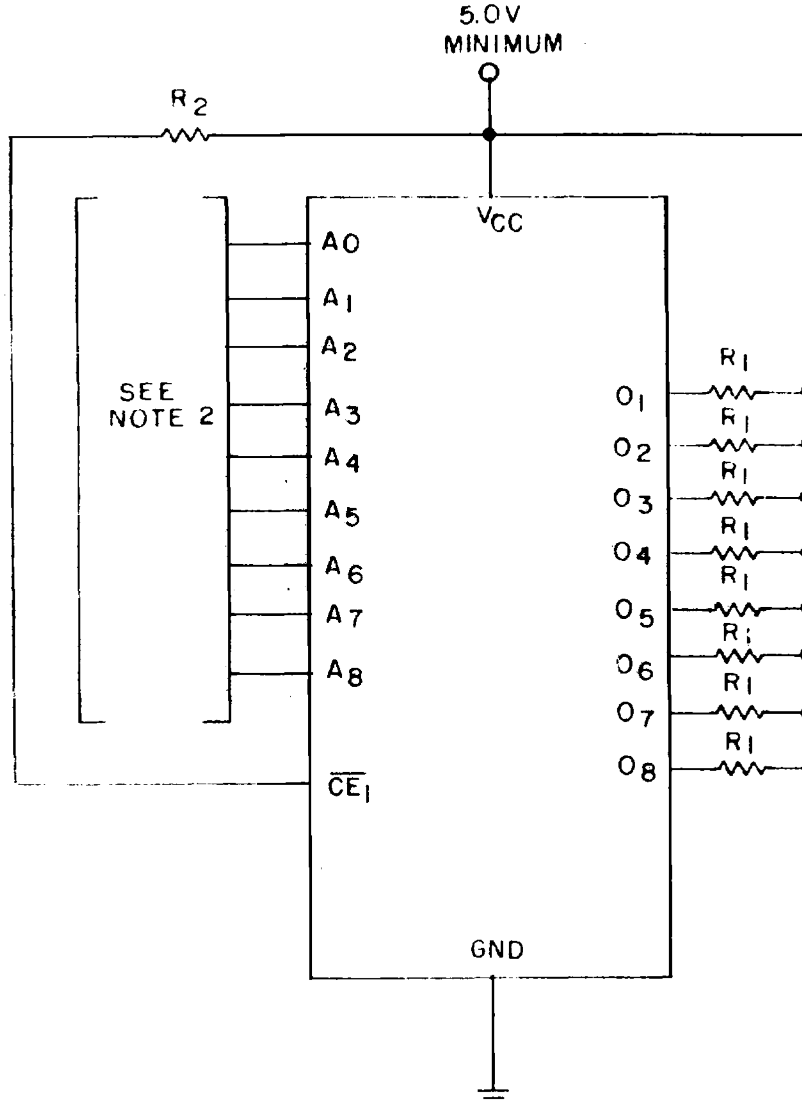
Device type 03



NOTES:
1. R_1 = 4.7 kΩ ±5%. All bit outputs shall have spearate identical loads.
2. All Address inputs shall be either high, low, or open.
3. R_2 = 1 kΩ ±5%.
4. Burn-in circuit may be used to perform this test. (See 4.2d.)

FIGURE 9. Freeze-out test bias configuration - Continued.

Device types 04 and 05



NOTES:
1. R_1 = 4.7 kΩ ±5%. All bit outputs shall have separate identical loads.
2. All Address inputs shall be either high, low, or open.
3. R_2 = 1 kΩ ±5%.
4. Burn-in circuit may be used to perform this test. (See 4.2d.)

FIGURE 9. Freeze-out test bias configuration - Continued.

TABLE III. Group A inspection for device type 01.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	GND	O_4	O_5	O_6	O_7	O_8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	V_{IC}		1	-10 mA											GND												4.5 V	A_7		-1.5	V
			2		-10 mA										"												"	A_6		"	"
			3			-10 mA									"												"	A_5		"	"
			4				-10 mA								"												"	A_4		"	"
			5					-10 mA							"												"	A_3		"	"
			6						-10 mA						"												"	A_2		"	"
			7							-10 mA					"												"	A_1		"	"
			8								-10 mA				"												"	A_0		"	"
			9												"						-10 mA						"	CE_4		"	"
			10												"							-10 mA					"	CE_3		"	"
			11												"								-10 mA				"	$\overline{CE}_2$		"	"
			12												"									-10 mA			"	$\overline{CE}_1$		"	"
			13												"											-10 mA	"	A_8		"	"
	V_{OL}	3007	14	1/2/	1/3/	1/	1/	1/	1/	1/	1/2/	8 mA			"						2.4 V	2.4 V	0.5 V	0.5 V		1/2/4/	"	O_1		0.5	"
		"	15	"	"	"	"	"	"	"	"		8 mA		"						"	"	"	"		"	"	O_2		"	"
		"	16	"	"	"	"	"	"	"	"			8 mA	"						"	"	"	"		"	"	O_3		"	"
		"	17	"	"	"	"	"	"	"	"				"	8 mA					"	"	"	"		"	"	O_4		"	"
		"	18	"	"	"	"	"	"	"	"				"		8 mA				"	"	"	"		"	"	O_5		"	"
		"	19	"	"	"	"	"	"	"	"				"			8 mA			"	"	"	"		"	"	O_6		"	"
		"	20	"	"	"	"	"	"	"	"				"				8 mA		"	"	"	"		"	"	O_7		"	"
		"	21	13/14/	13/14/	13/14/	13/14/	13/14/	13/14/	13/14/	13/14/				"					8 mA	"	"	"	"		13/14/	"	O_8		"	"
	I_{IL1}	3009	22	0.5 V											"												5.5 V	A_7	-1.0	-250	μA
		"	23		0.5 V										"												"	A_6	"	"	"
		"	24			0.5 V									"												"	A_5	"	"	"
		"	25				0.5 V								"												"	A_4	"	"	"
		"	26					0.5 V							"												"	A_3	"	"	"
		"	27						0.5 V						"												"	A_2	"	"	"
		"	28							0.5 V					"												"	A_1	"	"	"
		"	29								0.5 V				"												"	A_0	"	"	"
		"	30												"								0.5 V				"	$\overline{CE}_2$	"	"	"
		"	31												"									0.5 V			"	$\overline{CE}_1$	"	"	"
		"	32												"											0.5 V	"	A_8	"	"	"
	I_{IL2}	"	33												"						0.5 V						"	CE_4	"	-1000	"
		"	34												"							0.5 V					"	CE_3	"	-1000	"
	I_{IH1}	3010	35	5.5 V											"												"	A_7		50	"
		"	36		5.5 V										"												"	A_6		"	"
		"	37			5.5 V									"												"	A_5		"	"
		"	38				5.5 V								"												"	A_4		"	"
		"	39					5.5 V							"												"	A_3		"	"
		"	40						5.5 V						"												"	A_2		"	"
		"	41							5.5 V					"												"	A_1		"	"
		"	42								5.5 V				"												"	A_0		"	"
		"	43												"						5.5 V						"	CE_4		"	"
		"	44												"							5.5 V					"	CE_3		"	"
		"	45												"									5.5 V			"	$\overline{CE}_1$		"	"
		"	46												"											5.5 V	"	A_8		"	"
	I_{IH2}	"	47												"								4.5 V				"	$\overline{CE}_2$		100	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K, X,Z	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
			Test no.	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	GND	O_4	O_5	O_6	O_7	O_8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	I_{CEX}		48	15/	15/	15/	15/	15/	15/	15/	15/	5.2 V			GND											15/	5.5 V	O_1		100	µA
			49	1/	1/	1/	1/	1/	1/	1/	1/		5.2 V		"											1/	"	O_2		"	"
			50	"	"	"	"	"	"	"	"			5.2 V	"											"	"	O_3		"	"
			51	"	"	"	"	"	"	"	"				"	5.2 V										"	"	O_4		"	"
			52	"	"	"	"	"	"	"	"				"		5.2 V									"	"	O_5		"	"
			53	"	"	"	"	"	"	"	"				"			5.2 V								"	"	O_6		"	"
			54	"	"	"	"	"	"	"	"				"				5.2 V							"	"	O_7		"	"
			55	"	"	"	"	"	"	"	"									5.2 V						"		O_8		"	"
	I_{CC}	3005	56	GND	GND	GND	GND	GND	GND	GND	GND				"						5/	5/	GND	GND		GND	"	V_{CC}		185	mA
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																														
7 T_C = 25°C	Functional test	3014	57	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/	6/	Outputs		6/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																														
9 T_C = 25°C	t_{PLH1}	GALPAT Fig. 7	58	7/	7/	7/	7/	7/	7/	7/	7/	9/	9/	9/	GND	9/	9/	9/	9/	9/	5.5 V	5.5 V	GND	GND		7/	7/	Outputs		90	ns
	t_{PHL1}	GALPAT Fig. 7	59	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	5.5 V	5.5 V	GND	GND		7/	7/	"		90	"
	t_{PLH2}	Sequential Fig. 7	60	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	8/	"		50	"
	t_{PHL2}	Sequential Fig. 7	61	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	8/	"		50	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																														

See footnotes at end of table.

TABLE III. Group A inspection for device type 02.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X,Z Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
				A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_2	O_3	GND	O_4	O_5	O_6	O_7	O_8	CE_4	CE_3	$\overline{CE}_2$	$\overline{CE}_1$	NC	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	V_{IC}		1	-10 mA											GND												4.5 V	A_7		-1.5	V
			2		-10 mA										"												"	A_6		"	"
			3			-10 mA									"												"	A_5		"	"
			4				-10 mA								"												"	A_4		"	"
			5					-10 mA							"												"	A_3		"	"
			6						-10 mA						"												"	A_2		"	"
			7							-10 mA					"												"	A_1		"	"
			8								-10 mA				"												"	A_0		"	"
			9												"						-10 mA						"	CE_4		"	"
			10												"							-10 mA					"	CE_3		"	"
			11												"								-10 mA				"	$\overline{CE}_2$		"	"
			12												"									-10 mA			"	$\overline{CE}_1$		"	"
			13												"											-10 mA	"	A_8		"	"
	V_{OL}	3007	14	1/2/	1/3/	1/	1/	1/	1/	1/	1/2/	8 mA			"						2.4 V	2.4 V	0.5 V	0.5 V		1/4/	"	O_1		0.5	"
		"	15	"	"	"	"	"	"	"	"		8 mA		"						"	"	"	"		"	"	O_2		"	"
		"	16	"	"	"	"	"	"	"	"			8 mA	"						"	"	"	"		"	"	O_3		"	"
		"	17	"	"	"	"	"	"	"	"				"	8 mA					"	"	"	"		"	"	O_4		"	"
		"	18	16/	16/	16/	16/	16/	16/	16/	16/				"		8 mA				"	"	"	"		16/	"	O_5		"	"
		"	19	"	"	"	"	"	"	"	"				"			8 mA			"	"	"	"		"	"	O_6		"	"
		"	20	"	"	"	"	"	"	"	"				"				8 mA		"	"	"	"		"	"	O_7		"	"
		"	21	13/	13/	13/	13/	13/	13/	13/	13/				"					8 mA	"	"	"	"		13/	"	O_8		"	"
	V_{OH}	3006	22	"	1/10/	1/	1/	1/	1/	1/	1/	-2 mA			"						"	"	"	"		1/10/	"	O_1	2.4		"
		"	23	"	"	"	"	"	"	"	"		-2 mA		"						"	"	"	"		"	"	O_2	"		"
		"	24	"	"	"	"	"	"	"	"			-2 mA	"						"	"	"	"		"	"	O_3	"		"
		"	25	"	"	"	"	"	"	"	"				"	-2 mA					"	"	"	"		"	"	O_4	"		"
		"	26	"	"	"	"	"	"	"	"				"		-2 mA				"	"	"	"		"	"	O_5	"		"
		"	27	"	"	"	"	"	"	"	"				"			-2 mA			"	"	"	"		"	"	O_6	"		"
		"	28	"	"	"	"	"	"	"	"				"				-2 mA		"	"	"	"		"	"	O_7	"		"
		"	29	17/	17/	17/	17/	17/	17/	17/	17/				"					-2 mA	"	"	"	"		17/	"	O_8	"		"
	I_{IL1}	3009	30	0.5 V											"												5.5 V	A_7	-1.0	-250	μA
		"	31		0.5 V										"												"	A_6	"	"	"
		"	32			0.5 V									"												"	A_5	"	"	"
		"	33				0.5 V								"												"	A_4	"	"	"
		"	34					0.5 V							"												"	A_3	"	"	"
		"	35						0.5 V						"												"	A_2	"	"	"
		"	36							0.5 V					"												"	A_1	"	"	"
		"	37								0.5 V				"												"	A_0	"	"	"
		"	38												"								0.5 V				"	$\overline{CE}_2$	"	"	"
		"	39												"									0.5 V			"	$\overline{CE}_1$	"	"	"
		"	40												"											0.5 V	"	A_8	"	"	"
	I_{IL2} 24/	"	41												"						0.5 V						"	CE_4	"	-1000	"
		"	42												"							0.5 V					"	CE_3	"	-1000	"
	I_{IH1}	3010	43	5.5 V											"												"	A_7		50	"
		"	44		5.5 V										"												"	A_6		"	"
		"	45			5.5 V									"												"	A_5		"	"
		"	46				5.5 V								"												"	A_4		"	"
		"	47					5.5 V							"												"	A_3		"	"
		"	48						5.5 V						"												"	A_2		"	"
		"	49							5.5 V					"												"	A_1		"	"
		"	50								5.5 V				"												"	A_0		"	"
		"	51												"						5.5 V						"	CE_4		"	"
		"	52												"							5.5 V					"	CE_3		"	"
		"	53												"									5.5 V			"	$\overline{CE}_1$		"	"
		"	54												"											5.5 V	"	A_8		"	"
	I_{IH2} 23/	"	55												"								4.5 V				"	$\overline{CE}_2$		100	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 02 - Continued.

Terminal conditions: Outputs not designated are open for resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X,Z Test no.	1 A_7	2 A_6	3 A_5	4 A_4	5 A_3	6 A_2	7 A_1	8 A_0	9 O_1	10 O_2	11 O_3	12 GND	13 O_4	14 O_5	15 O_6	16 O_7	17 O_8	18 CE_4	19 CE_3	20 $\overline{CE}_2$	21 $\overline{CE}_1$	22 NC	23 A_8	24 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = 25°C	I_{OHZ}		56									5.2 V			GND						GND	GND	5.5 V	5.5 V			5.5 V	O_1		100	µA
			57										5.2 V		"						"	"	"	"			"	O_2		"	"
			58											5.2 V	"						"	"	"	"			"	O_3		"	"
			59												"	5.2 V					"	"	"	"			"	O_4		"	"
			60												"		5.2 V				"	"	"	"			"	O_5		"	"
			61												"			5.2 V			"	"	"	"			"	O_6		"	"
			62												"				5.2 V		"	"	"	"			"	O_7		"	"
			63												"					5.2 V	"	"	"	"			"	O_8		"	"
	I_{OLZ}		64									0.5 V			"						"	"	"	"			"	O_1		-100	"
			65										0.5 V		"						"	"	"	"			"	O_2		"	"
			66											0.5 V	"						"	"	"	"			"	O_3		"	"
			67												"	0.5 V					"	"	"	"			"	O_4		"	"
			68												"		0.5 V				"	"	"	"			"	O_5		"	"
			69												"			0.5 V			"	"	"	"			"	O_6		"	"
			70												"				0.5 V		"	"	"	"			"	O_7		"	"
			71												"					0.5 V	"	"	"	"			"	O_8		"	"
	I_{CC}	3005	72	GND	GND	GND	GND	GND	GND	GND	GND				"						5/	5/	GND	GND		GND	"	V_{CC}		185	mA
	I_{OS}	3011	73	1/	1/10/	1/	1/	1/	1/	1/	1/	GND			"						5.5 V	5.5 V	"	"		1/10/	"	O_1	-10	-100	"
		"	74	"	"	"	"	"	"	"	"		GND		"						"	"	"	"		"	"	O_2	"	"	"
		"	75	"	"	"	"	"	"	"	"			GND	"						"	"	"	"		"	"	O_3	"	"	"
		"	76	"	"	"	"	"	"	"	"				"	GND					"	"	"	"		"	"	O_4	"	"	"
		"	77	"	"	"	"	"	"	"	"				"		GND				"	"	"	"		"	"	O_5	"	"	"
		"	78	"	"	"	"	"	"	"	"				"			GND			"	"	"	"		"	"	O_6	"	"	"
		"	79	"	"	"	"	"	"	"	"				"				GND		"	"	"	"		"	"	O_7	"	"	"
		"	80	18/	18/	18/	18/	18/	18/	18/	18/				"					GND	"	"	"	"		18/	"	O_8	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																														
7 T_C = 25°C	Functional test	3014	81	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/	6/	Outputs		6/	ns
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																														
9 T_C = 25°C	t_{PLH1}	GALPAT Fig. 7	82	7/	7/	7/	7/	7/	7/	7/	7/	9/	9/	9/	GND	9/	9/	9/	9/	9/	5.5 V	5.5 V	GND	GND		7/	7/	Outputs		90	ns
	t_{PHL1}	GALPAT Fig. 7	83	7/	7/	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	5.5 V	5.5 V	GND	GND		7/	7/	"		90	"
	t_{PLH2}	Sequential Fig. 7	84	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	8/	"		50	"
	t_{PHL2}	Sequential Fig. 7	85	8/	8/	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/		8/	8/	"		50	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																														

See footnotes at end of table.

TABLE III. Group A inspection for device type 03.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	Measured terminal	Test limits		Unit
			Test no.	A_3	A_4	A_5	A_6	A_7	A_8	O_1	O_2	O_3	O_4	FE_2	GND	FE_1	O_5	O_6	O_7	O_8	Strobe	$\overline{CE}_2$	$\overline{CE}_1$	A_0	A_1	A_2	V_{CC}		Min	Max	
T_C = 25°C [1]	V_{IC}		1	-10 mA											GND												4.5 V	A_3		-1.5	V
			2		-10 mA										"												"	A_4		"	"
			3			-10 mA									"												"	A_5		"	"
			4				-10 mA								"												"	A_6		"	"
			5					-10 mA							"												"	A_7		"	"
			6						-10 mA						"												"	A_8		"	"
			7											-10 mA	"												"	FE_2		"	"
			8												"	-10 mA											"	FE_1		"	"
			9												"						-10 mA						"	Strobe		"	"
			10												"							-10 mA					"	$\overline{CE}_2$		"	"
			11												"								-10 mA				"	$\overline{CE}_1$		"	"
			12												"									-10 mA			"	A_0		"	"
			13												"										-10 mA		"	A_1		"	"
			14																							-10 mA		A_2			
	V_{OL}	3007	15	1/	1/	1/	1/	1/	1/	8 mA				GND	"	GND					2.4 V	2.4 V	0.5 V	1/	1/	1/	"	O_1		0.5	"
		"	16	"	"	"	"	"	"		8 mA			"	"	"					"	"	"	"	"	"	"	O_2		"	"
		"	17	"	"	"	"	"	"			8 mA		"	"	"					"	"	"	"	"	"	"	O_3		"	"
		"	18	"	"	"	"	"	"				8 mA	"	"	"					"	"	"	"	"	"	"	O_4		"	"
		"	19	"	"	"	"	"	"					"	"	"	8 mA				"	"	"	"	"	"	"	O_5		"	"
		"	20	"	"	"	"	"	"					"	"	"		8 mA			"	"	"	"	"	"	"	O_6		"	"
		"	21	"	"	"	"	"	"					"	"	"			8 mA		"	"	"	"	"	"	"	O_7		"	"
		"	22	"	"	"	"	"	"					"	"	"				8 mA	"	"	"	"	"	"	"	O_8			"
	V_{OH}	3006	23	"	"	"	"	"	1/10/	-2 mA				"	"	"					"	"	"	"		"	"	O_1	2.4		"
		"	24	"	"	"	"	"	"		-2 mA			"	"	"					"	"	"	"		"	"	O_2	"		"
		"	25	"	"	"	"	"	"			-2 mA		"	"	"					"	"	"	"		"	"	O_3	"		"
		"	26	"	"	"	"	"	"				-2 mA	"	"	"					"	"	"	"		"	"	O_4	"		"
		"	27	"	"	"	"	"	"					"	"	"	-2 mA				"	"	"	"		"	"	O_5	"		"
		"	28	"	"	"	"	"	"					"	"	"		-2 mA			"	"	"	"		"	"	O_6	"		"
		"	29	"	"	"	"	"	"					"	"	"			-2 mA		"	"	"	"		"	"	O_7	"		"
		"	30	"	"	"	"	"	"					"	"	"				-2 mA	"	"	"	"		"	"	O_8	"		"
	I_{IL1}	3009	31	0.5 V											"												5.5 V	A_3	-1.0	-100	µA
		"	32		0.5 V										"												"	A_4	"	"	"
		"	33			0.5 V									"												"	A_5	"	"	"
		"	34				0.5 V								"												"	A_6	"	"	"
		"	35					0.5 V							"												"	A_7	"	"	"
		"	36						0.5 V						"												"	A_8	"	"	"
		"	37											0.5 V	"												"	FE_2		1.0	mA
		"	38												"	0.5 V											"	FE_1		1.0	mA
		"	39												"						0.5 V						"	Strobe	-1.0	-100	µA
		"	40												"							0.5 V					"	$\overline{CE}_2$	"	"	"
		"	41												"								0.5 V				"	$\overline{CE}_1$	"	"	"
		"	42												"									0.5 V			"	A_0	"	"	"
		"	43												"										0.5 V		"	A_1	"	"	"
			44												"											0.5 V	"	A_2	"	"	"
	I_{IH1}	3010	45	5.5 V											"												"	A_3		50	"
		"	46		5.5 V										"												"	A_4		"	"
		"	47			5.5 V									"												"	A_5		"	"
		"	48				5.5 V								"												"	A_6		"	"
		"	49					5.5 V							"												"	A_7		"	"
		"	50						5.5 V						"												"	A_8		"	"
		"	51												"						5.5 V						"	Strobe		"	"
		"	52												"							5.5 V					"	$\overline{CE}_2$		"	"
		"	53												"								5.5 V				"	$\overline{CE}_1$		"	"
		"	54												"									5.5 V			"	A_0		"	"
		"	55												"										5.5 V		"	A_1		"	"
			56																							5.5 V		A_2			

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 - Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated are high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Cases J,K,X Test no.	1 A_3	2 A_4	3 A_5	4 A_6	5 A_7	6 A_8	7 O_1	8 O_2	9 O_3	10 O_4	11 FE_2	12 GND	13 FE_1	14 O_5	15 O_6	16 O_7	17 O_8	18 Strobe	19 $\overline{CE}_2$	20 $\overline{CE}_1$	21 A_0	22 A_1	23 A_2	24 V_{CC}	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = 25°C	I_{OHZ}		57							5.2 V					GND						0.5 V	2.4 V	0.5 V				5.5 V	O_1		100	µA
			58								5.2 V				"						"	"	"				"	O_2		"	"
			59									5.2 V			"						"	"	"				"	O_3		"	"
			60										5.2 V		"						"	"	"				"	O_4		"	"
			61												"		5.2 V				"	"	"				"	O_5		"	"
			62												"			5.2 V			"	"	"				"	O_6		"	"
			63												"				5.2 V		"	"	"				"	O_7		"	"
			64												"					5.2 V	"	"	"				"	O_8		"	"
	I_{OLZ}		65							0.5 V					"						"	"	"				"	O_1		-100	"
			66								0.5 V				"						"	"	"				"	O_2		"	"
			67									0.5 V			"						"	"	"				"	O_3		"	"
			68										0.5 V		"						"	"	"				"	O_4		"	"
			69												"		0.5 V				"	"	"				"	O_5		"	"
			70												"			0.5 V			"	"	"				"	O_6		"	"
			71												"				0.5 V		"	"	"				"	O_7		"	"
			72												"					0.5 V	"	"	"				"	O_8		"	"
	I_{CC}	3005	73	GND	GND	GND	GND	GND	GND					GND	"	GND					GND	GND	GND				"	V_{CC}		185	mA
	I_{OS}	3011	74	1/	1/	1/	1/	1/	1/10/	GND					"						"	5.5 V	"	1/	1/10/	1/	"	O_1	-10	-100	"
		"	75	"	"	"	"	"	"		GND				"						"	"	"	"	"	"	"	O_2	"	"	"
		"	76	"	"	"	"	"	"			GND			"						"	"	"	"	"	"	"	O_3	"	"	"
		"	77	"	"	"	"	"	"				GND		"						"	"	"	"	"	"	"	O_4	"	"	"
		"	78	"	"	"	"	"	"						"		GND				"	"	"	"	"	"	"	O_5	"	"	"
		"	79	"	"	"	"	"	"						"			GND			"	"	"	"	"	"	"	O_6	"	"	"
		"	80	"	"	"	"	"	"						"				GND		"	"	"	"	"	"	"	O_7	"	"	"
		"	81	"	"	"	"	"	"						"					GND	"	"	"	"	"	"	"	O_8	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																														
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																														
7 T_C = 25°C	Functional test	3014	82	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/		6/	6/	Outputs		6/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																														
9 T_C = 25°C	t_{PLH1}	GALPAT Fig. 7	83	7/	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	GND	GND	9/	9/	9/	9/	GND	5.5 V	GND	7/	7/	7/	7/	Outputs		90	ns
	t_{PHL1}	GALPAT Fig. 7	84	7/	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	7/	7/	7/	7/	"		90	"
	t_{PLH2}	Sequential Fig. 7	85	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	"		50	"
	t_{PHL2}	Sequential Fig. 7	86	8/	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	"		50	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																														
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																														

See footnotes at end of table.

TABLE III. Group A inspection for device type 04.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated may be high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	18	17	18	19	20	Measured terminal	Test limits		Unit
			Test no.	A_0	A_1	A_2	A_3	A_4	O_1	O_2	O_3	O_4	GND	O_5	O_6	O_7	O_8	$\overline{CE}_1$	A_5	A_6	A_7	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	V_{IC}		1	-10 mA									GND										4.5 V	A_0		-1.5	V
			2		-10 mA								"										"	A_1		"	"
			3			-10 mA							"										"	A_2		"	"
			4				-10 mA						"										"	A_3		"	"
			5					-10 mA					"										"	A_4		"	"
			6										"					-10 mA					"	$\overline{CE}_1$		"	"
			7										"						-10 mA				"	A_5		"	"
			8										"							-10 mA			"	A_6		"	"
			9										"								-10 mA		"	A_7		"	"
			10										"									-10 mA	"	A_8		"	"
	V_{OL}	3007	11	2.4 V	1/ 3/	1/	1/	1/	8 mA				"					0.5 V	1/	1/	1/	1/	"	O_1		0.5	"
		"	12	"	"	"	"	"		8 mA			"					"	"	"	"	"	"	O_2		"	"
		"	13	"	"	"	"	"			8 mA		"					"	"	"	"	"	"	O_3		"	"
		"	14	"	"	"	"	"				8 mA	"					"	"	"	"	"	"	O_4		"	"
		"	15	"	"	"	"	"					"	8 mA				"	"	"	"	"	"	O_5		"	"
		"	16	"	"	"	"	"					"		8 mA			"	"	"	"	"	"	O_6		"	"
		"	17	"	"	"	"	"					"			8 mA		"	"	"	"	"	"	O_7		"	"
		"	18	19/	19/	19/	19/	19/					"				8 mA	19/	19/	19/	19/	19/	19/	O_8		"	"
	I_{IL}	3009	19	0.5 V									"										5.5 V	A_0	-1.0	-250	µA
		"	20		0.5 V								"										"	A_1	"	"	"
		"	21			0.5 V							"										"	A_2	"	"	"
		"	22				0.5 V						"										"	A_3	"	"	"
		"	23					0.5 V					"										"	A_4	"	"	"
		"	24										"					0.5 V					"	$\overline{CE}_1$	"	"	"
		"	25										"						0.5 V				"	A_5	"	"	"
		"	26										"							0.5 V			"	A_6	"	"	"
		"	27										"								0.5 V		"	A_7	"	"	"
		"	28										"									0.5 V	"	A_8	"	"	"
	I_{IH1}	3010	29	5.5 V									"										"	A_0		50	"
		"	30		5.5 V								"										"	A_1		"	"
		"	31			5.5 V							"										"	A_2		"	"
		"	32				5.5 V						"										"	A_3		"	"
		"	33					5.5 V					"										"	A_4		"	"
		"	34										"						5.5 V				"	A_5		"	"
		"	35										"							5.5 V			"	A_6		"	"
		"	36										"								5.5 V		"	A_7		"	"
		"	37										"									5.5 V	"	A_8		"	"
	I_{IH2}	"	38										"					4.5 V					"	$\overline{CE}_1$		100	"
	I_{CEX}		39						5.2 V				"					5.5 V					"	O_1		"	"
			40							5.2 V			"					"					"	O_2		"	"
			41								5.2 V		"					"					"	O_3		"	"
			42									5.2 V	"					"					"	O_4		"	"
			43										"	5.2 V				"					"	O_5		"	"
			44										"		5.2 V			"					"	O_6		"	"
			45										"			5.2 V		"					"	O_7		"	"
			46										"				5.2 V	"					"	O_8		"	"
	I_{CC}	3005	47	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	"	V_{CC}		155	mA

See footnotes at end of table.

TABLE III. Group A inspection for device type 04 - Continued.
Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated may be high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Test no.	A_0	A_1	A_2	A_3	A_4	O_1	O_2	O_3	O_4	GND	O_5	O_6	O_7	O_8	$\overline{CE}_1$	A_5	A_6	A_7	A_8	V_{CC}		Min	Max	
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																										
7 T_C = 25°C	Functional test	3014	48	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	Outputs		6/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																										
9 T_C = 25°C	t_{PLH1}	GALPAT Fig. 7	49	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	9/	9/	9/	9/	GND	7/	7/	7/	7/	7/	Outputs		80	ns
	t_{PHL1}	GALPAT Fig. 7	50	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	GND	7/	7/	7/	7/	7/	"		80	"
	t_{PLH2}	Sequential Fig. 7	51	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		50	"
	t_{PHL2}	Sequential Fig. 7	52	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		50	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																										

See footnotes at end of table.

TABLE III. Group A inspection for device type 0?.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated may be high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Test no.	A_0	A_1	A_2	A_3	A_4	O_1	O_2	O_3	O_4	GND	O_5	O_6	O_7	O_8	$\overline{CE}_1$	A_5	A_6	A_7	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	V_{IC}		1	-10 mA									GND										4.5 V	A_0		-1.5	V
			2		-10 mA								"										"	A_1		"	"
			3			-10 mA							"										"	A_2		"	"
			4				-10 mA						"										"	A_3		"	"
			5					-10 mA					"										"	A_4		"	"
			6										"					-10 mA					"	$\overline{CE}_1$		"	"
			7										"						-10 mA				"	A_5		"	"
			8										"							-10 mA			"	A_6		"	"
			9										"								-10 mA		"	A_7		"	"
			10										"									-10 mA	"	A_8		"	"
	V_{OL}	3007	11	2.4 V	1/3/	1/11/	1/11/	1/	12/				"					0.5 V	1/	1/	1/	1/	"	O_1		0.5	"
		"	12	"	"	"	"	"		12/			"					"	"	"	"	"	"	O_2		"	"
		"	13	"	"	"	"	"			12/		"					"	"	"	"	"	"	O_3		"	"
		"	14	"	"	"	"	"				12/	"					"	"	"	"	"	"	O_4		"	"
		"	15	"	"	"	"	"					"	12/				"	"	"	"	"	"	O_5		"	"
		"	16	"	"	"	"	"					"		12/			"	"	"	"	"	"	O_6		"	"
		"	17	"	"	"	"	"					"			12/		"	"	"	"	"	"	O_7		"	"
		"	18	20/	20/	20/	20/	20/					"				12/	"	20/	20/	20/	20/	"	O_8		"	"
	V_{OH}	3006	19	1/	1/	1/	1/	1/	-2 mA				"					"	1/	1/	1/	1/	"	O_1	2.4		"
		"	20	"	"	"	"	"		-2 mA			"					"	"	"	"	"	"	O_2	"		"
		"	21	"	"	"	"	"			-2 mA		"					"	"	"	"	"	"	O_3	"		"
		"	22	"	"	"	"	"				-2 mA	"					"	"	"	"	"	"	O_4	"		"
		"	23	"	"	"	"	"					"	-2 mA				"	"	"	"	"	"	O_5	"		"
		"	24	"	"	"	"	"					"		-2 mA			"	"	"	"	"	"	O_6	"		"
		"	25	"	"	"	"	"					"			-2 mA		"	"	"	"	"	"	O_7	"		"
		"	26	21/	21/	21/	21/	21/					"				-2 mA	"	21/	21/	21/	21/	"	O_8	"		"
	I_{IL}	3009	27	0.5 V									"										5.5 V	A_0	-1.0	-250	μA
		"	28		0.5 V								"										"	A_1	"	"	"
		"	29			0.5 V							"										"	A_2	"	"	"
		"	30				0.5 V						"										"	A_3	"	"	"
		"	31					0.5 V					"										"	A_4	"	"	"
		"	32										"					0.5 V					"	$\overline{CE}_1$	"	"	"
		"	33										"						0.5 V				"	A_5	"	"	"
		"	34										"							0.5 V			"	A_6	"	"	"
		"	35										"								0.5 V		"	A_7	"	"	"
		"	36										"									0.5 V	"	A_8	"	"	"
	I_{IH1}	3010	37	5.5 V									"										"	A_0		50	"
		"	38		5.5 V								"										"	A_1		"	"
		"	39			5.5 V							"										"	A_2		"	"
		"	40				5.5 V						"										"	A_3		"	"
		"	41					5.5 V					"										"	A_4		"	"
		"	42										"						5.5 V				"	A_5		"	"
		"	43										"							5.5 V			"	A_6		"	"
		"	44										"								5.5 V		"	A_7		"	"
		"	45										"									5.5 V	"	A_8		"	"
	I_{IH2}	"	46										"					4.5 V					"	$\overline{CE}_1$		100	"

See footnotes at end of table.

TABLE III. Group A inspection for device type 05 - Continued.

Terminal conditions: Outputs not designated are open or resistive coupled to GND or voltage; inputs not designated may be high ≥2.0 V, low ≤0.8 V, or open.

Subgroup	Symbol	MIL-STD-883 method	Case Y	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measured terminal	Test limits		Unit
			Test no.	A_0	A_1	A_2	A_3	A_4	O_1	O_2	O_3	O_4	GND	O_5	O_6	O_7	O_8	$\overline{CE}_1$	A_5	A_6	A_7	A_8	V_{CC}		Min	Max	
1 T_C = 25°C	I_{OHZ}		47						5.2 V				GND					5.5 V					5.5 V	O_1		100	µA
			48							5.2 V			"					"					"	O_2		"	"
			49								5.2 V		"					"					"	O_3		"	"
			50									5.2 V	"					"					"	O_4		"	"
			51										"	5.2 V				"					"	O_5		"	"
			52										"		5.2 V			"					"	O_6		"	"
			53										"			5.2 V		"					"	O_7		"	"
			54										"				5.2 V	"					"	O_8		"	"
	I_{OLZ}		55						0.5 V				"					"					"	O_1		-100	"
			56							0.5 V			"					"					"	O_2		"	"
			57								0.5 V		"					"					"	O_3		"	"
			58									0.5 V	"					"					"	O_4		"	"
			59										"	0.5 V				"					"	O_5		"	"
			60										"		0.5 V			"					"	O_6		"	"
			61										"			0.5 V		"					"	O_7		"	"
			62										"				0.5 V	"					"	O_8		"	"
	I_{CC}	3005	63	GND	GND	GND	GND	GND					"					GND	GND	GND	GND	GND	"	V_{CC}	-10	-100	mA
	I_{OS}	3011	64	1/	1/	1/	1/	1/	GND				"					0.5 V	1/	1/	1/	1/	"	O_1	"	"	"
		"	65	"	"	"	"	"		GND			"					"	"	"	"	"	"	O_2	"	"	"
		"	66	"	"	"	"	"			GND		"					"	"	"	"	"	"	O_3	"	"	"
		"	67	"	"	"	"	"				GND	"					"	"	"	"	"	"	O_4	"	"	"
		"	68	"	"	"	"	"					"	GND				"	"	"	"	"	"	O_5	"	"	"
		"	69	"	"	"	"	"					"		GND			"	"	"	"	"	"	O_6	"	"	"
		"	70	"	"	"	"	"					"			GND		"	"	"	"	"	"	O_7	"	"	"
		"	71	22/	22/	22/	22/	22/					"				GND	"	22/	22/	22/	22/	"	O_8	"	"	"
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = 125°C and V_{IC} tests are omitted.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and V_{IC} tests are omitted.																										
7 T_C = 25°C	Functional test	3014	72	6/	6/	6/	6/	6/	6/	6/	6/	6/	GND	6/	6/	6/	6/	GND	6/	6/	6/	6/	6/	Outputs		6/	
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = 125°C and T_C = -55°C.																										
9 T_C = 25°C	t_{PLH1}	GALPAT Fig. 7	73	7/	7/	7/	7/	7/	9/	9/	9/	9/	GND	9/	9/	9/	9/	GND	7/	7/	7/	7/	7/	Outputs		80	ns
	t_{PHL1}	GALPAT Fig. 7	74	7/	7/	7/	7/	7/	"	"	"	"	"	"	"	"	"	GND	7/	7/	7/	7/	7/	"		80	"
	t_{PLH2}	Sequential Fig. 7	75	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		40	"
	t_{PHL2}	Sequential Fig. 7	76	8/	8/	8/	8/	8/	"	"	"	"	"	"	"	"	"	8/	8/	8/	8/	8/	8/	"		40	"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = 125°C.																										
11	Same tests, terminal conditions, and limits as for subgroup 9, except T_C = -55°C.																										

See footnotes at end of table.

1/ For unprogrammed devices, select an appropriate address to acquire the desired output state.

2/ For unprogrammed devices (circuit D), apply 12.0 V on pin 8 (A_0) and pin 1 (A_7).

3/ For unprogrammed device types 01 and 02 (circuit B), apply 12.0 V on pin 2 (A_6); for unprogrammed device types 04 and 05 (circuit B), apply 12.0 V on pin 2 (A_1).

4/ For unprogrammed devices (circuit A), apply 11.0 V on pin 23 (A_8).

5/ CE_4 and CE_3 may be "GND" or "2.4 V".

6/ The functional test shall verify that no fuses are blown for unprogrammed devices or that the altered item drawing pattern exists for programmed devices (see table II and 3.2.2.2). All bits shall be tested. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. Terminal conditions shall be as follows:

a. Inputs: H = 3.0 V, L = 0.0 V.

b. Outputs: OUtput voltage shall be either:

(1) H = 2.4 V minimum and L = 0.5 V maximum when using a high-speed checker double comparator, or

(2) H $\geq$ 1.0 V and L $<$ 1.0 V when using a high-speed checker single comparator.

7/ GALPAT (PROGRAMMED PROM). This program will test all bits in the array, the addressing and interaction between bits for ac performance, t_{PLH1} and t_{PHL1}. Each bit in the pattern is fixed by being programmed with an "H" or "L". The GALPAT tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:
Step 1. Word 0 is read.
Step 2. Word 1 is read.
Step 3. Word 0 is read.
Step 4. Word 2 is read.
Step 5. Word 0 is read.
Step 6. The reading procedure continues back and forth between word 0 and the next higher numbered word until word 511 is reached, then increments to the next word and reads back and forth as in Step 1 through Step 6 and shall include all words.
Step 7. Pass execution time = $(n^2 + n)$ x cycle time. n = 512.

8/ SEQUENTIAL (PROGRAMMED PROM). This program will test all bits in the array for t_{PHL2} and t_{PLH2}. The sequential tests shall be performed with V_{CC} = 4.5 V and 5.5 V.

Description:
Step 1. Each word in the pattern is tested from the enable lines to the output lines for recovery.
Step 2. Word 0 is addressed. Enable line is pulled high to low and low to high. t_{PHL2} and t_{PLH2} are read.
Step 3. Word 1 is addressed. Same enable sequence as above.
Step 4. The reading procedure continues until word 511 is reached.
Step 5. Pass execution time = 512 x cycle time.

9/ The outputs are loaded per figure 7.

10/ For unprogrammed device types 01 and 02 (circuit C), apply 10.0 V on pin 23 (A_8); 0.5 V on pin 2 (A_6); and 5.0 V on all other address pins. For unprogrammed device type 03 (circuit C), apply 10.0 V on pin 6 (A_8); 0.5 V on pin 22 (A_1); and 5.0 V on all other address pins.

11/ For unprogrammed devices (circuit F), apply 12.0 V on pin 3 (A_2) and 0.0 V on pin 4 (A_3).

12/ I_{OL} = 8 mA for circuit B devices; I_{OL} = 16 mA for circuit F devices.

13/ For unprogrammed device types 01, 02, 04, and 05 (circuit G) select an appropriate address to obtain the desired output state.

14/ For programmed device type 02 (circuit G) apply 4.5 V to pin 24; 10.5 V to pin 1; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3 and 2; and 0.0 V to pins 21, 20, 12, and 5.

15/ For unprogrammed device type 01 (circuit G) apply 10.5 V to pins 6 and 1; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, 3, and 2; 0.0 V to pins 21, 20, 12, and 5.

16/ For programmed device type 02 (circuit G) apply 10.5 V to pin 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 6, 4, 3, and 2; 0.0 V to pins 21, 20, 5, and 12.

17/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 6 and 1; 4.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, and 2; 2.0 V to pin 3; 0.0 V to pins 21, 20, 12, and 5.

18/ For unprogrammed device type 02 (circuit G) apply 10.5 V to pins 1 and 6; 5.5 V to pin 24; 3.0 V to pins 23, 19, 18, 8, 7, 4, 3 and 2; 0.0 V to pins 5, 12, 20, and 21.

19/ For programmed device type 04 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.

20/ For programmed device type 05 (circuit G) apply 10.5 V to pin 16; 4.5 V to pin 20; 3.0 V to pins 1, 2, 3, 4, 5, 18, and 19; 0.0 V to pins 10 and 15.

21/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 17 and 3; 4.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.

22/ For unprogrammed device type 05 (circuit G) apply 10.5 V to pins 3 and 17; 5.5 V to pin 20; 3.0 V to pins 2, 4, 5, 16, 18, and 19; 0.0 V to pins 1, 10, and 15.

23/ At the manufacturer's option, this may be prepared with V_{IH} = 5.5 and test limits of 50 μA maximum.

24/ At the manufacturer's option, this may be performed with V_{IO} = 0.5 V and test limits of -1 μA minimum to -250 μA maximum.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. Subgroup 2 shall be omitted for devices in package Z.

c. For moisture resistance and salt atmosphere of subgroups 3 and 5, omit initial conditioning for devices in package Z.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as specified herein.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

TABLE IVA. Programming characteristics for circuit A.

Characteristic	Symbol	Limits 1/			Unit
		Min	Recommended	Max	
Address input voltage 2/	V_{IH}	2.4	5.0	5.0	V
	V_{IL}	0.0	0.4	0.8	V
V_{CC} required during programming	V_{PH}	12.0	12.0	12.5	V
	V_{PL}	4.5	4.5	5.5	V
Programming input low current	I_{ILP}	---	-300	-600	µA
Programming voltage transition time	t_{TLH}	1	1	10	µs
	t_{THL}	1	1	10	µs
Programming delay	t_D	10	10	100	µs
Programming pulse width	t_P	90	100	110	µs
Programming duty cycle	D.C.	---	50	90	%
Output voltage Enable 3/	V_{OPE}	10.5	10.5	11.0	V
Disable 4/	V_{OPD}	4.5	5.0	5.5	V
Output voltage enable current	I_{OPE}	---	---	10	mA

1/ T_A = 25°C.

2/ Address and chip enable shall not be left open for V_{IH}.

3/ V_{OPE} supply shall be capable of sourcing 10 mA.

4/ Disable condition can be met with output open circuit.

4.6 Programming procedure identification. The programming procedure to be utilized shall be identified by the manufacturer's circuit designator. The circuit designtor is cross referenced in 6.6 herein with the manufacturer's symbol or FSCM number.

4.7 Programming procedures for circuit A. The waveforms on figure 8a, the programming characteristics of table IVA, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

c. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IL} to the CE_3 and CE_4 inputs. The CE inputs are TTL compatible.

d. Disable the programming circuitry by applying V_{OPD} to the outputs of the PROM.

e. Raise V_{CC} to V_{PH} as specified on the waveforms on figure 8a.

f. After a delay of t_D, apply only one V_{OPE} pulse with duration of t_P to the output selected for programming. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{PH} level by applying V_{OPE} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 8a.

h. Repeat 4.7b through 4.7g for all other bits to be programmed.

i. Lower V_{CC} to 4.5 volts following a delay of t_D from the last programming pulse applied to an output.

j. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IH} to the CE_3 and CE_4 inputs and verify the program.

k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.7b through 4.7i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.8 Programming procedures for circuit B. The waveforms on figure 8b, the programming characteristics of table IVB, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Raise V_{CC} to 5.5 volts.

c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ and V_{IL} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IH} to the CE input (device types 04 and 05). The CE input is TTL compatible.

e. Apply the V_{PP} pulse to the programming pin $\overline{CE}_2$ (device types 01 and 02) or $\overline{CE}$ (device types 04 and 05). In order to insure that the output transistor is off before increasing the voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the output pin's programming pulse by T_{D2} (see figure 8b).

f. Apply only one V_{OUT} pulse with duration of t_P to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

TABLE IVB. Programming characteristics for circuit B.

Characteristic	Symbol	Conditions	Limits 1/ Min	Recom-mended	Max	Unit
V_{CC} required during programming	V_{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t_{TLH}		0.34	0.40	0.46	V/µs
Programming voltage on programming pin	V_{PP}		32.5	33	33.5	V
Output programming voltage	V_{OUT}		25.5	26	26.5	V
Programming pin pulse width ($\overline{CE}_2$) 2/	t_{PP}	Chip disabled, V_{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t_p	Chip disabled, V_{CC} = 5.5 V	1		40	µs
Required current limit of power supply feeding programming pin and output during programming	I_L	V_{PP} = 33 V, V_{OUT} = 26 V, V_{CC} = 5.5 V	240			mA
Required time delay between disabling memory output and application of output programming pulse	T_{D1}	Measured at 10% levels	70	80	90	µs
Required time delay between removal of programming pulse and enabling memory output	T_{D2}	Measured at 10% levels	100			ns
Output current during verification	I_{OLV1}	Chip enabled, V_{CC} = 4.0 V	11	12	13	mA
	I_{OLV2}	Chip enabled, V_{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t_F/t_C			25	%

1/ T_A = 25°C.
2/ $\overline{CE}_1$ is the programming pin for device types 04 and 05.

g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

h. Repeat 4.8c through 4.8g for all other bits to be programmed.

i. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ and V_{IH} to the CE_3 and CE_4 inputs (device types 01 and 02) or V_{IL} to the $\overline{CE}$ inputs (device types 04 and 05) and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at V_{CC} = 4.0 V and 0.2 mA at V_{CC} = 7.0 V at T_A = 25°C.

j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.8c through 4.8i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.9 Programming procedures for circuit C. The waveforms on figure 8c, the programming characteristics of table IVC, and the following procedures shall apply:

4.9.1 Device types 01 and 02.

a. Connect the device in the electrical configuration for programming.

b. Terminate all device outputs with a 10-kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = V_{IH}, $\overline{CE}_2$ = V_{IL}, CE_3 = V_{IH}, and CE_4 = V_{IH}.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

d. After a t_D delay (10 µs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

e. After a t_D delay (10 µs), pulse CE_1 input to logic "0" for a duration of t_P.

f. After a t_D delay (10 µs), remove the V_{OUT} pulse from the programmed output. Programming a fuse will cause the output to go to a high-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay of t_D between pulses as shown on figure 8c.

h. Repeat 4.9.1c through 4.9.1g for all other bits to be programmed.

i. To verify programming after a t_D (10 µs) delay, lower V_{CC} to V_{CCH} and apply a logic "0" level to both $\overline{CE}_1$ and $\overline{CE}_2$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} and verify that the programmed output remains in the "1" state.

j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.9.1c through 4.9.1i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.9.2 Device type 03.

a. Connect the device in the electrical configuration for programming.

b. Terminate all device outputs with a 10-kΩ resistor to V_{CC}. Apply $\overline{CE}_1$ = V_{IL}, $\overline{CE}_2$ = V_{IH}, and strobe = V_{IH}.

c. Address the PROM with the binary address of the selected word to be programmed. Raise V_{CC} to V_{CCP}.

TABLE IVC. Programming characteristics for circuit C.

Characteristic	Symbol	Conditions	Limits Min	Limits Recom-mended	Limits Max	Unit
Programming voltage to V_{CC}	V_{CCP} 1/	I_{CCP} = 375 ±75 mA, transient or steady state	8.5	8.75	9.0	V
Verification upper limit	V_{CCH}		5.3	5.5	5.7	V
Verification lower limit	V_{CCL}		4.3	4.5	4.7	V
Verify threshold	V_S 2/		1.4	1.5	1.6	V
Programming supply current	I_{CCP}	V_{CCP} = 8.75 ±.25 V	300		450	mA
Input voltage, high level "1"	V_{IH}		2.4		5.5	V
Input voltage, low level "0"	V_{IL}		0	0.4	0.8	V
Input current	I_{IH}	V_{IH} = 5.5 V			50	µA
Input current	I_{IL}	V_{IL} = 0.4 V			-500	µA
Output programming voltage	V_{OUT} 3/	I_{OUT} = 200 ±20 mA, transient or steady state	16	17	18	V
Output programming current	I_{OUT}	V_{OUT} = 17 ±1 V	180	200	220	mA
Programming voltage transition time	t_{TLH}		10		50	µs
$\overline{CE}$ programming pulse width	t_P		300	400	500	µs
Pulse sequence delay	t_D		10			µs

1/ Bypass V_{CC} to GND with a 0.01 µF capacitor to reduce voltage spikes.

2/ V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.

3/ Care should be taken to insure the 17 ±1 output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.

d. After a t_D delay (10 μs), apply to FE_1 (pin 13) a voltage source of +5.0 ±0.5 V, with 10 mA sourcing current capability.

e. After a t_D delay (10 μs), apply only one V_{OUT} pulse to the output to be programmed. Program one output at a time.

f. After a t_D delay (10 μs), raise FE_2 (pin 11) from GND to +5.0 ±0.5 V for 1 ms, and return to GND.

g. After a t_D delay (10 μs), remove the V_{OUT} pulse from the programmed output.

h. Programming a fuse will cause the output to go to a high level logic in the verify mode. Other bits in the same word may be programmed sequentially while the V_{CC} input is at the V_{CCP} level by applying V_{OUT} pulses to each output to be programmed allowing a delay to t_D between pulses as shown on figure 8c.

i. Repeat 4.9.2c through 4.9.2h for all other bits to be programmed.

j. To verify programming after a t_D (10 μs) delay, return FE_1 to GND. Raise V_{CC} to V_{CCH}. The programmed output should remain in the high state. Again lower V_{CC} to V_{CCL} and verify that the programmed output remains in the high state.

k. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.9.2c through 4.9.2i one time only. Bits which fail to program the second time shall be considered programming rejects.

4.10 Programming procedures for circuit D. The waveforms on figure 8d, the programming characteristics of table IVD, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

c. Disable the chip by applying V_{IH} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IL} to the CE_3 and CE_4 inputs. The chip enable input is TTL compatible.

d. After a delay of t_D, apply only one V_{OUT} pulse with a duration of t_P to the output selected for programming. The other outputs may be left open or tied to V_{IH}. The outputs shall be programmed one output at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

e. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

f. Repeat 4.10b through 4.10e for all other bits to be programmed.

g. Enable the chip by applying V_{IL} to the $\overline{CE}_1$ and $\overline{CE}_2$ inputs and V_{IH} to the CE_3 and CE_4 inputs and verify the program.

h. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.10b through 4.10g one time only. Bits which fail to program the second time shall be considered programming rejects.

TABLE IVD. Programming characteristics for circuit D.

Characteristic	Symbol	Conditions 1/	Limits Min	Recommended	Max	Unit
V_{CC} required during programming	V_{CCP}		4.75	5.0	5.25	V
Verification V_{CC} read	V_{CCL}	Programming read verify	4.2	4.4	5.0	V
Input voltage, high level "1"	V_{IH}	Do not leave inputs open	2.4	5.0	5.0	V
Input voltage, low level "0"	V_{IL}	Do not leave inputs open	0	0	0.4	V
Output programming voltage	V_{OUT}	Applied to output to be programmed	20	20.5	21	V
Output programming current	I_{OUT}	If pulse generator is used, set current limit to the maximum value			100	mA
Programming voltage transition time	t_{TLH}		0.5	1.0	3.0	µs
Programming pulse width	t_P		50	100	180	µs
Programming duty cycle	D.C.	Maximum duty cycle to maintain T_A <85°C		20	20	%
Required delay between disabling memory output and application of output programming pulse	t_D		30			ns

1/ T_A = 25°C (recommended); T_A = 85°C (maximum).

4.11 Programming procedures for circuit F. The waveforms on figure 8b, the programming characteristics of table IVE, and the following procedures shall apply:

a. Connect the device in the electrical configuration for programming.

b. Raise V_{CC} to 5.5 volts.

c. Address the PROM with the binary address of the selected word to be programmed. Address inputs are TTL compatible.

d. Disable the chip by applying V_{IH} to the $\overline{CE}$ inputs and V_{IL} to the CE inputs. The chip enable inputs are TTL compatible.

e. Apply the V_{PP} pulse to the programming pin $\overline{CE}_2$. In order to insure that the output transistor is off before increasing voltage on the output pin, the programming pin's voltage pulse shall precede the output pin's programming pulse by T_{D1} and leave after the programming pin's programming pulse by T_{D2} (see figure 8b).

f. Apply only one V_{OUT} pulse with duration of t_p to the output selected for programming. The outputs shall be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time. Note that the PROM is supplied with fuses generating a high-level logic output. Programming a fuse will cause the output to go to a low-level logic in the verify mode.

g. Other bits in the same word may be programmed sequentially by applying V_{OUT} pulses to each output to be programmed.

h. Repeat 4.11c through 4.11g for all other bits to be programmed.

i. Enable the chip by applying V_{IL} to the $\overline{CE}$ inputs and V_{IH} to the CE inputs, and verify the program. Verification may check for a low output by requiring the device to sink 12 mA at V_{CC} = 4.0 V and 0.2 mA at V_{CC} = 7.0 V at T_A = 25°C.

j. For class S and B devices, if any bit does not verify as programmed, it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.11c through 4.11i one time only. Bits which fail to program the second time shall be considered programming rejects.

TABLE IVE. Programming characteristics for circuit F.

Characteristic	Symbol	Conditions	Limits 1/ Min	Recom-mended	Max	Unit
V_{CC} required during programming	V_{CCP}		5.4	5.5	5.6	V
Rise time of programming pulse to data out or programming pin	t_{TLH}		0.34	0.40	0.46	V/µs
Programming voltage on programming pin	V_{PP}		32.5	33	33.5	V
Output programming voltage	V_{OUT}		25.5	26	26.5	V
Programming pin pulse width ($\overline{CE}$)	t_{PP}	Chip disabled, V_{CC} = 5.5 V		100	180	ns
Pulse width of programming voltage	t_P	Chip disabled, V_{CC} = 5.5 V	1		40	µs
Required current limit of power supply feeding programming pin and output during programming	I_L	V_{PP} = 33 V, V_{OUT} = 26 V, V_{CC} = 5.5 V	240			mA
Reouired time delay between disabling memory output and application of output programming pulse	T_{D1}	Measured at 10% levels	70	80	90	µs
Required time delay between removal of programming pulse and enabling memory output	T_{D2}	Measured at 10% levels	100			ns
Output current during verification	I_{OLV1}	Chip enabled, V_{CC} = 4.0 V	11	12	13	mA
	I_{OLV2}	Chip enabled, V_{CC} = 7.0 V	0.19	0.2	0.21	mA
Address input voltage	V_{IH}		2.4	5.0	5.5	V
	V_{IL}		0.0	0.4	0.8	V
Maximum duty cycle during automatic programming of programming pin and output pin	D.C.	t_P/t_C			25	%

1/ T_A = 25°C.

4.12 Programming procedure for circuit G. The programming characteristics on table IV G and the following procedures shall be used for programming:

a. Connect the device in the electrical configuration for programming. The waveforms on figure 8G and the programming characteristics of table IVG shall apply to these procedures.

b. Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more 'active low' chip Enable inputs. NOTE: Address and enable inputs must be driven with TTL logic levels during programming and verification.

c. Increase V_{CC} from nominal to V_{CCP} (10.5 ±0.5 V) with a slew rate limit of I_{RR} (1.0 to 10.0 v/µs). Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750 mA at 11.0 volts.

d. Select the output where a logical high is desired by raising that output voltage to V_{OP} (10.5 ±0.5 V). Limit the slew rate to I_{RR} (1.0 to 10.0 v/µs). This voltage change may occur simultaneously with the V_{CC} increase to V_{CCP}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20 kiliohms minimum (remember that the outputs of the device are disabled at this time).

e. Enable the device by taking the chip Enable(s) to a low level. This is done with a pulse PWE for 10 µs. The 10 µs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

f. Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 5.0 (±0.25 V). The device must be Enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits.

g. If the device is not to be tested for V_{OH} over the entire operating range subsequent to programming, the verification of Step f. is to be performed at a V_{CC} level of 4.0 volts (±0.2 V). V_{OH}, during the 4 volt verification, must be at least 2.0 volts. The 4 volt V_{CC} verification assures minimum V_{OH} levels over the entire operating range.

h. Repeat steps 4.12b thru 4.12f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25 percent. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

i. For class S and B devices, if any bit does not verify as programmed it shall be considered a programming reject. For class C devices, if any bit does not verify as programmed, repeat 4.12b through 4.12f, one time only. Bits which fail to program the second time shall be considered programming rejects.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

TABLE IVG. Programming characteristics for circuit G.

Characteristic	Symbol	Conditions	Limits 1/ Min	Recom-mended	Max	Unit
Required V_{CC} for programming	V_{CCP}		10.0	10.5	11.0	V
I_{CC} during programming	I_{CCP}	V_{CC} = 11 V			750	mA
Required output voltage for programming	V_{OP}		10.0	10.5	11.0	V
Output current while programming	I_{OP}	V_{OUT} = 11 V			20	mA
Rate of voltage change of V_{CC} or output	I_{RR}		1.0		10.0	V/µs
Programming pulse width (Enabled)	PWE		9	10	11	µs
Rquired V_{CC} for verification	V_{CCV}		3.8	4.0	4.2	V
Maximum duty cycle for V_{CC} at V_{CCP}	MDC			25	25	%
Address set-up time	t_1		100			ns
V_{CCP} set-up time	t_2	2/	5			µs
V_{CCP} hold time	t_5		100			ns
V_{OP} set-up time	t_3		100			ns
V_{OP} hold time	t_4		100			ns

1/ T_A = 25°C.

2/ V_{CCP} set-up time may be greater than 0 if V_{CCP} rises at the same rate or faster than V_{OP}.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirements for programming the device, including processing option.

i. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND - - - - - - - - - - - - - - - Electrical ground (common terminal).
I_{IN} - - - - - - - - - - - - - - - Current flowing into an input terminal.
V_{IC} - - - - - - - - - - - - - - - Input clamp voltage.
V_{IN} - - - - - - - - - - - - - - - Voltage level at an input terminal.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead finish C (see 3.3). Longer length leads and lead forming shall not affect the part number. It is intended that spare devices for logistic support be acquired in the unprogrammed condition (see 3.7.1) and programmed by the maintenance activity, except where use quantities for devices with a specific program or pattern justify stocking of preprogrammed devices.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type/manufacturer	Circuit designator	Fusible link	Symbol/ FSCM no.
01	7640/Harris Corporation	A	NiCr	CDW0/34371
01	5340-1/Monolithic Memories, Inc.	B	NiCr	CECD/50364
01	82S140/Signetics Corporation	C	NiCr	CDKB/18324
01	93438/Fairchild Corporation	D	NiCr	CFJ/07263
01	54S475/National Semiconductor	G	TiW	CCXP/27014
02	7641/Harris Corporation	A	NiCr	---
02	5341-1/Monolithic Memories, Inc.	B	NiCr	---
02	82S141/Signetics Corporation	C	NiCr	---
02	93448/Fairchild Corporation	D	NiCr	---
02	54S474/National Semiconductor	G	TiW	---
03	82S115/Signetics Corporation	C	NiCr	---
04	5348-1/Monolithic Memories, Inc.	B	NiCr	---
04	54S473/National Semiconductor	G	TiW	---
05	5349-1/Monolithic Memories, Inc.	B	NiCr	---
05	29621/Raytheon Company	F	NiCr	CRP/07933
05	54S472/National Semiconductor	G	TiW	---

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Agent:
DLA - ES

Preparing activity:
Air Force - 17

(Project 5962-0528)

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DOCUMENT IDENTIFIER *(Number)* AND TITLE MIL-M-38510/208C MICROCIRCUITS, DIGITAL, 4096-BIT SCHOTTKY, BIPOLAR, PROGRAMMABLE READ-ONLY MEMORY (PROM), MONOLITHIC SILICON

NAME OF ORGANIZATION AND ADDRESS OF SUBMITTER

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