54F10, 54F11
Gates

Triple Three-Input NAND ('F10) AND ('F11) Gates

Product Specification

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	$\overline{Y}$('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F10/BCA, 54F11/BCA
14-Pin Ceramic Flat Pack	54F10/BDA, 54F11/BDA
20-Pin Ceramic LLCC	54F10/B2A, 54F11/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A - C	Inputs	1.0/1.0	20μA/0.6mA
Y, $\overline{Y}$	Output	50/33	1.0mA/20mA

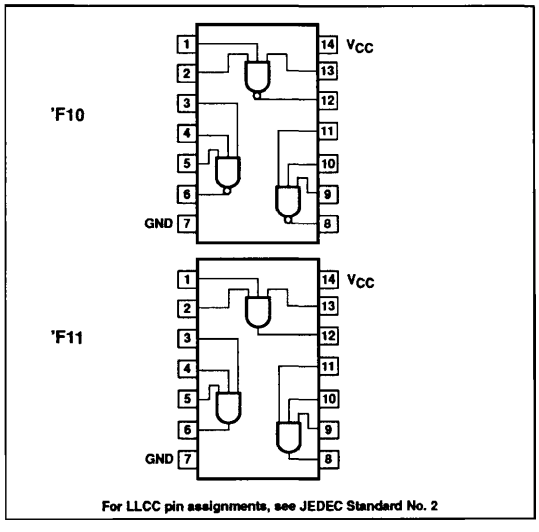
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

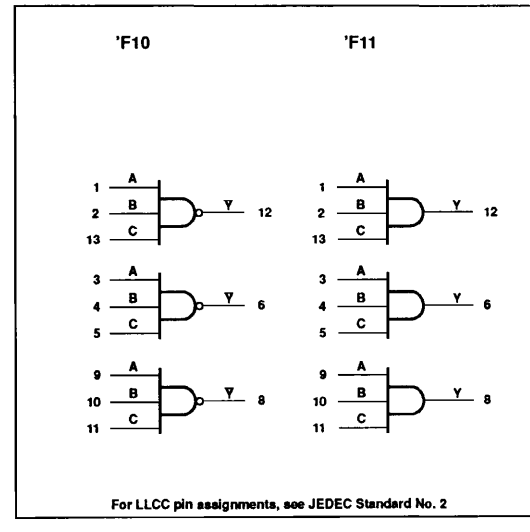
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage			V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage			V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current			V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current			V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = Max, V_O = 0.0V		-60	-75	-150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = Max	V_I = GND		1.8	2.1	mA
			I_{CCL}		$V_I \geq 4.0V$		6.0	7.7	mA
		'F11	I_{CCH}		$V_I \geq 4.0V$		4.7	6.2	mA
			I_{CCL}		V_I = GND		7.2	9.7	mA

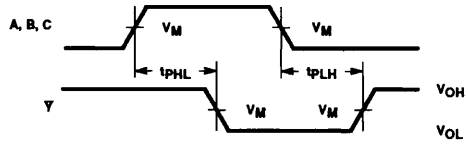
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic".)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B, C to Y	Waveform 1 'F10	2.4	3.7	5.0	2.0	7.0	ns
t_{PHL}			2.0	3.2	4.3	1.5	6.5	ns
t_{PLH}	Propagation delay A, B, C to Y	Waveform 2 'F11	3.0	4.2	5.6	2.5	7.5	ns
t_{PHL}			2.5	4.1	5.5	2.0	7.5	ns

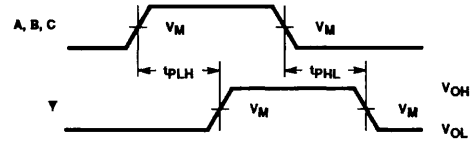
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC WAVEFORMS



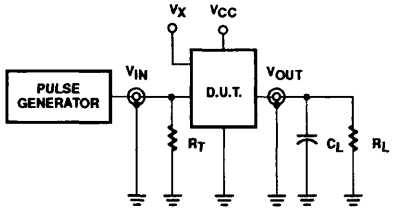
'F10
Waveform 1. For Inverting Outputs



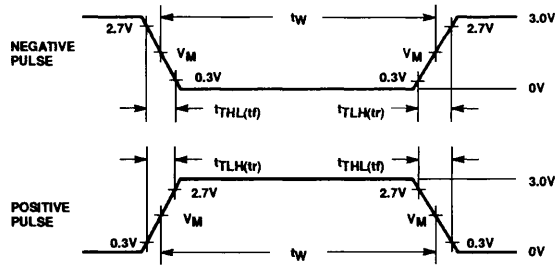
'F11
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns