To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD442002-X

2M-BIT CMOS STATIC RAM
128K-WORD BY 16-BIT
EXTENDED TEMPERATURE OPERATION

Description

The μPD442002-X is a high speed, low power, 2,097,152 bits (131,072 words by 16 bits) CMOS static RAM.

<R> The μPD442002-X is packed in 48-pin PLASTIC FBGA.

<R> Features

- 131,072 words by 16 bits organization
- Fast access time : 70 ns (MAX.)
- Byte data control : /LB (I/O1 to I/O8), /UB (I/O9 to I/O16)
- Low voltage operation : V_{CC} = 2.7 to 3.6 V (-BB70X)
- Low V_{CC} data retention : 1.0 V (MIN.)
- Operating ambient temperature : T_A = –25 to +85 °C
- Output Enable input for easy application

μPD442002	Access time	Operating supply	Operating ambient	Supply current		
	ns (MAX.)	voltage	temperature	At operating	At standby	At data retention
		V	°C	mA (MAX.)	μA (MAX.)	μA (MAX.)
-BB70X	70	2.7 to 3.6	–25 to +85	30	4	2

Document No. M14670EJ9V0DS00 (9th edition)
Date Published December 2007
Printed in Japan

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

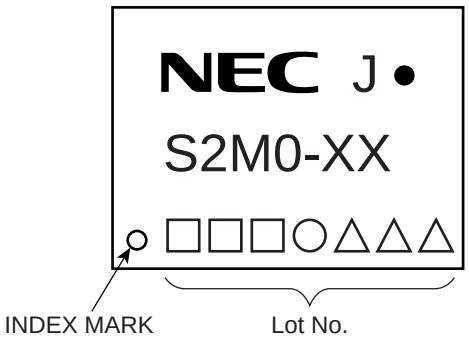
<R> **Ordering Information**

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C
μPD442002F1-BB70X-BC2-A	48-pin PLASTIC FBGA (8×6)	70	2.7 to 3.6	–25 to +85

Remark Products with -A at the end of the part number are lead-free products.

<R> **Marking Image**

Part number	Marking (XX)
μPD442002F1-BB70X-BC2-A	B2

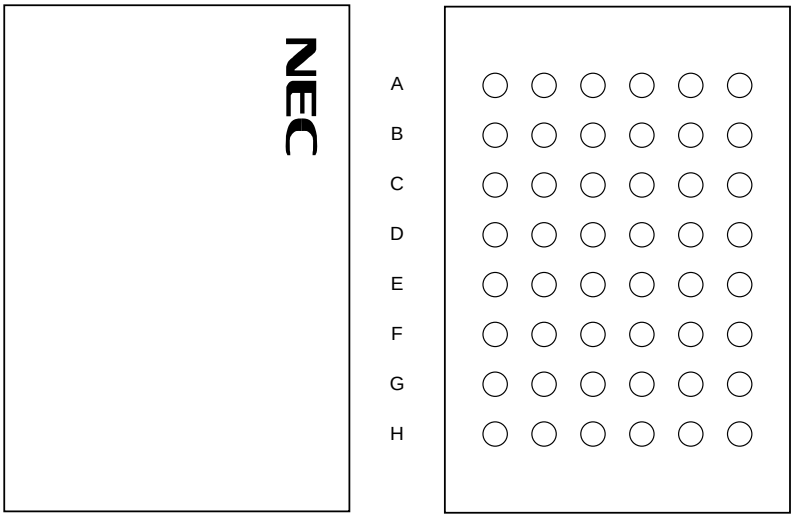


Pin Configuration

/xxx indicates active low signal.

<R> **48-pin PLASTIC FBGA (8×6)**

Top View **Bottom View**



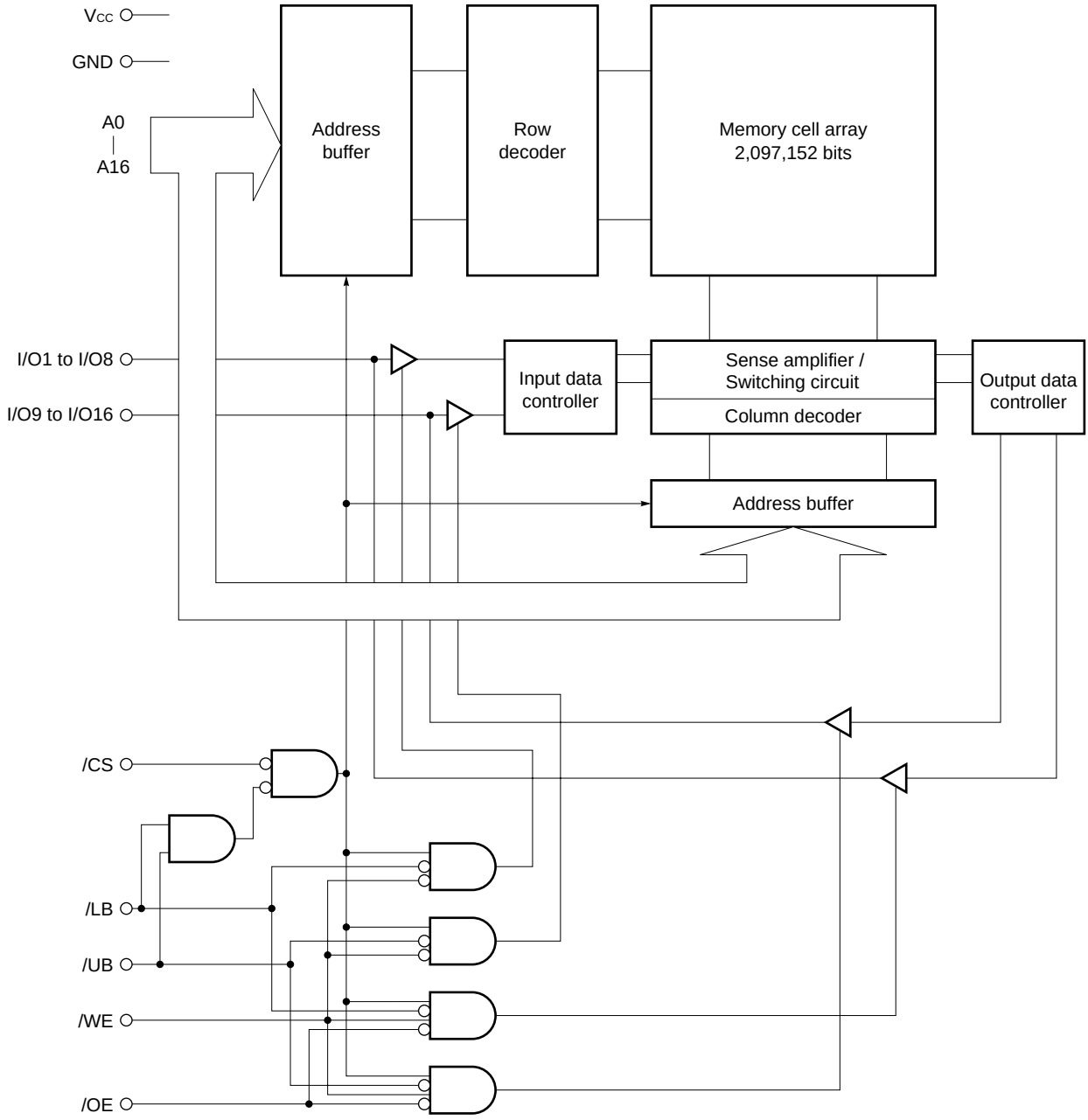
	1	2	3	4	5	6
A	/LB	/OE	A0	A1	A2	NC
B	I/O9	/UB	A3	A4	/CS	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	GND	I/O12	NC	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	NC	A16	I/O5	GND
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	/WE	I/O8
H	NC	A8	A9	A10	A11	NC

	6	5	4	3	2	1
A	NC	A2	A1	A0	/OE	/LB
B	I/O1	/CS	A4	A3	/UB	I/O9
C	I/O3	I/O2	A6	A5	I/O11	I/O10
D	V_{CC}	I/O4	A7	NC	I/O12	GND
E	GND	I/O5	A16	NC	I/O13	V_{CC}
F	I/O7	I/O6	A15	A14	I/O14	I/O15
G	I/O8	/WE	A13	A12	NC	I/O16
H	NC	A11	A10	A9	A8	NC

A0 to A16 : Address inputs
I/O1 to I/O16 : Data inputs / outputs
/CS : Chip Select
/WE : Write Enable
/OE : Output Enable
/LB, /UB : Byte data select
V_{CC} : Power supply
GND : Ground
NC : No Connection

Remark Refer to **Package Drawing** for the index mark.

Block Diagram



Truth Table

/CS	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
						I/O1 to I/O8	I/O9 to I/O16	
H	×	×	×	×	Not selected	High-Z	High-Z	I_{SB}
×	×	×	H	H	Not selected	High-Z	High-Z	
L	H	H	L	×	Output disable	High-Z	High-Z	I_{CCA}
			×	L	Output disable	High-Z	High-Z	
	L	H	L	L	Word read	D_{OUT}	D_{OUT}	
			L	H	Lower byte read	D_{OUT}	High-Z	
			H	L	Upper byte read	High-Z	D_{OUT}	
	×	L	L	L	Word write	D_{IN}	D_{IN}	
			L	H	Lower byte write	D_{IN}	High-Z	
			H	L	Upper byte write	High-Z	D_{IN}	

Remark × : V_{IH} or V_{IL}

Electrical Specifications

<R> **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.5 Note to +4.0	V
Input / Output voltage	V_T		–0.5 Note to V_{CC}+0.4 (4.0 V MAX.)	V
Operating ambient temperature	T_A		–25 to +85	°C
Storage temperature	T_{stg}		–55 to +125	°C

Note –3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

<R> **Recommended Operating Conditions**

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{CC}		2.7	3.6	V
High level input voltage	V_{IH}		2.4	V_{CC}+0.4	V
Low level input voltage	V_{IL}		–0.3 Note	+0.5	V
Operating ambient temperature	T_A		–25	+85	°C

Note –1.0 V (MIN.) (Pulse width : 20 ns)

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are not 100% tested.

<R> **DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{LI}	V_{IN} = 0 V to V_{CC}	–1.0		+1.0	μA
I/O leakage current	I_{LO}	$V_{I/O}$ = 0 V to V_{CC}, /CS = V_{IH} or /WE = V_{IL} or /OE = V_{IH}	–1.0		+1.0	μA
Operating supply current	I_{CCA1}	/CS = V_{IL}, $I_{I/O}$ = 0 mA, Minimum cycle time		–	30	mA
	I_{CCA2}	/CS = V_{IL}, $I_{I/O}$ = 0 mA, Cycle time = ∞		–	4	
	I_{CCA3}	/CS ≤ 0.2 V, Cycle time = 1 μs, $I_{I/O}$ = 0 mA, V_{IL} ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V		–	4	
Standby supply current	I_{SB}	/CS = V_{IH} or /LB = /UB = V_{IH}		–	0.6	mA
	I_{SB1}	/CS ≥ V_{CC} – 0.2 V		0.3	4	μA
	I_{SB2}	/LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V		0.3	4	
High level output voltage	V_{OH}	I_{OH} = –0.5 mA	2.4			V
Low level output voltage	V_{OL}	I_{OL} = 1.0 mA			0.4	V

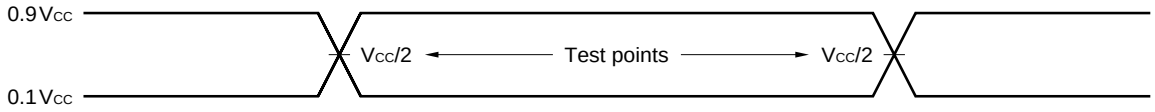
Remark V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

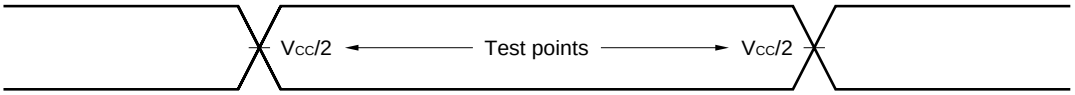
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



<R> **Output Load**

1TTL + 50 pF

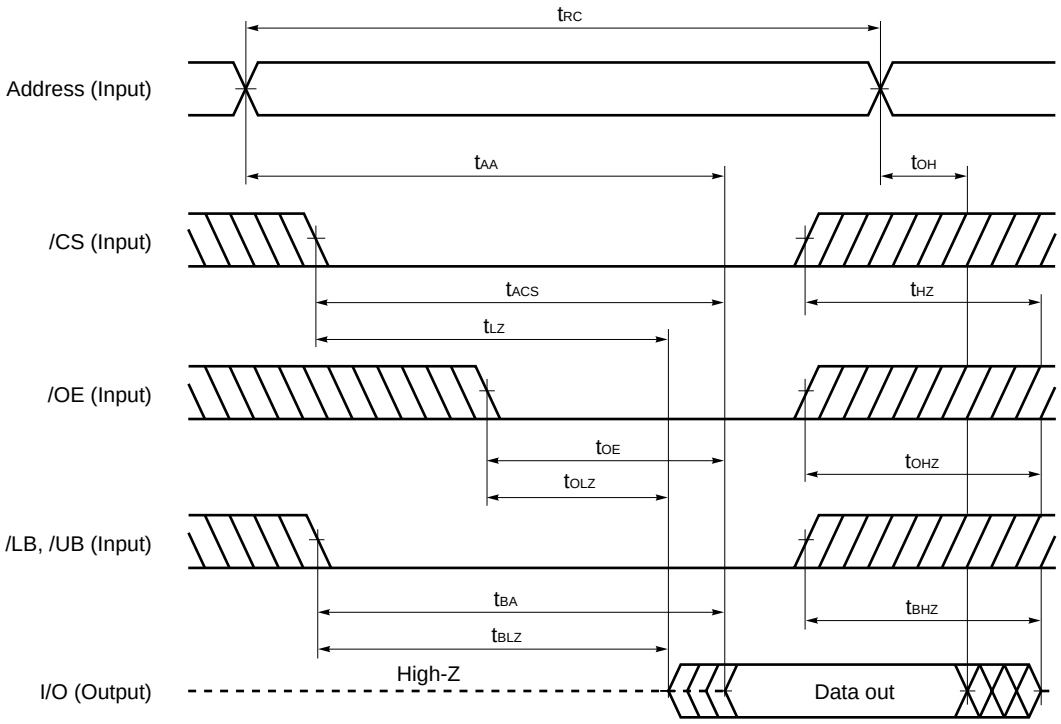
<R> **Read Cycle**

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Read cycle time	t_{RC}	70		ns	
Address access time	t_{AA}		70	ns	**Note 1**
/CS access time	t_{ACS}		70	ns	
/OE to output valid	t_{OE}		35	ns	
/LB, /UB to output valid	t_{BA}		70	ns	
Output hold from address change	t_{OH}	10		ns	
/CS to output in low impedance	t_{LZ}	10		ns	**Note 2**
/OE to output in low impedance	t_{OLZ}	5		ns	
/LB, /UB to output in low impedance	t_{BLZ}	10		ns	
/CS to output in high impedance	t_{HZ}		25	ns	
/OE to output in high impedance	t_{OHZ}		25	ns	
/LB, /UB to output in high impedance	t_{BHZ}		25	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



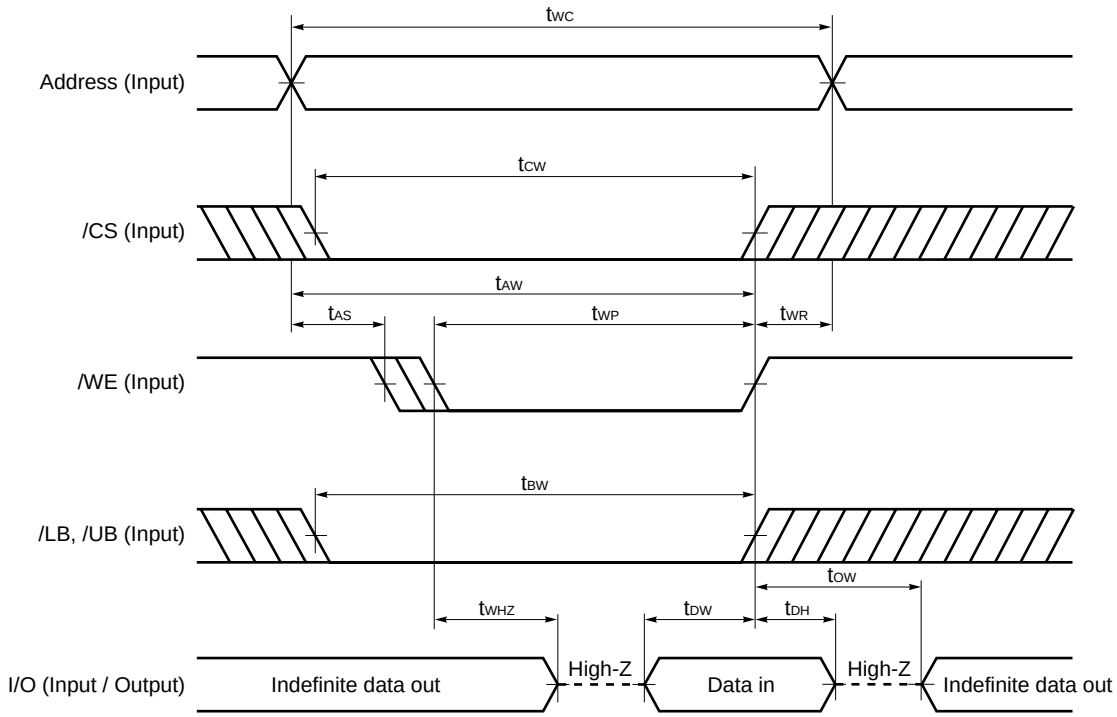
Remark In read cycle, /WE should be fixed to high level.

<R> **Write Cycle**

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Write cycle time	t_{WC}	70		ns	
/CS to end of write	t_{CW}	55		ns	
/LB, /UB to end of write	t_{BW}	55		ns	
Address valid to end of write	t_{AW}	55		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	50		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
/WE to output in high impedance	t_{WHZ}		25	ns	Note
Output active from end of write	t_{OW}	5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle Timing Chart 1 (/WE Controlled)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

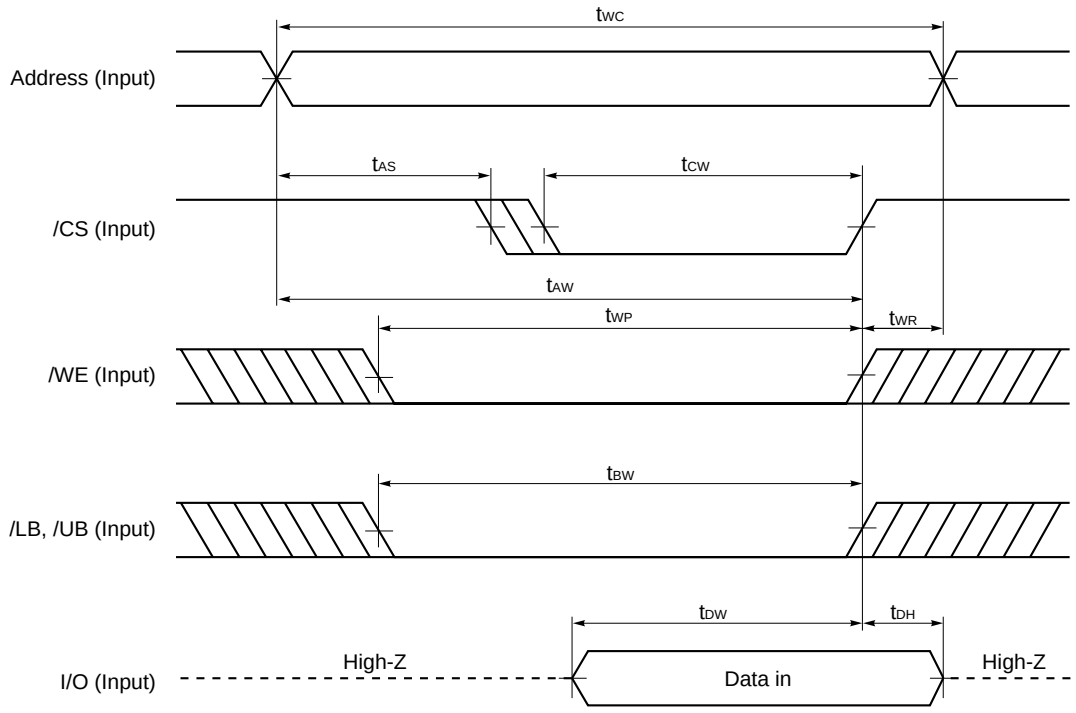
2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

2. If /CS changes to low level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.

3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

Write Cycle Timing Chart 2 (/CS Controlled)

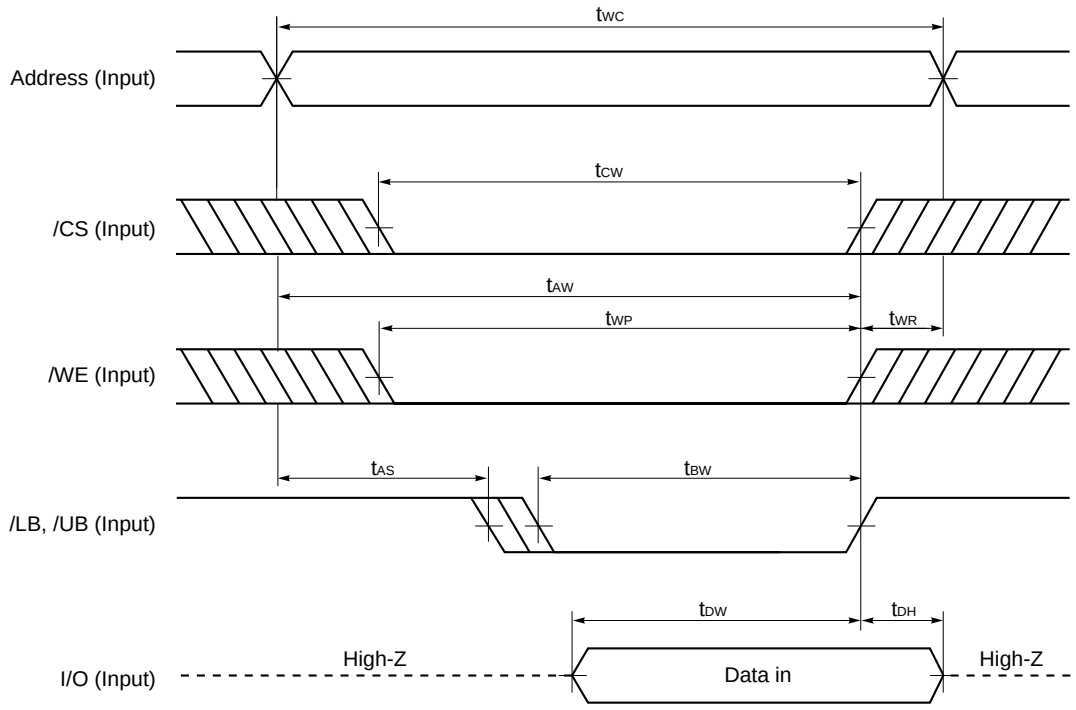


Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

Write Cycle Timing Chart 3 (/LB, /UB Controlled)



Cautions 1. During address transition, at least one of pins /CS, /WE should be inactivated.

2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CS, a low level /WE and a low level /LB (or low level /UB).

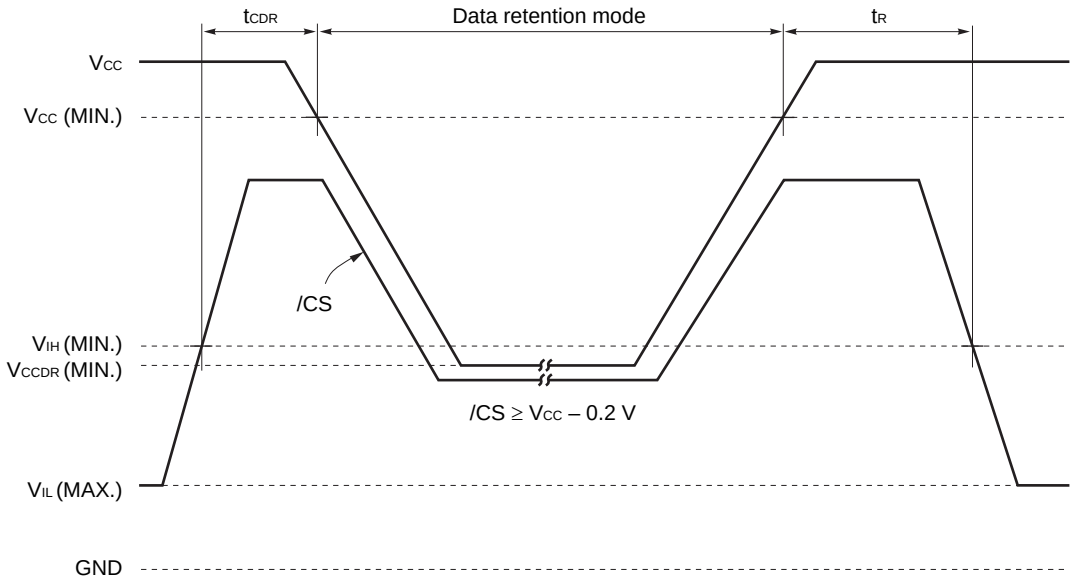
<R> **Low V_{CC} Data Retention Characteristics (T_A = –25 to +85°C)**

Parameter	Symbol	Test Condition	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{CCDR1}	/CS ≥ V_{CC} – 0.2 V	1.0		3.6	V
	V_{CCDR2}	/LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V	1.0		3.6	
Data retention supply current	I_{CCDR1}	V_{CC} = 1.2 V, /CS ≥ V_{CC} – 0.2 V		0.15	2	μA
	I_{CCDR2}	V_{CC} = 1.2 V, /LB = /UB ≥ V_{CC} – 0.2 V, /CS ≤ 0.2 V		0.15	2	
Chip deselection to data retention mode	t_{CDR}		0			ns
Operation recovery time	t_R		t_{RC} Note			ns

Note t_{RC} : Read cycle time

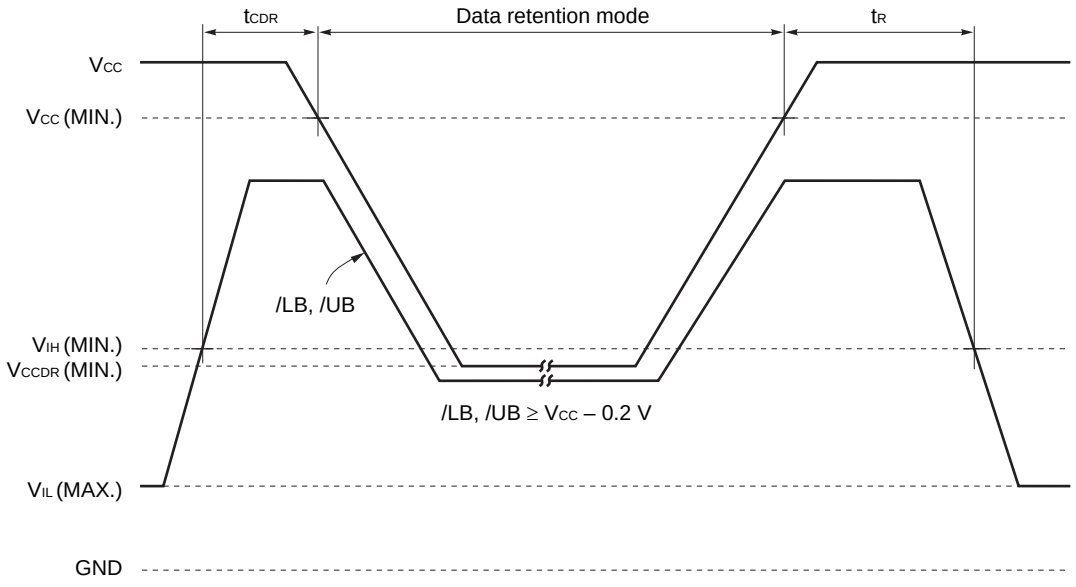
<R> **Data Retention Timing Chart**

(1) /CS Controlled



Remark On the data retention mode by controlling /CS, the other pins (Address, I/O, /WE, /OE, /LB, /UB) can be in high impedance state.

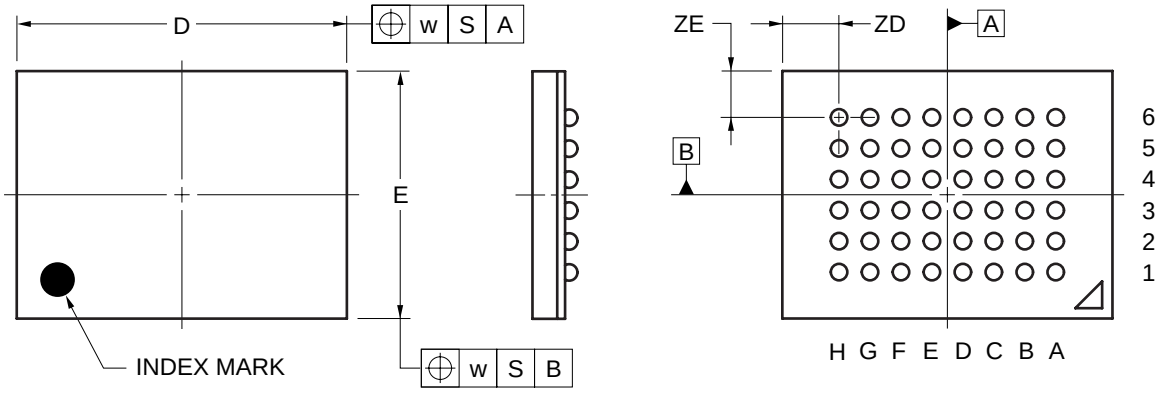
(2) /LB, /UB Controlled

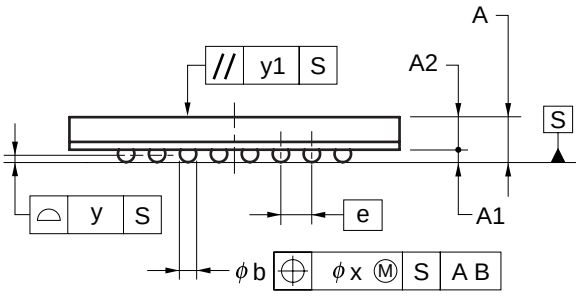


Remark On the data retention mode by controlling /LB and /UB, the input level of /CS must be ≥ V_{CC} – 0.2 V or ≤ 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

<R> **Package Drawing**

48-PIN PLASTIC FBGA (8x6)





(UNIT:mm)

ITEM	DIMENSIONS
D	8.00±0.10
E	6.00±0.10
w	0.20
A	1.09±0.10
A1	0.30±0.05
A2	0.79
e	0.75
b	0.40±0.05
x	0.08
y	0.10
y1	0.20
ZD	1.375
ZE	1.125

P48F1-75-BC2

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD442002-X.

<R> **Types of Surface Mount Device**

μPD442002F1-BC2-A : 48-pin PLASTIC FBGA (8x6)

Quality Grade

- A quality grade of the products is “Standard”.
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
9th edition/ Dec. 2007	p.1	p.1	Modification	Description	48-pin TAPE FBGA (8×6) (F9-BC2) → 48-pin PLASTIC FBGA (8×6) (F1-BC2)
	p.2	p.2		Ordering Information, Marking Image	
	p.3	p.3		Pin Configuration	
	p.17	p.18		Package Drawing	
	p.18	p.19		Types of Surface Mount Device	
	p.1	p.1	Deletion	Features	Delete –BC70X, –DD85X and –DD10X
	p.2	p.2		Ordering Information, Marking Image	
	p.6	p.6		Absolute Maximum Ratings	
	p.6	p.6		Recommended Operating Conditions	
	p.7	pp.7-8		DC Characteristics	
	p.8	p.9		AC Test Conditions	
	p.9	p.10		Read Cycle	
	p.11	p.12		Write Cycle	
	p.15	p.16		Low V_{CC} Data Retention Characteristics	
	p.16	p.17		Data Retention Timing Chart	Delete Note

[MEMO]

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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