ECL 10KH High-Speed Emitter-Coupled Logic Family Dual Latch MC10H130

Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation, 155 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

Description

The MC10H130 is a dual latch which has two different mechanisms to retain data through latch control signals. Each latch can be operated separately by holding the common latch control signal ($\overline{C}$) LOW, then switching an individual latch control signal ($\overline{CE1}$/$\overline{CE2}$) from LOW to HIGH to cause retention of data in the relevant latch. If simultaneous operation of both latches is required, $\overline{CE1}$ and $\overline{CE2}$ are held LOW and the common latch control C is switched from LOW to HIGH.

For either latch, data present at the inputs (D1/D2) will be seen at the outputs (Q1/$\overline{Q1}$ and Q2/$\overline{Q2}$) when both latch control signals are LOW. This condition allows data to be setup within the latch, after which time causing a positive transition to the HIGH state on either or both latch control signals causes data retention. After either or both of these signals are HIGH, subsequent changes in data at an input are ignored by the latch, provided the hold time requirement is met.

An alternative means to load data in the latches is to use the direct set and reset (S1/S2 and R1/R2, respectively) lines. These inputs do not override the latch controls, or the D inputs. Instead, set or reset are only effective when either $\overline{C}$, $\overline{CE1}$/$\overline{CE2}$ or both, are HIGH. Note that this relationship is different than the case for a similar part, the MC10H131, which is a Dual Master-Slave D-type Flip-Flop.

Function Table

D	$\overline{C}$	$\overline{CE1}$/$\overline{CE2}$	R	S	$Q_{n=1}$
L	L	L	X	X	L
H	L	L	X	X	H
X	H	X	L	L	Q_n
X	H	X	L	H	H
X	H	X	H	L	L
X	H	X	H	H	N.D.
X	X	H	L	L	Q_n
X	X	H	L	H	H
X	X	H	H	L	L
X	X	H	H	H	N.D.

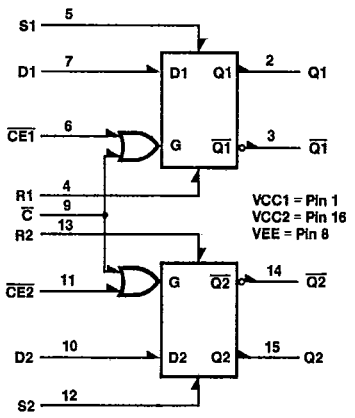
X = Don't Care
N.D. = Not Defined

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE
MC10H130	J,N,NL(20)	Com

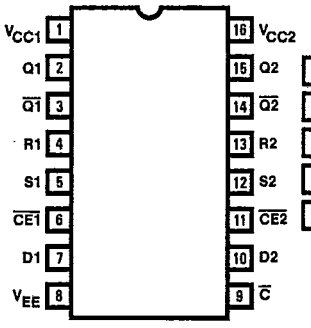
Logic Diagram

MC10H130
Dual Latch

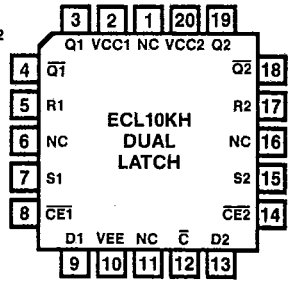


Pin Configurations

MC10H130
Dual Latch



MC10H130



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Absolute Maximum Ratings

Supply voltage V_{EE} (V_{CC} = 0) ..... -8.0 V to $0V_{dc}$
Input voltage V_I (V_{CC} = 0) ..... $0V_{dc}$ to V_{EE}
Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	TYP	MAX	UNIT
V_{EE}	Supply voltage		-5.46	-5.2	-4.94	V
T_A	Operating temperature range		0		75	°C
T_{stg}	Storage temperature range	Plastic	-55		150	°C
		Ceramic	-55		165	

Electrical Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
I_E	Power supply current		—	38	—	35	—	38	mA
I_{inH}	Input current HIGH	Pins 6, 11	—	468	—	275	—	275	µA
		Pins 7, 9, 10	—	545	—	320	—	320	
		Pins 4, 5, 12, 13	—	434	—	255	—	255	
I_{inL}	Input current LOW		0.5	—	0.5	—	0.3	—	µA
V_{OH}	HIGH output voltage		-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V_{OL}	LOW output voltage		-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V_{IH}	HIGH input voltage		-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
V_{IL}	LOW input voltage		-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

Switching Characteristics V_{EE} = -5.2 V ±5% (See Note)

SYMBOL	PARAMETER		0° MIN	0° MAX	25° MIN	25° MAX	75° MIN	75° MAX	UNIT
t_{pd}	Propagation delay	Data	0.40	1.60	0.40	1.70	0.40	1.80	ns
		Set, Reset	0.60	1.70	0.70	1.80	1.80	1.90	
		Clock, CE	0.50	1.60	0.50	1.70	1.70	1.80	
t_r,t+	Rise time (20%-80%)		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_f,t-	Fall time (80%-20%)		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_{set}	Setup time		0.5	1.6	0.5	1.7	0.5	1.8	ns
t_{hold}	Hold time		0.5	1.6	0.7	—	0.7	—	ns

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to -2.0 V.