128Kx8 MONOLITHIC SRAM *PRELIMINARY**

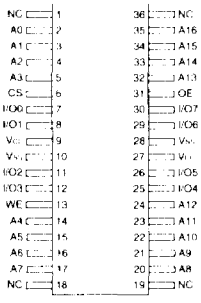
FEATURES

- Access Times 17, 20, 25, 35, 45, 55nS
- Radiation Tolerant Devices Available
- Packaging
  - 36 pin Ceramic Flat Pack, JEDEC Approved Revolutionary Pinout (Package 200)
  - 36 pin Ceramic SOJ, JEDEC Approved Revolutionary Pinout (Package 100)
  - 32 pin Ceramic DIP, JEDEC Approved Pinout (Package 300)
- MIL-STD-883 Compliant Devices Available
- Commercial, Industrial and Military Temperature Range
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs

* *This data sheet describes a product not fully characterized and is subject to change*

FIG. 1 PIN CONFIGURATION FOR WMS128K8-XFX

TOP VIEW
FLAT PACK

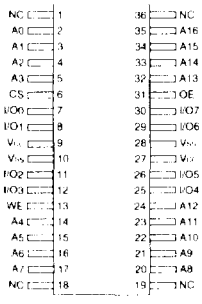


PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

FIG. 2 PIN CONFIGURATION FOR WMS128K8-XDJX

TOP VIEW
CSOJ

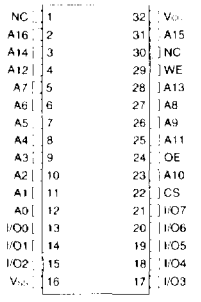


PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

FIG. 3 PIN CONFIGURATION FOR WMS128K8-XCX

TOP VIEW
DIP



PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	20	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	20	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

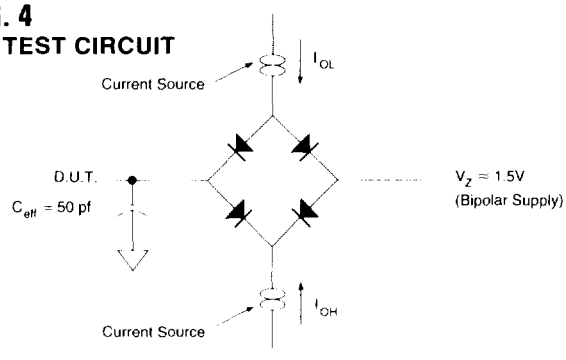
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		110		110		110	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		30		30		30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		110		70		70	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		30		25		25	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	nS
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Read Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Read Cycle Time	t_{RC}	17		20		25		35		45		55		nS
Address Access Time	t_{AA}		17		20		25		35		45		55	nS
Output Hold from Address Change	t_{OH}	5		5		5		5		5		5		nS
Chip Select Access Time	t_{ACS}		17		20		25		35		45		55	nS
Output Enable to Output Valid	t_{OE}		9		10		12		25		35		45	nS
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		5		5		5		nS
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		5		5		nS
Chip Disable to Output in High Z	t_{CHZ}[1]		10		10		12		15		15		15	nS
Output Disable to Output in High Z	t_{OHZ}[1]		10		10		12		15		15		15	nS

1. This parameter is guaranteed by design but not tested.

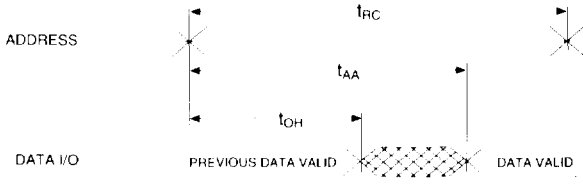
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

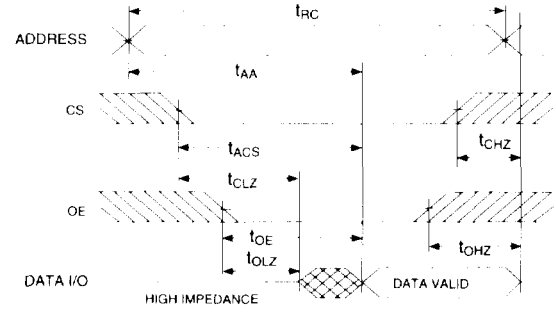
Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Write Cycle		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Write Cycle Time	t_{WC}	17		20		25		35		45		55		nS
Chip Select to End of Write	t_{CW}	13		15		20		25		30		45		nS
Address Valid to End of Write	t_{AW}	13		15		20		25		30		45		nS
Data Valid to End of Write	t_{DW}	9		10		15		20		25		40		nS
Write Pulse Width	t_{WP}	13		15		20		25		30		45		nS
Address Setup Time	t_{AS}	0		0		0		0		0		0		nS
Address Hold Time	t_{AH}	0		0		0		0		0		0		nS
Output Active from End of Write	t_{OW}[1]	5		5		5		5		5		5		nS
Write Enable to Output in High Z	t_{WHZ}[1]		10		12		15		20		25		25	nS
Data Hold Time	t_{DH}	0		0		0		0		0		0		nS

1. This parameter is guaranteed by design but not tested.

FIG. 5
TIMING WAVEFORM - READ CYCLE

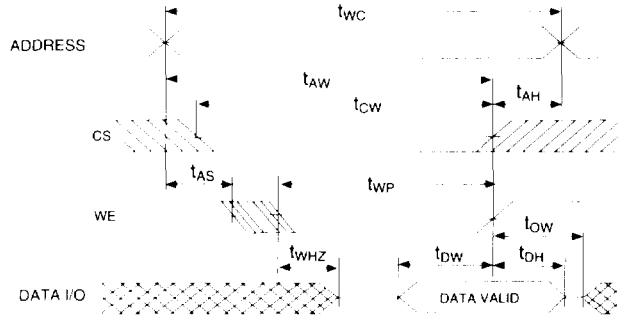


READ CYCLE 1 (CS = OE = V_{IL}, WE = V_{IH})



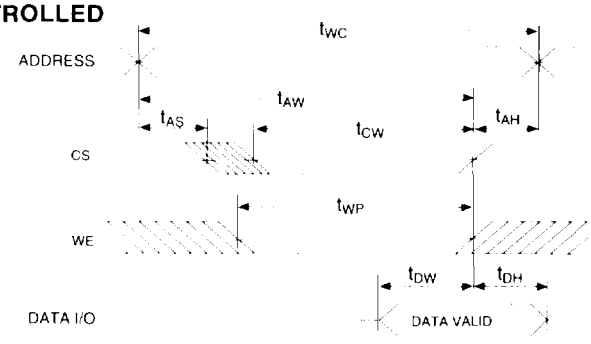
READ CYCLE 2 ($WE = V_{IH}$)

FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



WRITE CYCLE 1, WE CONTROLLED ($OE = V_{IH}$)

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, CS CONTROLLED ($OE = V_{IH}$)

ORDERING INFORMATION