# DATA SHEET

# 74ALVCH162601

## 18-bit universal bus transceiver with 30 Ω termination resistor; 3-state

Product specification
1999 Oct 14
File under Integrated Circuits, IC24

Philips
Semiconductors

PHILIPS

# 18-bit universal bus transceiver with 30 Ω termination resistor; 3-state

# 74ALVCH162601

## FEATURES

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and ground pins for minimum noise and ground bounce
- All data inputs have bus hold circuitry
- Integrated 30 Ω termination resistors.

## DESCRIPTION

The 74ALVCH162601 is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($\overline{OE}_{AB}$ and $\overline{OE}_{BA}$), and clock ($CP_{AB}$ and $CP_{BA}$) inputs. For A-to-B data flow, the device operates in the transparent mode when $LE_{AB}$ is HIGH. When $LE_{AB}$ is LOW, the A data is latched if $CP_{AB}$ is held at a HIGH or LOW logic level. If $LE_{AB}$ is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of $CP_{AB}$. When $\overline{OE}_{AB}$ is LOW, the outputs are active. When $\overline{OE}_{AB}$ is HIGH, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($\overline{CE}_{BA}$/$\overline{CE}_{AB}$).

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{OE}_{BA}$, $LE_{BA}$ and $CP_{BA}$.

To ensure the high-impedance state during power-down, $\overline{OE}_{BA}$ and $\overline{OE}_{AB}$ should be tied to $V_{CC}$ through a pull-up resistor, the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The 74ALVCH162601 is designed with 30 Ω series resistors in both HIGH or LOW output stage.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## QUICK REFERENCE DATA

Ground = 0; $T_{amb}$ = 25 °C; $t_r = t_f$ = 2.5 ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | propagation delay $A_n$, $B_n$ to $B_n$, $A_n$ | $C_L$ = 30 pF; $V_{CC}$ = 2.5 V | 4.0 | ns |
| | | $C_L$ = 50 pF; $V_{CC}$ = 3.3 V | 3.1 | ns |
| $C_{I/O}$ | input/output capacitance | | 8.0 | pF |
| $C_I$ | input capacitance | | 4.0 | pF |
| $C_{PD}$ | power dissipation capacitance per latch | notes 1 and 2 | | |
| | | outputs enabled | 21 | pF |
| | | outputs disabled | 3 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz;

   $f_o$ = output frequency in MHz;

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

   $C_L$ = output load capacitance in pF;

   $V_{CC}$ = supply voltage in Volts.
2. The condition is $V_I$ = GND to $V_{CC}$.

## FUNCTION TABLE

See note 1.

| INPUTS | | | | | OUTPUTS | STATUS |
|---|---|---|---|---|---|---|
| $\overline{CE}_{XX}$ | $\overline{OE}_{XX}$ | $LE_{XX}$ | $CP_{XX}$ | $A_n$, $B_n$ | | |
| X | H | X | X | X | Z | disabled |
| X<br>X | L<br>L | H<br>H | X<br>X | H<br>L | H<br>L | transparent |
| H | L | L | X | X | NC | hold |
| L<br>L | L<br>L | L<br>L | ↑<br>↑ | h<br>l | H<br>L | clock and display |
| L<br>L | L<br>L | L<br>L | L<br>H | X<br>X | NC | hold |

**Note**

1. XX = AB for A-to-B direction, BA for B-to-A direction;
   H = HIGH voltage level;
   L = LOW voltage level;
   h = HIGH state must be present one set-up time before the LOW-to-HIGH transition of $CP_{XX}$;
   l = LOW state must be present one set-up time before the LOW-to-HIGH transition of $CP_{XX}$;
   X = don't care;
   ↑ = LOW-to-HIGH level transition;
   NC = no change;
   Z = high-impedance OFF-state.

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|---|---|---|---|---|---|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74ALVCH162601DGG | −40 to +85 °C | 56 | TSSOP | plastic | SOT364-1 |

**PINNING**

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | $\overline{OE}_{AB}$ | output enable A-to-B |
| 2 | $LE_{AB}$ | latch enable A-to-B |
| 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26 | $A_0$ to $A_{17}$ | data inputs/outputs |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | ground (0 V) |
| 7, 22, 35, 50 | $V_{CC}$ | DC supply voltage |
| 27 | $\overline{OE}_{BA}$ | output enable B-to-A |
| 28 | $LE_{BA}$ | latch enable B-to-A |
| 29 | $\overline{CE}_{BA}$ | clock enable B-to-A |
| 30 | $CP_{BA}$ | clock input B-to-A |
| 31, 33, 34, 36, 37, 38, 40, 41, 42, 43, 44, 45, 47, 48, 49, 51, 52, 54 | $B_{17}$ to $B_0$ | data inputs/outputs |
| 55 | $CP_{AB}$ | clock input A-to-B |
| 56 | $\overline{CE}_{AB}$ | clock enable A-to-B |

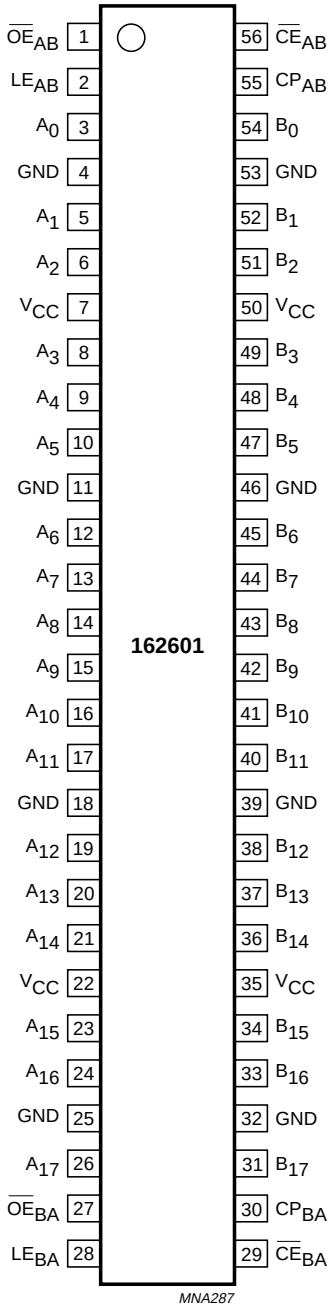



Fig.1 Pin configuration.

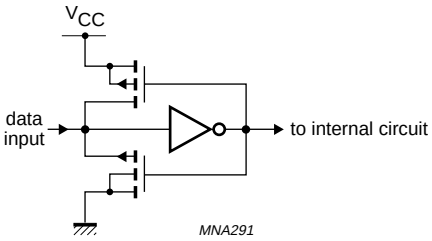



Fig.2 Bus hold circuit.

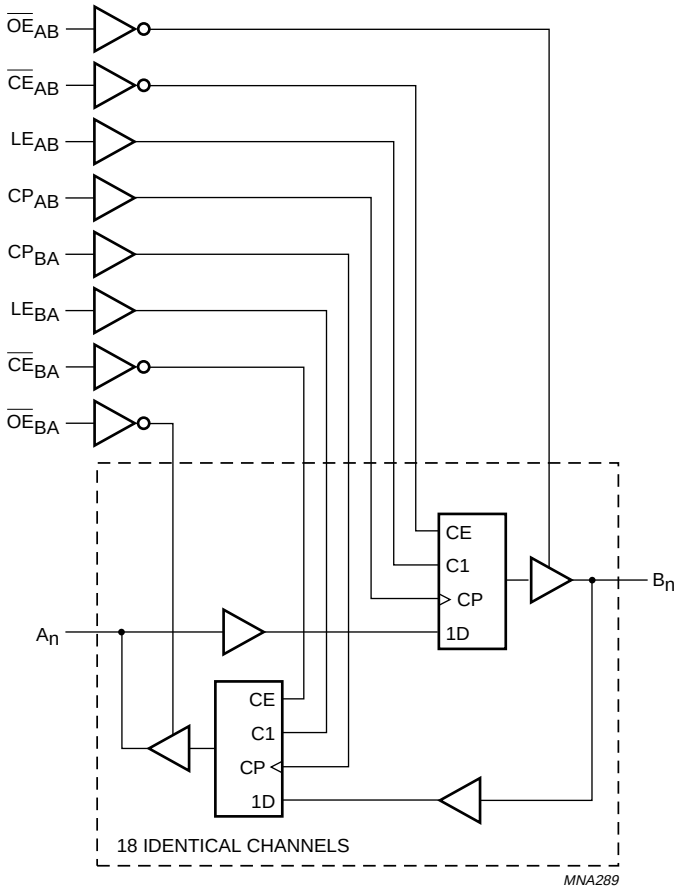



Fig.3 Logic diagram (one section).

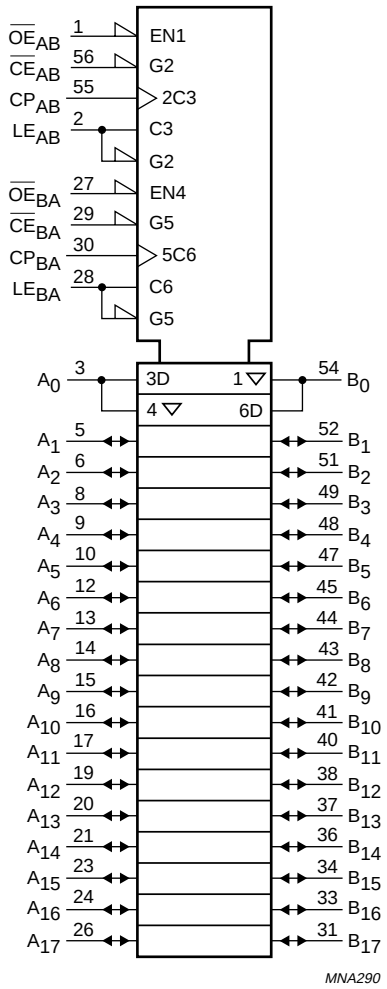



Fig.4 IEC logic symbol.

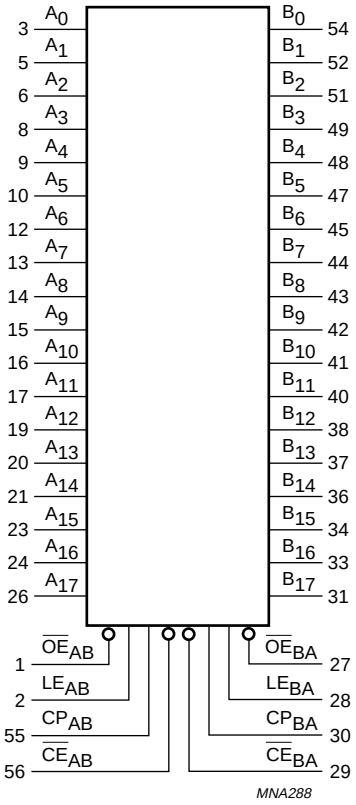



Fig.5 Logic symbol.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | | | | |
| | for max. speed performance | $C_L$ = 30 pF | 2.3 | 2.5 | 2.7 | V |
| | for max. speed performance | $C_L$ = 50 pF | 3.0 | 3.3 | 3.6 | V |
| | for low-voltage applications | | 1.2 | 2.4 | 3.6 | V |
| $V_I$ | DC input voltage | | 0 | – | $V_{CC}$ | V |
| $V_O$ | DC output voltage | | 0 | – | $V_{CC}$ | V |
| $T_{amb}$ | operating ambient temperature | in free air | –40 | – | +85 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 2.3 to 3.0 V | 0 | – | 20 | ns/V |
| | | $V_{CC}$ = 3.0 to 3.6 V | 0 | – | 10 | ns/V |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 | +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I$ < 0 | – | –50 | mA |
| $V_I$ | DC input voltage | note 1 | –0.5 | +4.6 | V |
| $I_{OK}$ | DC output diode current | $V_O$ > $V_{CC}$ or $V_O$ < 0 | – | ±50 | mA |
| $V_O$ | DC output voltage | note 1 | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_O$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | – | ±50 | mA |
| $I_{CC}$, $I_{GND}$ | DC $V_{CC}$ or GND current | | – | ±100 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$ | power dissipation | for temperature range: –40 to +125 °C; note 2 | – | 600 | mW |

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of $P_{tot}$ derates linearly with 8 mW/K.

## DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | | $T_{amb}$ = −40 TO +85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | $V_I$ (V) | OTHER | $V_{CC}$ (V) | MIN. | TYP.(1) | MAX. | |
| $V_{IH}$ | HIGH-level input voltage | | | 2.3 to 2.7 | 1.7 | 1.2 | – | V |
| | | | | 2.7 to 3.6 | 2.0 | 1.5 | – | |
| $V_{IL}$ | LOW-level input voltage | | | 2.3 to 2.7 | – | 1.2 | 0.7 | V |
| | | | | 2.7 to 3.6 | – | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH-level output voltage | $V_{IH}$ or $V_{IL}$ | $I_O$ = −100 μA | 2.3 to 3.6 | $V_{CC}$ − 0.2 | $V_{CC}$ | – | V |
| | | | $I_O$ = −4 mA | 2.3 | $V_{CC}$ − 0.4 | $V_{CC}$ − 0.11 | – | |
| | | | $I_O$ = −6 mA | 2.3 | $V_{CC}$ − 0.6 | $V_{CC}$ − 0.17 | – | |
| | | | $I_O$ = −4 mA | 2.7 | $V_{CC}$ − 0.5 | $V_{CC}$ − 0.09 | – | |
| | | | $I_O$ = −8 mA | 2.7 | $V_{CC}$ − 0.7 | $V_{CC}$ − 0.19 | – | |
| | | | $I_O$ = −6 mA | 3.0 | $V_{CC}$ − 0.6 | $V_{CC}$ − 0.13 | – | |
| | | | $I_O$ = −12 mA | 3.0 | $V_{CC}$ − 1.0 | $V_{CC}$ − 0.27 | – | |
| $V_{OL}$ | LOW-level output voltage | $V_{IH}$ or $V_{IL}$ | $I_O$ = 100 μA | 2.3 to 3.6 | – | GND | 0.20 | V |
| | | | $I_O$ = 4 mA | 2.3 | – | 0.07 | 0.40 | |
| | | | $I_O$ = 6 mA | 2.3 | – | 0.11 | 0.55 | |
| | | | $I_O$ = 4 mA | 2.7 | – | 0.06 | 0.40 | |
| | | | $I_O$ = 8 mA | 2.7 | – | 0.13 | 0.60 | |
| | | | $I_O$ = 6 mA | 3.0 | – | 0.09 | 0.55 | |
| | | | $I_O$ = 12 mA | 3.0 | – | 0.19 | 0.80 | |
| $I_I$ | input leakage current | $V_{CC}$ or GND | | 2.3 to 3.6 | – | 0.1 | 5 | μA |
| $I_{OZ}$ | 3-state output OFF-state current | $V_{IH}$ or $V_{IL}$ | $V_O$ = $V_{CC}$ or GND | 2.3 to 3.6 | – | 0.1 | 10 | μA |
| $I_{CC}$ | quiescent supply voltage | $V_{CC}$ or GND | $I_O$ = 0 | 2.3 to 3.6 | – | 0.2 | 40 | μA |
| $\Delta I_{CC}$ | additional quiescent supply current given per data I/O pin with bus hold | $V_{CC}$ − 0.6 | $I_O$ = 0 | 2.3 to 3.6 | – | 150 | 750 | μA |
| $I_{BHL}$ | bus hold LOW sustaining current | 0.7(2) | | 2.3(2) | 45 | – | – | μA |
| | | 0.8(2) | | 3.0(2) | 75 | 150 | – | |
| $I_{BHH}$ | bus hold HIGH sustaining current | 1.7(2) | | 2.3(2) | −45 | | – | μA |
| | | 2.0(2) | | 3.0(2) | −75 | −175 | – | |
| $I_{BHLO}$ | bus hold LOW overdrive current | | | 3.6(2) | 500 | – | – | μA |
| $I_{BHHO}$ | bus hold LOW overdrive current | | | 3.6(2) | −500 | – | – | μA |

**Notes**

1. All typical values are measured at $T_{amb}$ = 25 °C.
2. Valid for data inputs of bus hold parts.

**AC CHARACTERISTICS FOR $V_{CC}$ = 2.3 TO 2.7 V**

Ground = 0 V; $t_r = t_f \leq 2.0$ ns; $C_L$ = 30 pF.

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_{amb}$ = −40 TO +85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $V_{CC}$ (V) | MIN. | TYP.(1) | MAX. | |
| $t_{PHL}/t_{PLH}$ | propagation delay $A_n$, $B_n$ to $B_n$, $A_n$ | see Figs 6 and 10 | 2.3 to 2.7 | 1.3 | 4.0 | 5.3 | ns |
| | propagation delay $LE_{AB}$, $LE_{BA}$ to $B_n$, $A_n$ | see Figs 7 and 10 | 2.3 to 2.7 | 1.0 | 4.5 | 6.0 | ns |
| | propagation delay $CP_{AB}$, $CP_{BA}$ to $B_n$, $A_n$ | see Figs 7 and 10 | 2.3 to 2.7 | 1.5 | 4.7 | 6.4 | ns |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time $\overline{OE}_{AB}$, $\overline{OE}_{BA}$ to $B_n$, $A_n$ | see Figs 8 and 10 | 2.3 to 2.7 | 1.6 | 3.9 | 6.1 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time $\overline{OE}_{AB}$, $\overline{OE}_{BA}$ to $B_n$, $A_n$ | see Figs 8 and 10 | 2.3 to 2.7 | 1.8 | 2.6 | 5.7 | ns |
| $t_W$ | clock pulse width HIGH $LE_{AB}$ or $LE_{BA}$ | see Figs 7 and 10 | 2.3 to 2.7 | 3.3 | 1.6 | – | ns |
| | clock pulse width HIGH or LOW $CP_{AB}$ or $CP_{BA}$ | see Figs 7 and 10 | 2.3 to 2.7 | 3.3 | 2.0 | – | ns |
| $t_{su}$ | set-up time $A_n$, $B_n$ to $CP_{AB}$, $CP_{BA}$ | see Figs 9 and 10 | 2.3 to 2.7 | +2.3 | −0.2 | – | ns |
| | set-up time $A_n$, $B_n$ to $LE_{AB}$, $LE_{BA}$ | see Figs 9 and 10 | 2.3 to 2.7 | 1.3 | 0.1 | – | ns |
| | set-up time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to $CP_{AB}$, $CP_{BA}$ | | 2.3 to 2.7 | +2.0 | −0.4 | – | ns |
| $t_h$ | hold time $A_n$, $B_n$ to $CP_{AB}$, $CP_{BA}$ | see Figs 9 and 10 | 2.3 to 2.7 | 1.2 | 0.3 | – | ns |
| | hold time $A_n$, $B_n$ to $LE_{AB}$, $LE_{BA}$ | see Figs 9 and 10 | 2.3 to 2.7 | 1.3 | 0.2 | – | ns |
| | hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to $CP_{AB}$, $CP_{BA}$ | | 2.3 to 2.7 | 1.1 | 0.4 | – | ns |
| $f_{max}$ | maximum clock pulse frequency | see Figs 7 and 10 | 2.3 to 2.7 | 150 | 190 | – | MHz |

**Note**

1. All typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 2.5 V.

**AC CHARACTERISTICS FOR $V_{CC}$ = 2.7 V AND $V_{CC}$ = 3.0 TO 3.6 V**

Ground = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L$ = 50 pF.

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_{amb}$ = −40 TO +85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $V_{CC}$ (V) | MIN. | TYP.(1) | MAX. | |
| $t_{PHL}/t_{PLH}$ | propagation delay $A_n$, $B_n$ to $B_n$, $A_n$ | see Figs 6 and 10 | 2.7 | – | 3.9 | 5.2 | ns |
| | | | 3.0 to 3.6 | 1.6 | 3.1(2) | 4.5 | |
| | propagation delay $LE_{AB}$, $LE_{BA}$ to $B_n$, $A_n$ | see Figs 7 and 10 | 2.7 | – | 4.3 | 5.9 | ns |
| | | | 3.0 to 3.6 | 1.5 | 3.5(2) | 5.1 | |
| | propagation delay $CP_{AB}$, $CP_{BA}$ to $B_n$, $A_n$ | see Figs 7 and 10 | 2.7 | – | 4.5 | 6.3 | ns |
| | | | 3.0 to 3.6 | 1.6 | 3.7(2) | 5.5 | |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time $\overline{OE}_{AB}$, $\overline{OE}_{BA}$ to $B_n$, $A_n$ | see Figs 8 and 10 | 2.7 | – | 3.9 | 6.7 | ns |
| | | | 3.0 to 3.6 | 1.6 | 3.1(2) | 5.7 | |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time $\overline{OE}_{AB}$, $\overline{OE}_{BA}$ to $B_n$, $A_n$ | see Figs 8 and 10 | 2.7 | – | 3.2 | 5.3 | ns |
| | | | 3.0 to 3.6 | 1.8 | 2.9(2) | 4.8 | |
| $t_W$ | clock pulse width $LE_{AB}$, $LE_{BA}$ to $CP_{AB}$, $CP_{BA}$ | see Figs 7 and 10 | 2.7 | 3.3 | 0.7 | – | ns |
| | | | 3.0 to 3.6 | 3.3 | 0.9(2) | – | |
| | clock pulse width HIGH or LOW $CP_{AB}$, $CP_{BA}$ | see Figs 7 and 10 | 2.7 | 3.3 | 1.2 | – | ns |
| | | | 3.0 to 3.6 | 3.3 | 0.9(2) | – | |
| $t_{su}$ | set-up time $A_n$, $B_n$ to $CP_{AB}$, $CP_{BA}$ | see Figs 9 and 10 | 2.7 | 2.4 | 0.0 | – | ns |
| | | | 3.0 to 3.6 | +2.1 | –0.2(2) | – | |
| | set-up time $A_n$, $B_n$ to $LE_{AB}$, $LE_{BA}$ | see Figs 9 and 10 | 2.7 | +1.2 | –0.2 | – | ns |
| | | | 3.0 to 3.6 | 1.1 | 0.3(2) | – | |
| | set-up time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to $CP_{AB}$, $CP_{BA}$ | | 2.7 | +2.0 | –0.7 | – | ns |
| | | | 3.0 to 3.6 | +1.7 | –0.2(2) | – | |
| $t_h$ | hold time $A_n$, $B_n$ to $CP_{AB}$, $CP_{BA}$ | see Figs 9 and 10 | 2.7 | 1.1 | 0.3 | – | ns |
| | | | 3.0 to 3.6 | +1.0 | –0.1(2) | – | |
| | hold time $A_n$, $B_n$ to $LE_{AB}$, $LE_{BA}$ | see Figs 9 and 10 | 2.7 | 1.6 | 0.1 | – | ns |
| | | | 3.0 to 3.6 | 1.4 | 0.1(2) | – | |
| | hold time $\overline{CE}_{AB}$, $\overline{CE}_{BA}$ to $CP_{AB}$, $CP_{BA}$ | | 2.7 | 1.2 | 0.6 | – | ns |
| | | | 3.0 to 3.6 | 1.1 | 0.4(2) | – | |
| $f_{max}$ | maximum clock pulse frequency | see Figs 7 and 10 | 2.7 | 150 | 190 | – | MHz |
| | | | 3.0 to 3.6 | 150 | 240(2) | – | |

**Notes**

1. All typical values are measured at $T_{amb}$ = 25 °C.
2. Typical values at $V_{CC}$ = 3.3 V.

**AC WAVEFORMS**

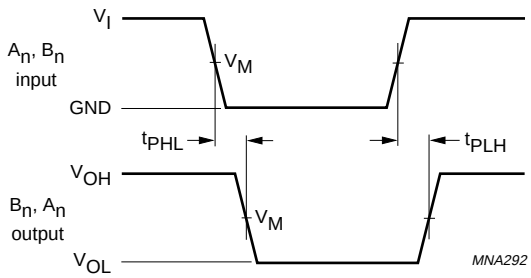



Fig.6 The input $A_n$, $B_n$ to output $B_n$, $A_n$ propagation delay times.

**Notes: $V_{CC}$ = 2.3 to 2.7 V**

$V_M = 0.5V_{CC}$;

$V_X = V_{OL} + 150$ mV;

$V_Y = V_{OH} - 150$ mV;

$V_I = V_{CC}$;

$V_{OL}$ and $V_{OH}$ are typical output voltage drop that occur with the output load.

**Notes: $V_{CC}$ = 3.0 to 3.6 V and $V_{CC}$ = 2.7 V**

$V_M = 1.5$ V;

$V_X = V_{OL} + 300$ mV;

$V_Y = V_{OH} - 300$ mV;

$V_I = 2.7$ V;

$V_{OL}$ and $V_{OH}$ are typical output voltage drop that occur with the output load.

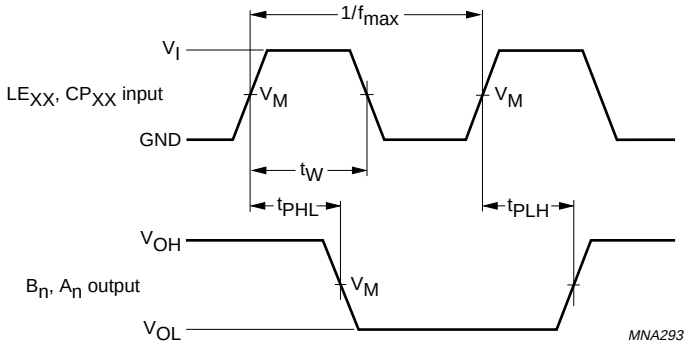



Fig.7 Latch enable input $LE_{AB}$, $LE_{BA}$ and clock input $CP_{AB}$, $CP_{BA}$ to output $B_n$, $A_n$ propagation delay times; pulse width and $f_{max}$ of $CP_{AB}$, $CP_{BA}$.

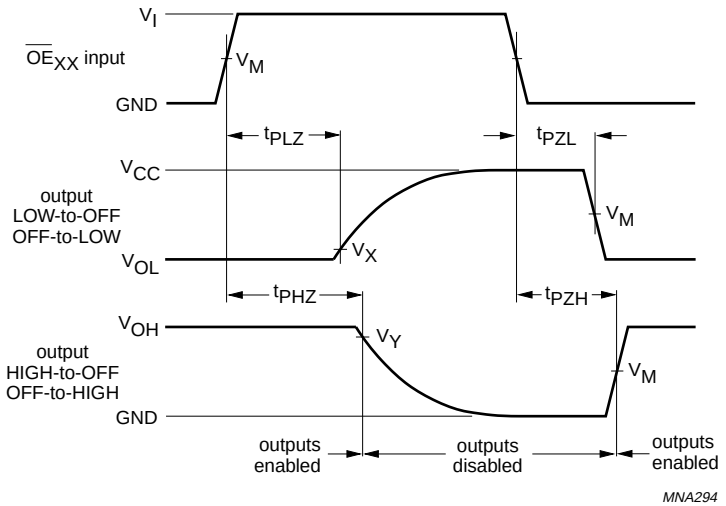
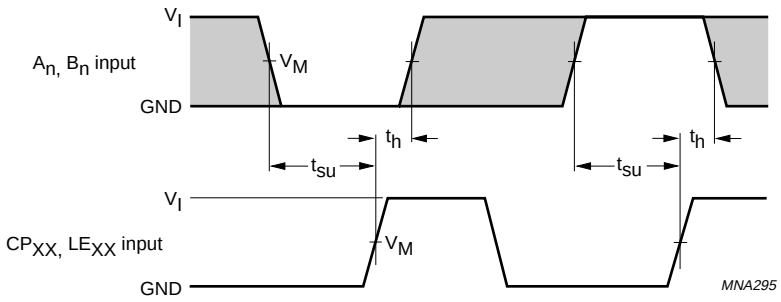
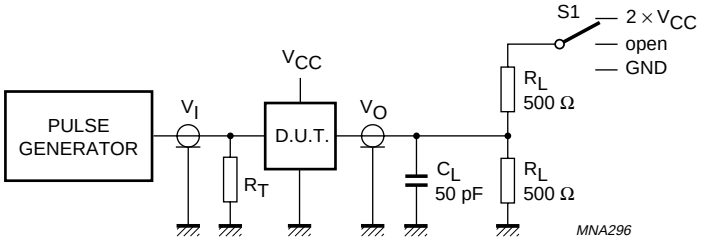



Fig.8 3-state enable and disable times.




The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.9 Data set-up and hold times for $A_n$ and $B_n$ inputs to $LE_{AB}$, $LE_{BA}$, $CP_{AB}$ or $CP_{BA}$ inputs.




| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ |
|---|---|
| <2.7 V | $V_{CC}$ |
| 2.7 to 3.6 V | 2.7 V |

Definitions for test circuit.

$C_L$ = load capacitance including jig and probe capacitance (See Chapter “AC characteristics”).

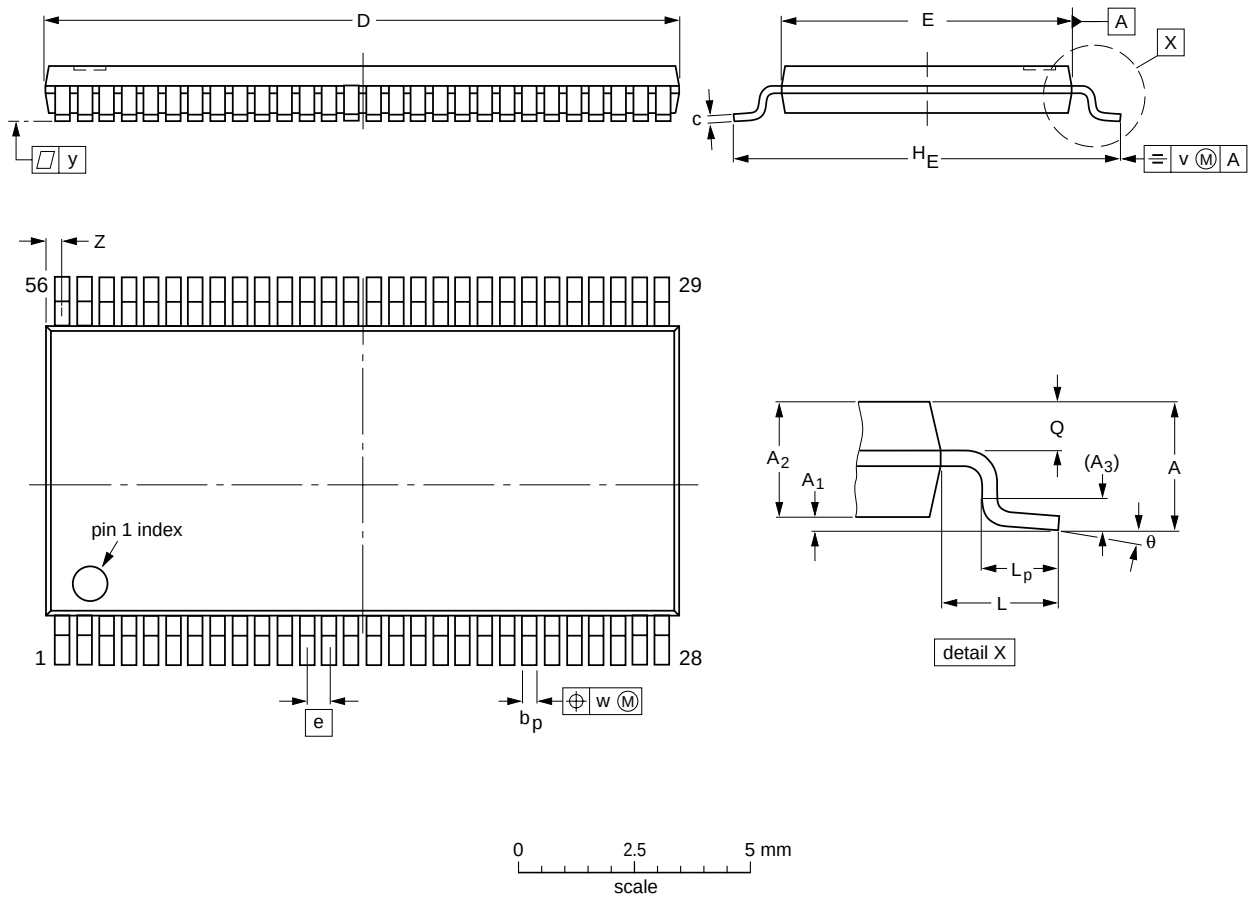
$R_L$ = load resistance.

$R_T$ = termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

Fig.10 Load circuitry for switching times.

## PACKAGE OUTLINE

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm** **SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT364-1 | | MO-153EE | | | | | ~~93-02-03~~<br>95-02-10 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
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**NOTES**

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Printed in The Netherlands 245004/01/pp20 Date of release: 1999 Oct 14 Document order number: 9397 750 05257


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Information as of 2001-04-18

# 74ALVCH162601; 18-bit universal bus transceiver with 30 Ω termination resistor; 3-state



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## Description

The 74ALVCH162601 is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ($OE_{AB}$ and $OE_{BA}$), and clock ($CP_{AB}$ and $CP_{BA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when $LE_{AB}$ is HIGH. When $LE_{AB}$ is LOW, the A data is latched if $CP_{AB}$ is held at a HIGH or LOW logic level. If $LE_{AB}$ is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of $CP_{AB}$. When $OE_{AB}$ is LOW, the outputs are active. When $OE_{AB}$ is HIGH, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ($CE_{BA}$ /$CE_{AB}$ ).

Data flow for B-to-A is similar to that of A-to-B but uses $OE_{BA}$ ,$LE_{BA}$ and $CP_{BA}$.

To ensure the high-impedance state during power-down, $OE_{BA}$ and $OE_{AB}$ should be tied to $V_{CC}$ through a pull-up resistor, the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The 74ALVCH162601 is designed with 30 Ω series resistors in both HIGH or LOW output stage.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## Features

- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and ground pins for minimum noise and ground bounce
- All data inputs have bus hold circuitry
- Integrated 30 Ω termination resistors.

## Datasheet

| Type nr. | Title | Publication release date | Datasheet status | Page count | File size (kB) | Datasheet |
|---|---|---|---|---|---|---|
| 74ALVCH162601 | 18-bit universal bus transceiver with 30 Ω termination resistor; 3-state | 14-Oct-99 | Product Specification | 20 | 98 | Download |

## Products, packages, availability and ordering

| Partnumber | North American Partnumber | Order code (12nc) | marking/packing IC packing info | package | device status | buy online |
|---|---|---|---|---|---|---|
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