TC74HC237P/F

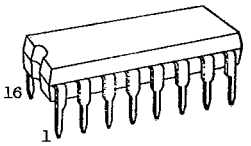
T-67-21-55

TC74HC237P/F 3-TO-8 LINE DECODER/LATCH

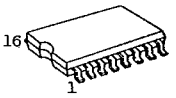
The TC74HC237 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go high. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Inverting type of the 74HC137



DIP16(3D16A-P)



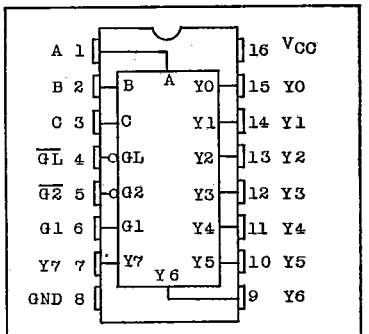
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



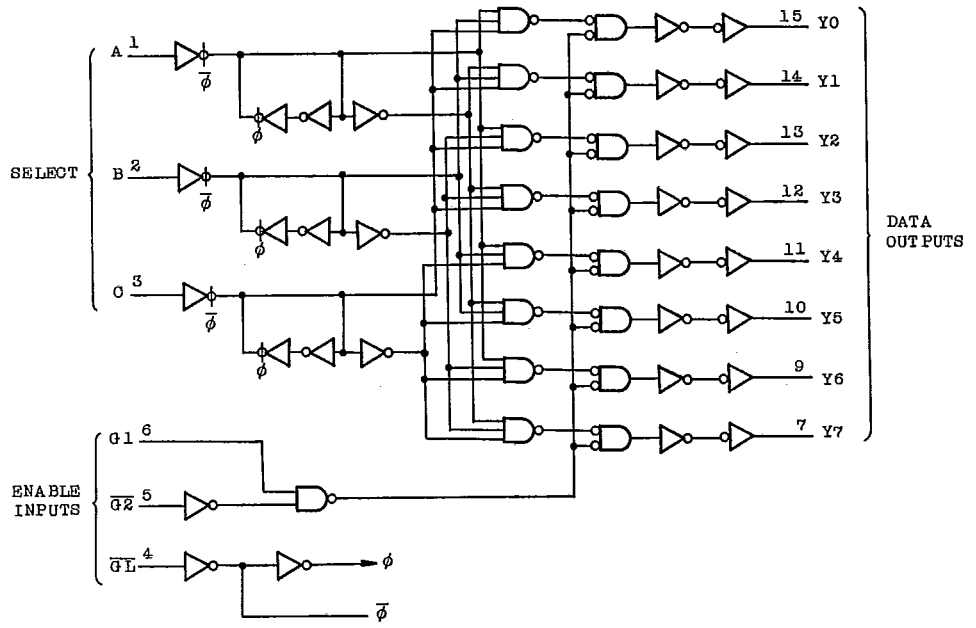
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H ; ALL OTHERS, L							

X : DON'T CARE

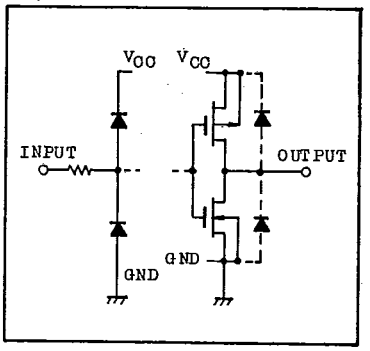
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

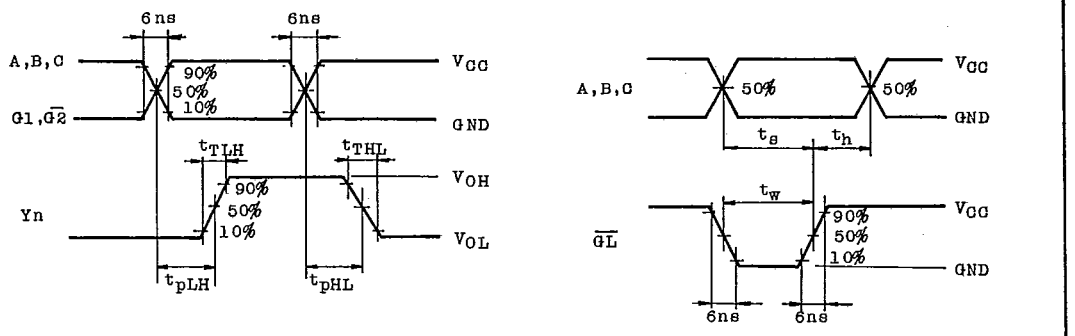
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{GL}$ - Y)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		2.0	-	12	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

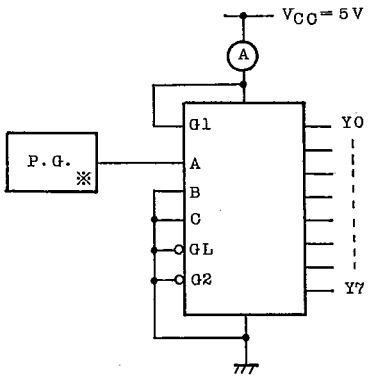
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

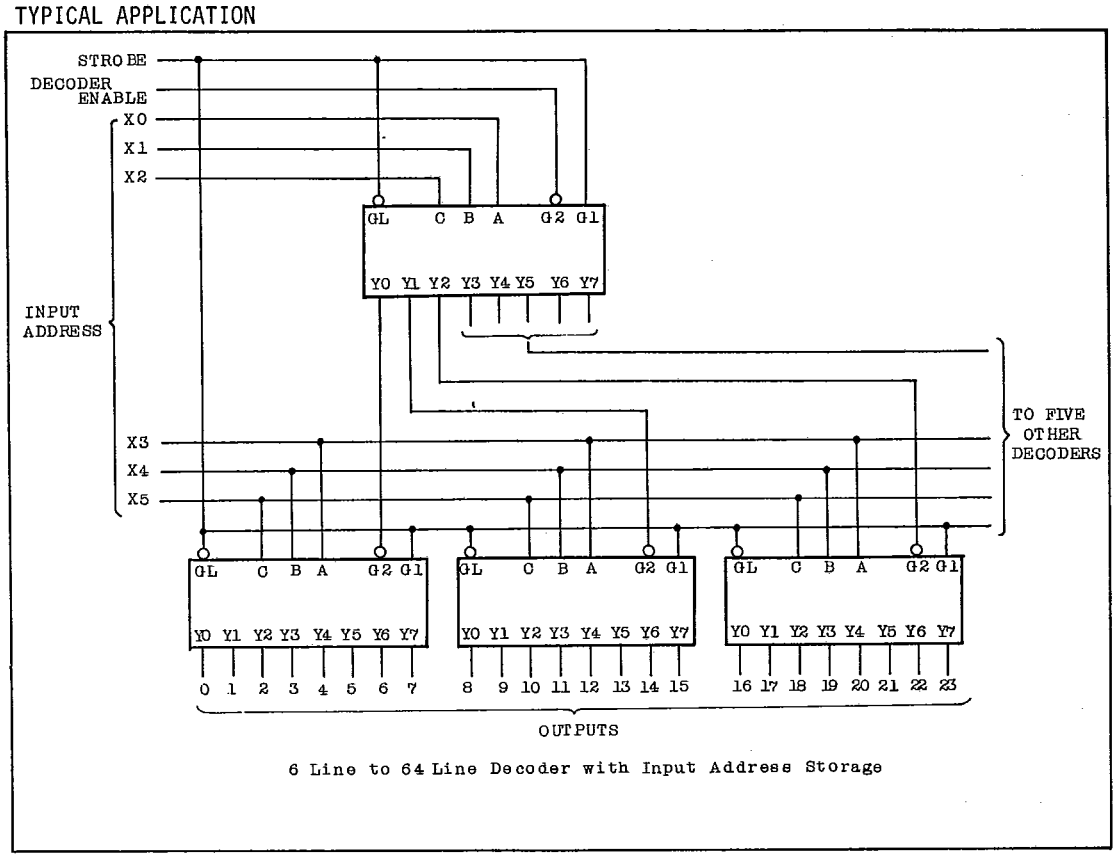


I_{CC}(Opr.) TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage