

Octal Bus Buffer

TC74LVQ240 Inverted, 3-State Outputs

TC74LVQ241 Non-Inverted, 3-State Outputs

TC74LVQ244 Non-Inverted, 3-State Outputs

The TC74LVQ240, 241 and 244 are high speed CMOS OCTAL BUS BUFFERS fabricated with silicon gate and double-layer metal wiring C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

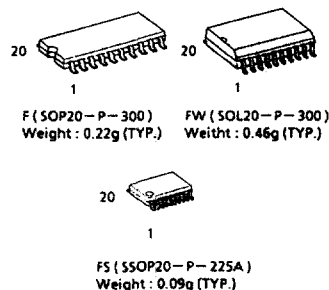
The TC74LVQ240 is an inverting 3-state buffer having two active-low output enables. The TC74LVQ241 and TC74LVQ244 are non-inverting 3-state buffers that differ only in that the LVQ241 has one active-high and one active-low output enable, and the LVQ244 has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: $t_{pd} = 5.4\text{ns}$ (Typ.) at $V_{CC} = 3.3\text{V}$
- Low Power Dissipation: $I_{CC} = 4\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Input Voltage Level:
 - $V_{IL} = 0.8\text{V}$ (Max.) at $V_{CC} = 3\text{V}$
 - $V_{IH} = 2.0\text{V}$ (Min.) at $V_{CC} = 3\text{V}$
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL} = 12\text{mA}$ (Min.)
- Balanced Propagation Delays: $t_{PLH} \approx t_{PHL}$
- Pin and Function Compatible with 74HC240/241/244



Truth Table

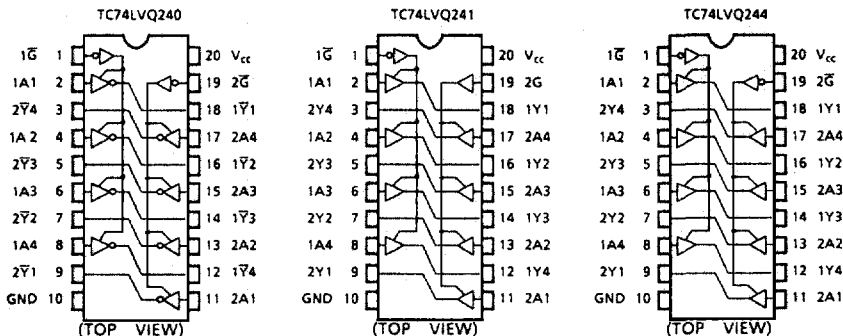
Inputs	\bar{G}	$G\Delta$	A_n	Outputs	Y_n	$\bar{Y}_n\Delta\Delta$
L	H	L	L	L	H	
L	H	H	H	H	L	
H	L	X	Z	Z	Z	

Δ : for TC74LVQ241 only

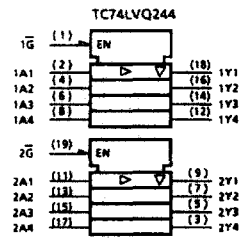
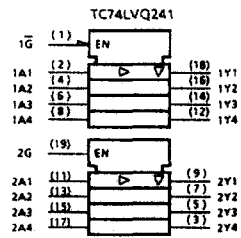
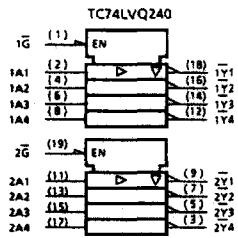
$\Delta\Delta$: for TC74LVQ240 only

x: Don't Care

z: High Impedance



Pin Assignment



IEC Logic Symbol

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V _{CC}	-0.5 - 7.0	V
DC Input Voltage	V _{IN}	-0.5 - V _{CC} + 0.5	V
DC Output Voltage	V _{OUT}	-0.5 - V _{CC} + 0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±50	mA
DC Output Current	I _{OUT}	±50	mA
DC V _{CC} /Ground Current	I _{CC}	±200	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65 - 150	°C
Lead Temperature 10sec	T _L	300	°C

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V _{CC}	2.0 - 3.6	V
Input Voltage	V _{IN}	0 - V _{CC}	V
Output Voltage	V _{OUT}	0 - V _{CC}	V
Operating Temperature	T _{opr}	-40 - 85	°C
Input Rise and Fall Time	dt/dv	0 - 100	ns/V

DC Electrical Characteristics

Parameter	Symbol	Test Condition	T _a = 25°C			T _a = -40 ~ 85°C		Unit	
			V _{CC} (V)	Min	Typ.	Max.	Min.		Max.
High-Level Input Voltage	V _{IH}		3.0	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V _{IL}		3.0	-	-	0.8	-	0.8	
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL} I _{OH} = -50µA I _{OH} = -12mA	3.0	2.9	3.0	-	2.9	-	
			3.0	2.58	-	-	2.48	-	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50µA I _{OL} = 12mA	3.0	-	0.0	0.1	-	0.1	
			3.0	-	-	0.36	-	0.44	
3-State Output Off-State Current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	3.6	-	-	±0.5	-	±5.0	µA
Input Leakage Current	I _{IN}	V _{IN} = V _{CC} or GND	3.6	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	3.6	-	-	4.0	-	40.0	

AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	V _{CC} (V)	Ta = 25°C			Ta = -40 ~ 85°C		Unit
				Min	Typ.	Max.	Min.	Max.	
Propagation Delay Time (TC74LVQ240)	t_{pLH} t_{pHL}		2.7	–	7.2	14.1	1.0	15.0	ns
			3.3±0.3	–	6.0	10.0	1.0	10.5	
Propagation Delay Time (TC74LVQ241/244)	t_{pLH} t_{pHL}		2.7	–	7.8	13.4	1.0	15.0	
			3.3±0.3	–	6.5	9.5	1.0	10.5	
Output Enable Time	t_{pZL} t_{pZH}		2.7	–	9.5	18.3	1.0	19.0	
			3.3±0.3	–	7.9	13.0	1.0	13.5	
Output Disable Time	t_{pLZ} t_{pHZ}		2.7	–	7.2	19.0	1.0	20.0	
			3.3±0.3	–	6.0	13.5	1.0	14.0	
Output to Output Skew	$t_{oS LH}$ $t_{oS HL}$	(Note 1)	2.7	–	–	1.5	–	1.5	
			3.3±0.3	–	–	1.5	–	1.5	
Input Capacitance	C _{IN}	(Note 2)		–	5	10	–	10	pF
Output Capacitance	C _{OUT}			–	10	–	–	–	
Power Dissipation Capacitance	C _{PD}	(Note 3)		–	30	–	–	–	

Note (1) Parameter guaranteed by design. $t_{oS LH} = |t_{pLHm} - t_{pLHn}|$, $t_{oS HL} = |t_{pHLm} - t_{pHLn}|$

Note (2) Parameter guaranteed by design.

Note (3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{op}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

Noise Characteristics (Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$)

Parameter	Symbol	Test Condition	V _{CC}	Ta = 25°C		Unit
				Typ.	Max.	
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	–	3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	–	3.3	-0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	–	3.3	–	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	–	3.3	–	0.8	V

1. This technical data may be controlled under U.S. Export Administration Regulations and may be subject to the approval of the U.S. Department of Commerce prior to export. Any export or re-export, directly or indirectly, in contravention of the U.S. Export Administration Regulations is strictly prohibited.

2. LIFE SUPPORT POLICY

Toshiba products described in this document are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

A critical component in any component of a life support system whose failure to perform may cause a malfunction of the life support system, or may affect its safety or effectiveness.

3. The information in this document has been carefully checked and is believed to be reliable; however no responsibility can be assumed for inaccuracies that may not have been caught. All information in this data book is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.