TC74AC175
Quad D-Type Flip Flop with Clear

Features:

- **High Speed:** f_{max} = 170MHz (typ.) at V_{CC} = 5V
- **Low Power Dissipation:** I_{CC} = 8μA (max.) at Ta = 25°C
- **High Noise Immunity:** $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min.)
- **Symmetrical Output Impedance:** $|I_{OH}| = I_{OL}$ = 24mA (min.). Capability of driving 50Ω transmission lines.
- **Balanced Propagation Delays:** $t_{pLH} = t_{pHL}$
- **Wide Operating Voltage Range:** V_{CC}(opr) = 2V~5.5V
- **Pin and Function Compatible with 74F175**
- **Available in 16-pin DIP and 150 mil SOIC**

The TC74AC175 is an advanced high speed CMOS QUAD D-TYPE FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

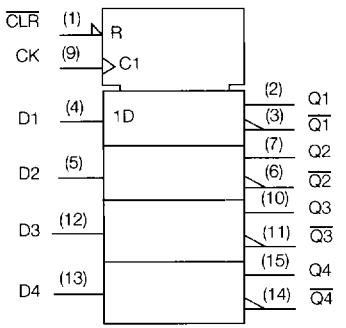
These four flip-flops are controlled by a clock input (CLOCK) and a clear input ($\overline{CLEAR}$).

The information data applied to the D inputs (1D thru 4D) are transferred to the outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$) on the positive going edge of the clock pulse.

Reset is accomplished when the clear input is taken low; all Q outputs are held low regardless of other input conditions.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

IEC Logic Symbol

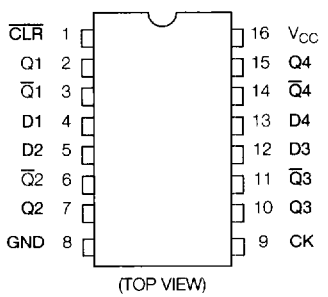


Truth Table

INPUTS			OUTPUTS		FUNCTION
$\overline{CLR}$	D	CK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	H	—
H	X	↓	Qn	$\overline{Q}$n	NO CHANGE

X : Don't Care

Pin Assignment



(TOP VIEW)

Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500 (DIP) */180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta = -40°C~65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C should be applied up to 300mW.

Recommended Operating Conditions

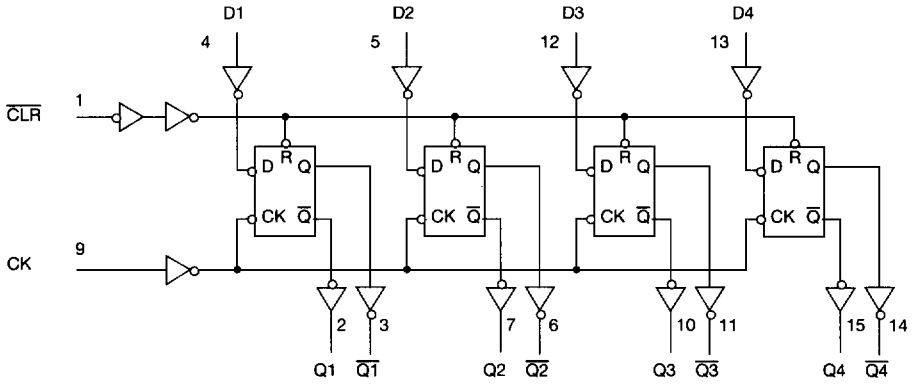
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns/v

DC Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40~85°C Min.	Ta = -40~85°C Max.	UNIT
High-Level Input Voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				3.0	2.10	—	—	2.10	—	
				5.5	3.85	—	—	3.85	—	
Low-Level Input Voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				3.0	—	—	0.90	—	0.90	
				5.5	—	—	1.65	—	1.65	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = -4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = -24mA	4.5	3.94	—	—	3.80	—	
			I_{OH} = -75mA*	5.5	—	—	—	3.85	—	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 12mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 24mA	4.5	—	—	0.36	—	0.44	
			I_{OL} = 75mA*	5.5	—	—	—	—	1.65	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	8.0	—	80.0	

* This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

System Diagram



Timing Requirements (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = -40~85°C	UNIT
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	—	3.3±0.3	—	7.0	7.0	ns
			5.0±0.5	—	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$	—	3.3±0.3	—	7.0	7.0	
			5.0±0.5	—	5.0	5.0	
Minimum Set-up Time	t_s	—	3.3±0.3	—	12.0	12.0	
			5.0±0.5	—	6.5	6.5	
Minimum Hold Time	t_h	—	3.3±0.3	—	0.0	0.0	
			5.0±0.5	—	0.0	0.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}	—	3.3±0.3	—	7.0	7.0	
			5.0±0.5	—	5.0	5.0	

AC Electrical Characteristics (C_L = 50pF, R_L = 500Ω, Input $t_r = t_f$ = 3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = -40~85°C		UNIT
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Propagation Delay Time (CK–Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	3.3±0.3	—	8.2	13.9	1.0	16.0	ns
			5.0±0.5	—	6.1	8.7	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$–Q, $\overline{Q}$)	t_{pLH}	—	3.3±0.3	—	7.8	13.3	1.0	15.3	
			5.0±0.5	—	6.1	8.7	1.0	10.0	
Maximum Clock Frequency	f_{MAX}	—	3.3±0.3	40	80	—	40	—	MHz
			5.0±0.5	80	150	—	80	—	
Input Capacitance	C_{IN}	—	—	—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)	—	—	—	85	—	—	—	

Note (1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation: $I_{CC\ (opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}/4$ (per bit).
And the total C_{PD} when n pcs of Flip-Flop operate can be gained by the following equation: C_{PD} (total)=35+50 • n.