

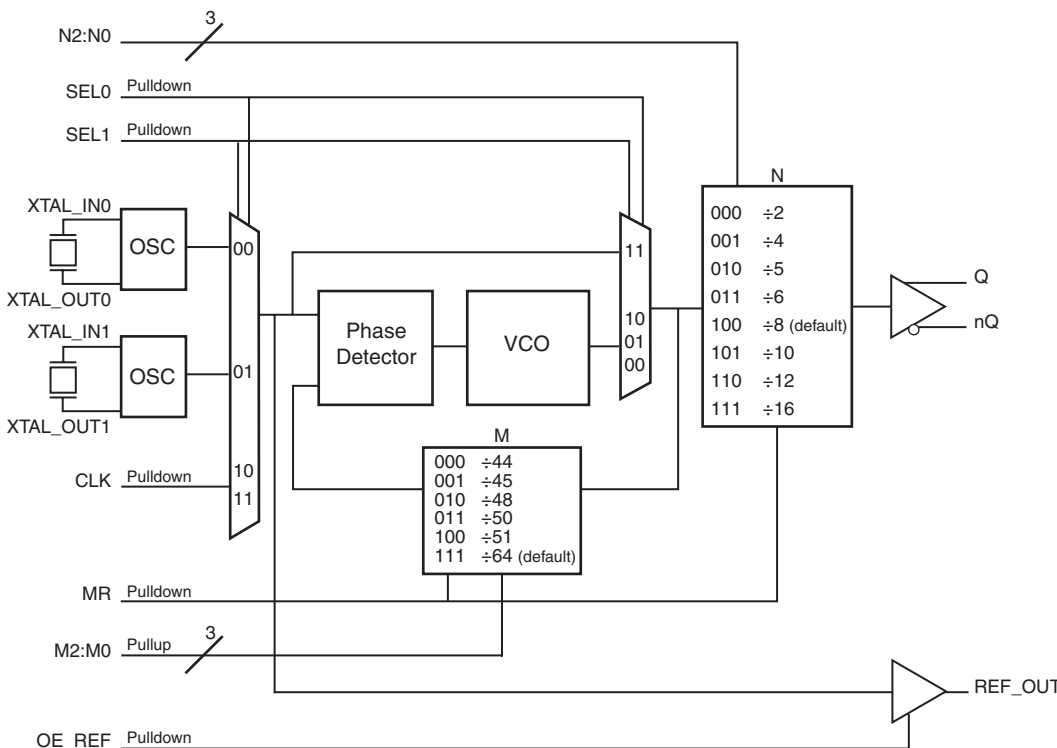
### General Description

The ICS843001I-23 is a highly versatile, low phase noise LVPECL/LVCMOS Synthesizer which can generate low jitter reference clocks for a variety of communication applications. The dual crystal interface allows the synthesizer to support up to three communication standards in a given application (i.e. SONET with a 19.44MHz crystal, 1Gb/10Gb Ethernet and Fibre Channel using a 25MHz crystal). The RMS phase jitter performance is typically less than 1ps, thus making the device acceptable for use in demanding applications such as OC48 SONET, GbE/10Gb Ethernet and SAN applications. The ICS843001I-23 is packaged in a small 24-pin TSSOP, E-Pad package.

### Features

- One 3.3V differential LVPECL output pair and one LVCMOS/LVTTL single-ended reference clock output
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- Crystal and CLK range: 19.44MHz – 27MHz
- Able to generate GbE/10GbE/12GbE, Fibre Channel (1Gb/4Gb/10Gb), PCI-E and SATA from a 25MHz crystal
- VCO range: 1.12GHz – 1.275GHz
- Supports the following applications: SONET, Ethernet, Fibre Channel, Serial ATA, and HDTV
- RMS phase jitter @ 622.08MHz (12kHz - 20MHz): 0.9ps (typical), 3.3V
- Supply modes  
 $V_{CC}/V_{CCO}$   
 3.3V/3.3V  
 3.3V/2.5V  
 2.5V/2.5V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) package

### Block Diagram



### Pin Assignment

|                   |    |    |           |
|-------------------|----|----|-----------|
| $V_{CCO\_LVCMOS}$ | 1  | 24 | REF_OUT   |
| N0                | 2  | 23 | VEE       |
| N1                | 3  | 22 | OE_REF    |
| N2                | 4  | 21 | M2        |
| $V_{CCO\_LVPECL}$ | 5  | 20 | M1        |
| Q                 | 6  | 19 | M0        |
| nQ                | 7  | 18 | MR        |
| VEE               | 8  | 17 | SEL1      |
| VCCA              | 9  | 16 | SEL0      |
| VCC               | 10 | 15 | CLK       |
| XTAL_OUT1         | 11 | 14 | XTAL_IN0  |
| XTAL_IN1          | 12 | 13 | XTAL_OUT0 |

### ICS843001I-23

**24-Lead TSSOP, E-Pad**  
**4.4mm x 7.8mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

| Number     | Name                    | Type   |          | Description   |
|------------|-------------------------|--------|----------|---|
| 1          | V <sub>CCO_LVCMOS</sub> | Power  |          | Output supply pin for REF_CLK output.   |
| 2, 3       | N0, N1                  | Input  | Pulldown | Output divider select pins. LVCMOS/LVTTL interface levels. See Table 3C.  |
| 4          | N2                      | Input  | Pullup   |   |
| 5          | V <sub>CCO_LVPECL</sub> | Power  |          | Output supply pin for LVPECL output.  |
| 6, 7       | Q, nQ                   | Output |          | Differential output pair. LVPECL interface levels.  |
| 8, 23      | V <sub>EE</sub>         | Power  |          | Negative supply pins.   |
| 9          | V <sub>CCA</sub>        | Power  |          | Analog supply pin.  |
| 10         | V <sub>CC</sub>         | Power  |          | Core supply pin.  |
| 11, 12     | XTAL_OUT1, XTAL_IN1     | Input  |          | Parallel resonant crystal interface. XTAL_OUT1 is the output, XTAL_IN1 is the input.  |
| 13, 14     | XTAL_OUT0, XTAL_IN0     | Input  |          | Parallel resonant crystal interface. XTAL_OUT0 is the output, XTAL_IN0 is the input.  |
| 15         | CLK                     | Input  | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels.  |
| 16, 17     | SEL0, SEL1              | Input  | Pulldown | Input MUX select pins. LVCMOS/LVTTL interface levels. See Table 3D.   |
| 18         | MR                      | Input  | Pulldown | Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. |
| 19, 20, 21 | M0, M1, M2              | Input  | Pullup   | Feedback divider select pins. LVCMOS/LVTTL interface levels. See Table 3B.  |
| 22         | OE_REF                  | Input  | Pulldown | Reference clock output enable. Default LOW. See Table 3E. LVCMOS/LVTTL interface levels.  |
| 24         | REF_OUT                 | Output |          | Reference clock output. LVCMOS/LVTTL interface levels.  |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum                 | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|-------------------------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |                         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |                         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |                         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance        | REF_OUT         | V <sub>CCO</sub> = 3.3V | 21      |         | Ω     |
|                       |                         |                 | V <sub>CCO</sub> = 2.5V | 25      |         | Ω     |

## Function Tables

**Table 3A. Common Configuration Table**

| Input Frequency (MHz) | M Feedback Divider Value | VCO Frequency (MHz) | N Output Divider Value | Output Frequency (MHz) | Application          |
|-----------------------|--------------------------|---------------------|------------------------|------------------------|----------------------|
| 27                    | 44                       | 1188                | 16                     | 74.25                  | HDTV                 |
| 24.75                 | 48                       | 1188                | 16                     | 74.25                  | HDTV                 |
| 19.44                 | 64                       | 1244.16             | 8                      | 155.52                 | SONET                |
| 19.44                 | 64                       | 1244.16             | 2                      | 622.08                 | SONET                |
| 19.44                 | 64                       | 1244.16             | 4                      | 311.04                 | SONET                |
| 25                    | 50                       | 1250                | 10                     | 125                    | GigE                 |
| 25                    | 50                       | 1250                | 8                      | 156.25                 | 10 GigE              |
| 25                    | 50                       | 1250                | 5                      | 250                    | GigE                 |
| 25                    | 50                       | 1250                | 4                      | 312.5                  | XGMII                |
| 25                    | 50                       | 1250                | 2                      | 625                    | 10 GigE              |
| 25                    | 45                       | 1125                | 6                      | 187.5                  | 12 GigE              |
| 25                    | 48                       | 1200                | 12                     | 100                    | PCI Express          |
| 25                    | 48                       | 1200                | 8                      | 150                    | SATA                 |
| 25                    | 48                       | 1200                | 16                     | 75                     | SATA                 |
| 25                    | 51                       | 1275                | 12                     | 106.25                 | Fibre Channel        |
| 25                    | 51                       | 1275                | 8                      | 159.375                | 10 Gig Fibre Channel |
| 25                    | 51                       | 1275                | 6                      | 212.5                  | 4 Gig Fibre Channel  |

**Table 3B. Programmable M Feedback Divider Function Table**

| Inputs |    |    | M Feedback Divider Value | Input Frequency (MHz) |         |
|--------|----|----|--------------------------|-----------------------|---------|
| M2     | M1 | M0 |                          | Minimum               | Maximum |
| 0      | 0  | 0  | 44                       | 25.5                  | 27      |
| 0      | 0  | 1  | 45                       | 24.9                  | 27      |
| 0      | 1  | 0  | 48                       | 23.3                  | 26.56   |
| 0      | 1  | 1  | 50                       | 22.4                  | 25.5    |
| 1      | 0  | 0  | 51                       | 22.0                  | 25      |
| 1      | 0  | 1  | 64 (default)             | 19.44                 | 19.92   |

**Table 3C. Programmable N Output Divider Function Table**

| Inputs |    |    | N Divider Value |
|--------|----|----|-----------------|
| N2     | N1 | N0 |                 |
| 0      | 0  | 0  | 2               |
| 0      | 0  | 1  | 4               |
| 0      | 1  | 0  | 5               |
| 0      | 1  | 1  | 6               |
| 1      | 0  | 0  | 8 (default)     |
| 1      | 0  | 1  | 10              |
| 1      | 1  | 0  | 12              |
| 1      | 1  | 1  | 16              |

**Table 3D. Select Mode Function Table**

| Inputs |      | Reference Input | PLL Mode         |
|--------|------|-----------------|------------------|
| SEL1   | SEL0 |                 |                  |
| 0      | 0    | XTAL0           | Active (default) |
| 0      | 1    | XTAL1           | Active           |
| 1      | 0    | CLK             | Active           |
| 1      | 1    | CLK             | Bypass           |

**Table 3E. OE\_REF Output Function Table**

| Input         | Output                   |
|---------------|--------------------------|
| <b>OE_REF</b> | <b>REF_OUT</b>           |
| 0             | High-Impedance (default) |
| 1             | Active                   |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                                     |
|--|--|
| Supply Voltage, $V_{CC}$                                       | 4.6V                                       |
| Inputs, $V_I$<br>XTAL_IN<br>Other Input                        | 0V to $V_{CC}$<br>-0.5V to $V_{CC} + 0.5V$ |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | 50mA<br>100mA                              |
| Outputs, $V_O$ (LVCMOS)  | -0.5V to $V_{CCO\_LVCMOS} + 0.5V$          |
| Package Thermal Impedance, $\theta_{JA}$                       | 32.1°C/W (0 mps)                           |
| Storage Temperature, $T_{STG}$                                 | -65°C to 150°C                             |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol                                   | Parameter             | Test Conditions      | Minimum         | Typical | Maximum  | Units |
|--|-----------------------|----------------------|-----------------|---------|----------|-------|
| $V_{CC}$                                 | Core Supply Voltage   |                      | 3.135           | 3.3     | 3.465    | V     |
| $V_{CCA}$                                | Analog Supply Voltage |                      | $V_{CC} - 0.11$ | 3.3     | $V_{CC}$ | V     |
| $V_{CCO\_LVPECL}$ ,<br>$V_{CCO\_LVCMOS}$ | Output Supply Voltage |                      | 3.135           | 3.3     | 3.465    | V     |
| $I_{EE}$                                 | Power Supply Current  |                      |                 |         | 140      | mA    |
| $I_{CCA}$                                | Analog Supply Current | Outputs Unterminated |                 |         | 11       | mA    |

**Table 4B. Power Supply DC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

| Symbol                                   | Parameter             | Test Conditions      | Minimum         | Typical | Maximum  | Units |
|--|-----------------------|----------------------|-----------------|---------|----------|-------|
| $V_{CC}$                                 | Core Supply Voltage   |                      | 3.135           | 3.3     | 3.465    | V     |
| $V_{CCA}$                                | Analog Supply Voltage |                      | $V_{CC} - 0.11$ | 3.3     | $V_{CC}$ | V     |
| $V_{CCO\_LVPECL}$ ,<br>$V_{CCO\_LVCMOS}$ | Output Supply Voltage |                      | 2.375           | 2.5     | 2.625    | V     |
| $I_{EE}$                                 | Power Supply Current  |                      |                 |         | 139      | mA    |
| $I_{CCA}$                                | Analog Supply Current | Outputs Unterminated |                 |         | 11       | mA    |

**Table 4C. Power Supply DC Characteristics,  $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol                               | Parameter             | Test Conditions      | Minimum         | Typical | Maximum  | Units |
|--------------------------------------|-----------------------|----------------------|-----------------|---------|----------|-------|
| $V_{CC}$                             | Core Supply Voltage   |                      | 2.375           | 2.5     | 2.625    | V     |
| $V_{CCA}$                            | Analog Supply Voltage |                      | $V_{CC} - 0.10$ | 2.5     | $V_{CC}$ | V     |
| $V_{CCO\_PECL}$ ,<br>$V_{CCO\_CMOS}$ | Output Supply Voltage |                      | 2.375           | 2.5     | 2.625    | V     |
| $I_{EE}$                             | Power Supply Current  |                      |                 |         | 133      | mA    |
| $I_{CCA}$                            | Analog Supply Current | Outputs Unterminated |                 |         | 10       | mA    |

**Table 4D. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol   | Parameter           | Test Conditions  | Minimum | Typical | Maximum        | Units   |
|----------|---------------------|--|---------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage  | $V_{CC} = 3.3V$  | 2       |         | $V_{CC} + 0.3$ | V       |
|          |                     | $V_{CC} = 2.5V$  | 1.7     |         | $V_{CC} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage   | $V_{CC} = 3.3V$  | -0.3    |         | 0.8            | V       |
|          |                     | $V_{CC} = 2.5V$  | -0.3    |         | 0.7            | V       |
| $I_{IH}$ | Input High Current  | CLK, OE_REF, MR, N0, N1 SEL0, SEL1<br>$V_{CC} = V_{IN} = 3.465V$ or $2.625V$           |         |         | 150            | $\mu A$ |
|          |                     | N2, M[2:0]<br>$V_{CC} = V_{IN} = 3.465V$ or $2.625V$                                   |         |         | 5              | $\mu A$ |
| $I_{IL}$ | Input Low Current   | CLK, OE_REF, MR, N0, N1 SEL0, SEL1<br>$V_{CC} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$ | -5      |         |                | $\mu A$ |
|          |                     | N2, M[2:0]<br>$V_{CC} = 3.465V$ or $2.625V$ ,<br>$V_{IN} = 0V$                         | -150    |         |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage | REF_OUT<br>$V_{CCO\_LVCMOS} = 3.465V$ ,<br>$I_{OH} = -12mA$                            | 2.6     |         |                | V       |
|          |                     | $V_{CCO\_LVCMOS} = 2.625V$ ,<br>$I_{OH} = -12mA$                                       | 1.8     |         |                | V       |
| $V_{OL}$ | Output Low Voltage  | REF_OUT<br>$V_{CCO\_LVCMOS} = 3.465V$ or $2.625V$ ,<br>$I_{OL} = 12mA$                 |         |         | 0.5            | V       |

**Table 4E. LVPECL DC Characteristics,  $V_{CC} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum                 | Typical | Maximum                 | Units |
|-------------|-----------------------------------|-----------------|-------------------------|---------|-------------------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO\_LVPECL} - 1.4$ |         | $V_{CCO\_LVPECL} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO\_LVPECL} - 2.0$ |         | $V_{CCO\_LVPECL} - 1.7$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.6                     |         | 1.0                     | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO\_LVPECL} - 2V$ .

**Table 4F. LVPECL DC Characteristics**,  $V_{CC} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $V_{CCO\_LVPECL} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol      | Parameter                         | Test Conditions | Minimum                 | Typical | Maximum                 | Units |
|-------------|-----------------------------------|-----------------|-------------------------|---------|-------------------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       |                 | $V_{CCO\_LVPECL} - 1.4$ |         | $V_{CCO\_LVPECL} - 0.9$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        |                 | $V_{CCO\_LVPECL} - 2.0$ |         | $V_{CCO\_LVPECL} - 1.5$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing |                 | 0.4                     |         | 1.0                     | V     |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO\_LVPECL} - 2V$ .**Table 5. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 19.44       |         | 27      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 6A. AC Characteristics**,  $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ 

| Symbol               | Parameter                          | Test Conditions            | Minimum           | Typical | Maximum | Units |    |
|----------------------|------------------------------------|----------------------------|-------------------|---------|---------|-------|----|
| $f_{OUT}$            | Output Frequency                   | Q, nQ                      | 70                |         | 637.5   | MHz   |    |
|                      |                                    | REF_OUT                    | 19.44             |         | 27      | MHz   |    |
| $t_{PD}$             | Propagation Delay; NOTE 1          | CLK to REF_OUT             | 2.2               |         | 2.7     | ns    |    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random); NOTE 2 | 622.08MHz, (12kHz – 20MHz) |                   | 0.97    |         | ps    |    |
| $f_{VCO}$            | PLL VCO Lock Range                 |                            | 1.12              |         | 1.275   | GHz   |    |
| $t_R / t_F$          | Output Rise/Fall Time              | Q, nQ                      | 20% to 80%        | 200     |         | 700   | ps |
|                      |                                    | REF_OUT, NOTE 3            | 20% to 80%        | 250     |         | 650   | ps |
| odc                  | Output Duty Cycle                  | Q, nQ                      |                   | 46      |         | 54    | %  |
|                      |                                    | REF_OUT; NOTE 3            | Using Clock Input | 48      |         | 52    | %  |
| $t_{LOCK}$           | PLL Lock Time                      |                            |                   |         | 60      | ms    |    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{CC}/2$  of the input to  $V_{CCO\_LVCMOS}/2$  of the output.

NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.

NOTE 3: REF\_OUT output duty cycle characterized with CLK input duty cycle between 48% and 52%.

**Table 6B. AC Characteristics,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol               | Parameter                             | Test Conditions               | Minimum           | Typical | Maximum | Units |
|----------------------|---------------------------------------|-------------------------------|-------------------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                      | Q, nQ                         | 70                |         | 637.5   | MHz   |
|                      |                                       | REF_OUT                       | 19.44             |         | 27      | MHz   |
| $t_{PD}$             | Propagation Delay;<br>NOTE 1          | CLK to<br>REF_OUT             | 2.3               |         | 2.9     | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random);<br>NOTE 2 | 622.08MHz,<br>(12kHz – 20MHz) |                   | 1       |         | ps    |
| $f_{VCO}$            | PLL VCO Lock Range                    |                               | 1.12              |         | 1.275   | GHz   |
| $t_R / t_F$          | Output<br>Rise/Fall Time              | Q, nQ                         | 20% to 80%        | 200     | 700     | ps    |
|                      |                                       | REF_OUT                       | 20% to 80%        | 350     | 750     | ps    |
| odc                  | Output Duty Cycle                     | Q, nQ                         |                   | 46      | 54      | %     |
|                      |                                       | REF_OUT;<br>NOTE 3            | Using Clock Input | 48      | 52      | %     |
| $t_{LOCK}$           | PLL Lock Time                         |                               |                   |         | 60      | ms    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from the  $V_{CC}/2$  of the input to  $V_{CCO\_LVCMOS}/2$  of the output.

NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.

NOTE 3: REF\_OUT output duty cycle characterized with CLK input duty cycle between 48% and 52%.

**Table 6C. AC Characteristics,  $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol               | Parameter                             | Test Conditions               | Minimum           | Typical | Maximum | Units |
|----------------------|---------------------------------------|-------------------------------|-------------------|---------|---------|-------|
| $f_{OUT}$            | Output Frequency                      | Q, nQ                         | 70                |         | 637.5   | MHz   |
|                      |                                       | REF_OUT                       | 19.44             |         | 27      | MHz   |
| $t_{PD}$             | Propagation Delay;<br>NOTE 1          | CLK to<br>REF_OUT             | 2.3               |         | 2.9     | ns    |
| $f_{jit}(\emptyset)$ | RMS Phase Jitter, (Random);<br>NOTE 2 | 622.08MHz,<br>(12kHz – 20MHz) |                   | 1.1     |         | ps    |
| $f_{VCO}$            | PLL VCO Lock Range                    |                               | 1.12              |         | 1.275   | GHz   |
| $t_R / t_F$          | Output<br>Rise/Fall Time              | Q, nQ                         | 20% to 80%        | 200     | 700     | ps    |
|                      |                                       | REF_OUT                       | 20% to 80%        | 350     | 750     | ps    |
| odc                  | Output Duty Cycle                     | Q, nQ                         |                   | 46      | 54      | %     |
|                      |                                       | REF_OUT;<br>NOTE 3            | Using Clock Input | 48      | 52      | %     |
| $t_{LOCK}$           | PLL Lock Time                         |                               |                   |         | 60      | ms    |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

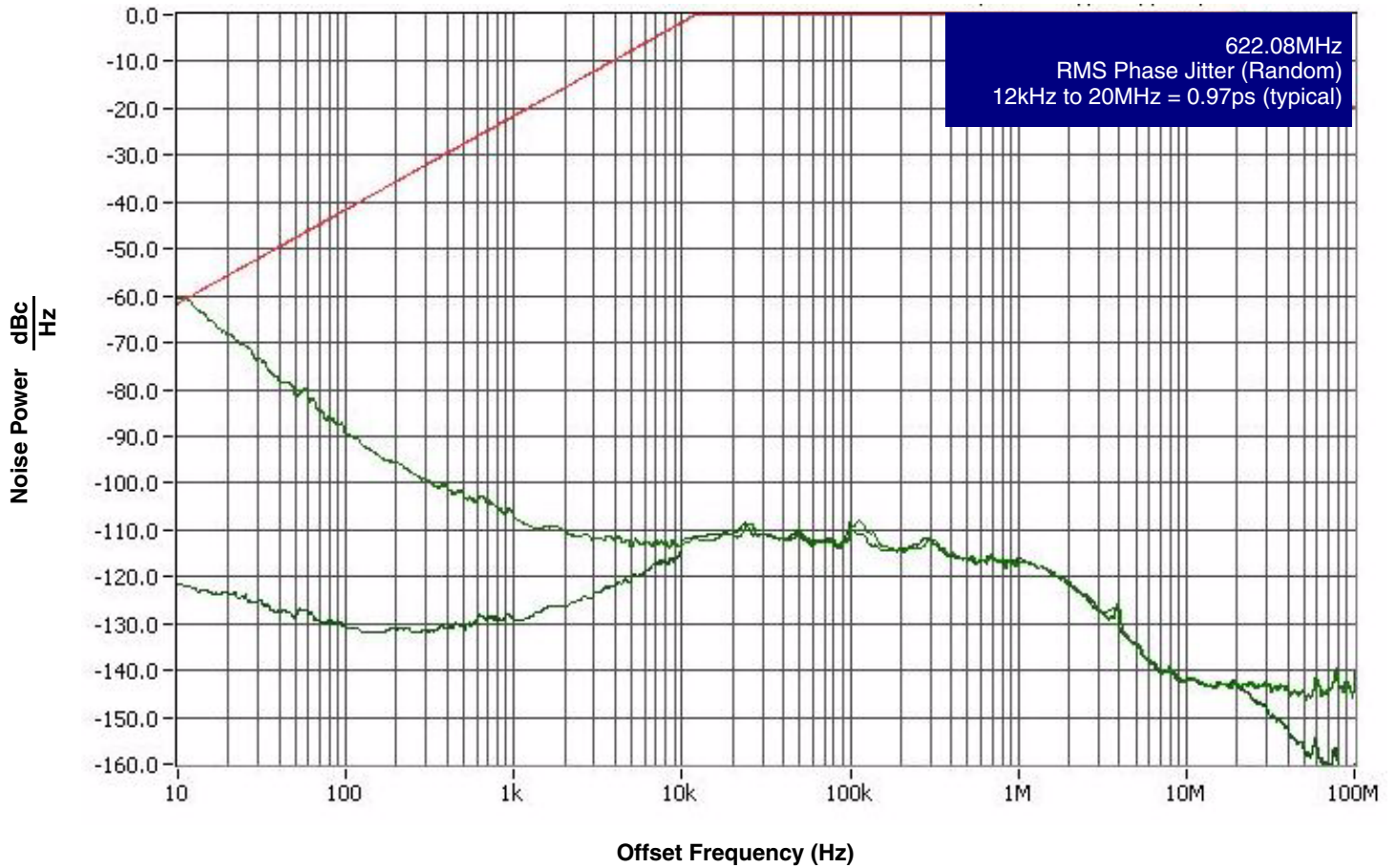
NOTE 1: Measured from the  $V_{CC}/2$  of the input to  $V_{CCO\_LVCMOS}/2$  of the output.

NOTE 2: Phase jitter measured using a 19.44MHz quartz crystal.

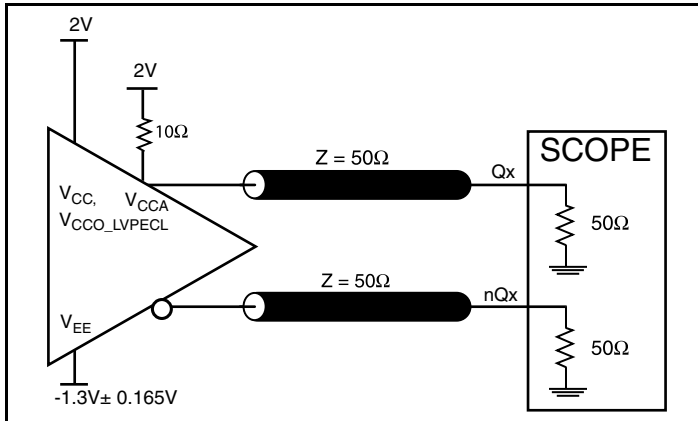
NOTE 3: REF\_OUT output duty cycle characterized with CLK input duty cycle between 48% and 52%.



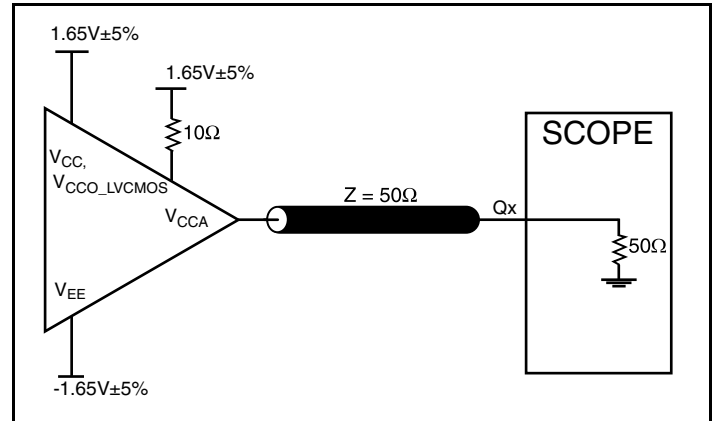
## Typical Phase Noise at 622.08MHz



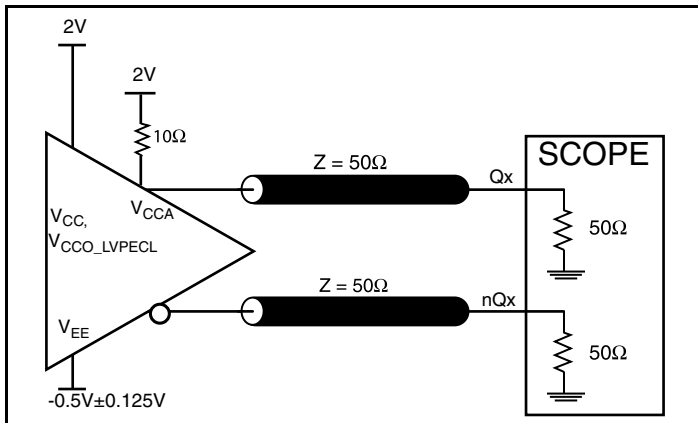
## Parameter Measurement Information



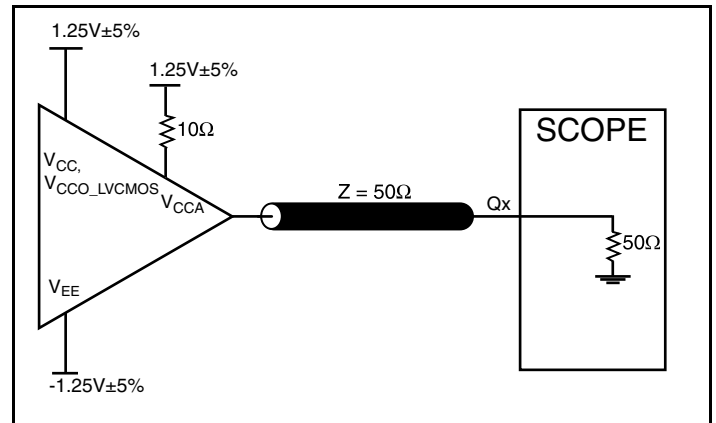
3.3V LVPECL Output Load AC Test Circuit



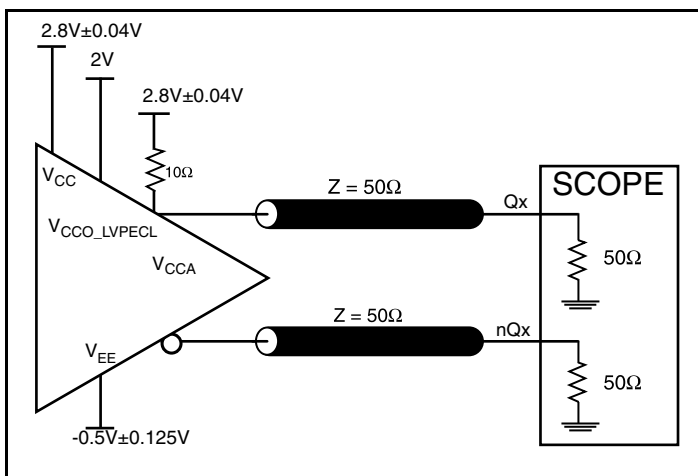
3.3V LVCMOS Output Load AC Test Circuit



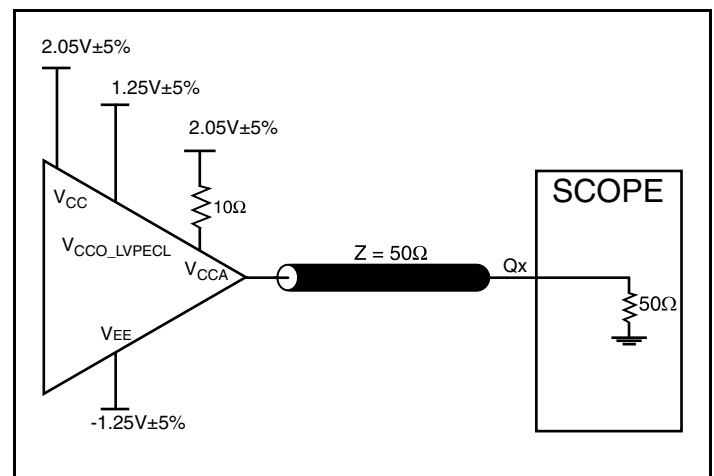
2.5V LVPECL Output Load AC Test Circuit



2.5V LVCMOS Output Load AC Test Circuit

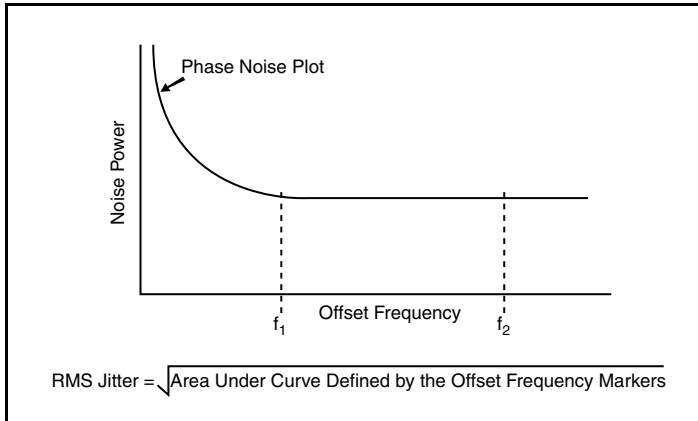


3.3 Core/2.5V LVPECL Output Load AC Test Circuit

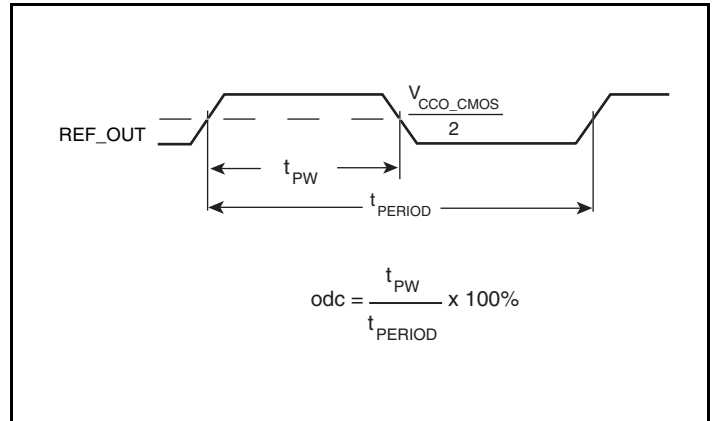


3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

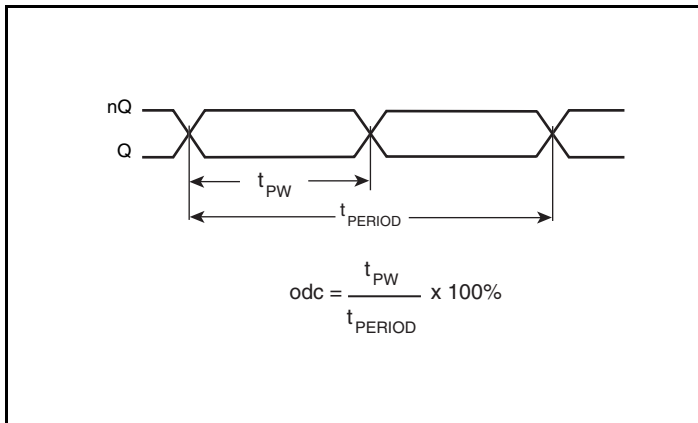
### Parameter Measurement Information, continued



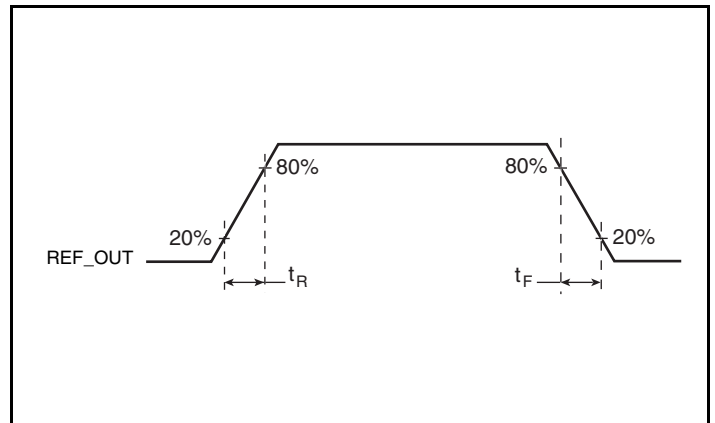
**RMS Phase Jitter**



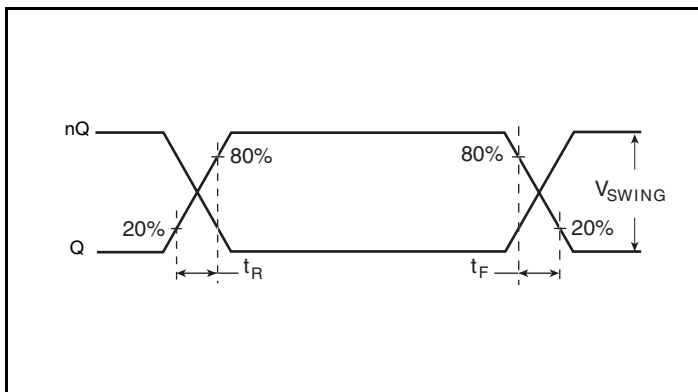
**LVCMOS Output Duty Cycle/Pulse Width/Period**



**LVPECL Output Duty Cycle/Pulse Width/Period**



**LVCMOS Output Rise/Fall Time**



**LVPECL Output Rise/Fall Time**

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

##### CLK Input

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVPECL Outputs

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

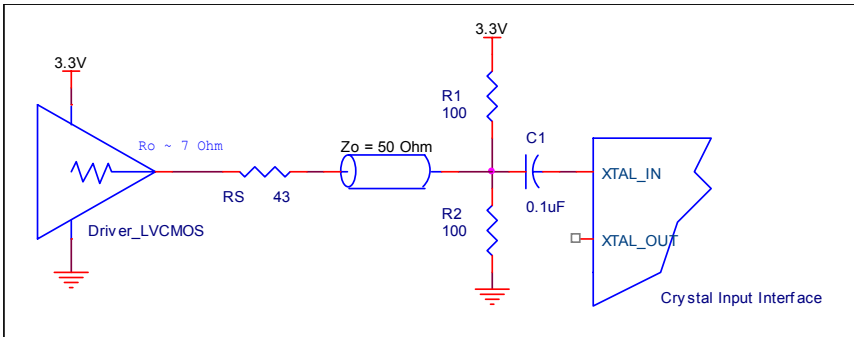
##### LVCMOS Output

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

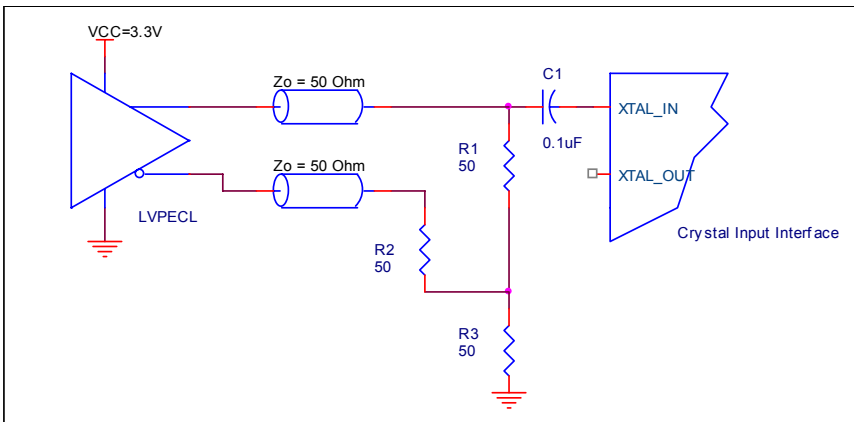
## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ . By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

*Figures 2A and 2B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

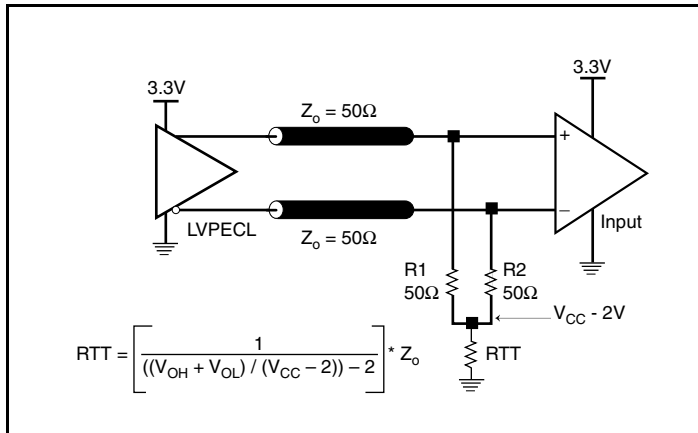


Figure 2A. 3.3V LVPECL Output Termination

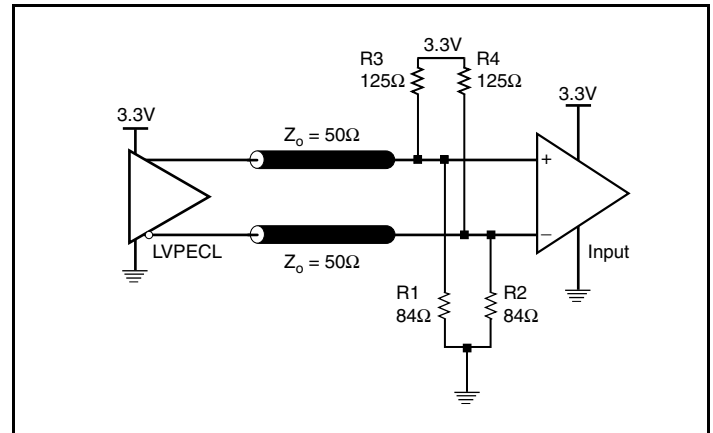


Figure 2B. 3.3V LVPECL Output Termination

## Termination for 2.5V LVPECL Outputs

Figure 3A and Figure 3B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{CC0} - 2V$ . For  $V_{CC0} = 2.5V$ , the  $V_{CC0} - 2V$  is very close to

ground level. The R3 in Figure 3B can be eliminated and the termination is shown in Figure 3C.

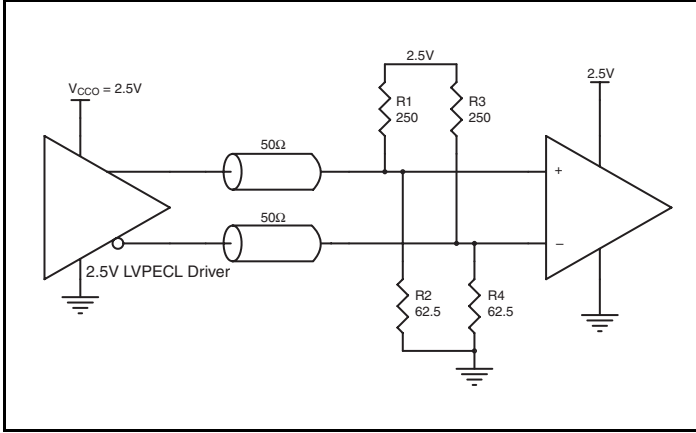


Figure 3A. 2.5V LVPECL Driver Termination Example

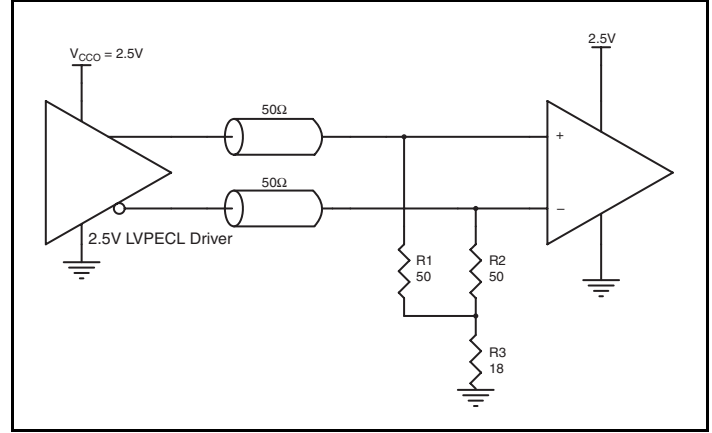


Figure 3B. 2.5V LVPECL Driver Termination Example

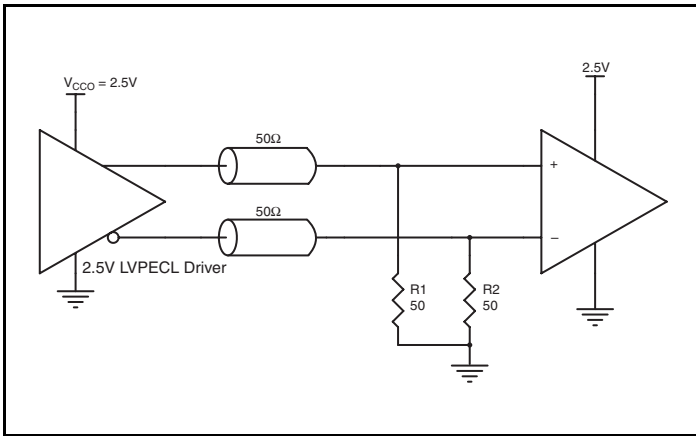


Figure 3C. 2.5V LVPECL Driver Termination Example

## Schematic Layout

Figure 6 (next page) shows an example of ICS843001I-23 application schematic. In this example, the device is operated  $V_{CC} = V_{CCO\_LVCMOS} = V_{CCO\_LVPECL} = 3.3V$ . The 18pF parallel resonant 17.5-29.54MHz crystal is used. The load capacitance  $C1 = 22pF$  and  $C2 = 22pF$  are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting  $C1$  and  $C2$ . For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843001I-23 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the

0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequency. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component with high amplitude interference is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally general design practice for power plane voltage stability suggests adding bulk capacitances in the general area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.



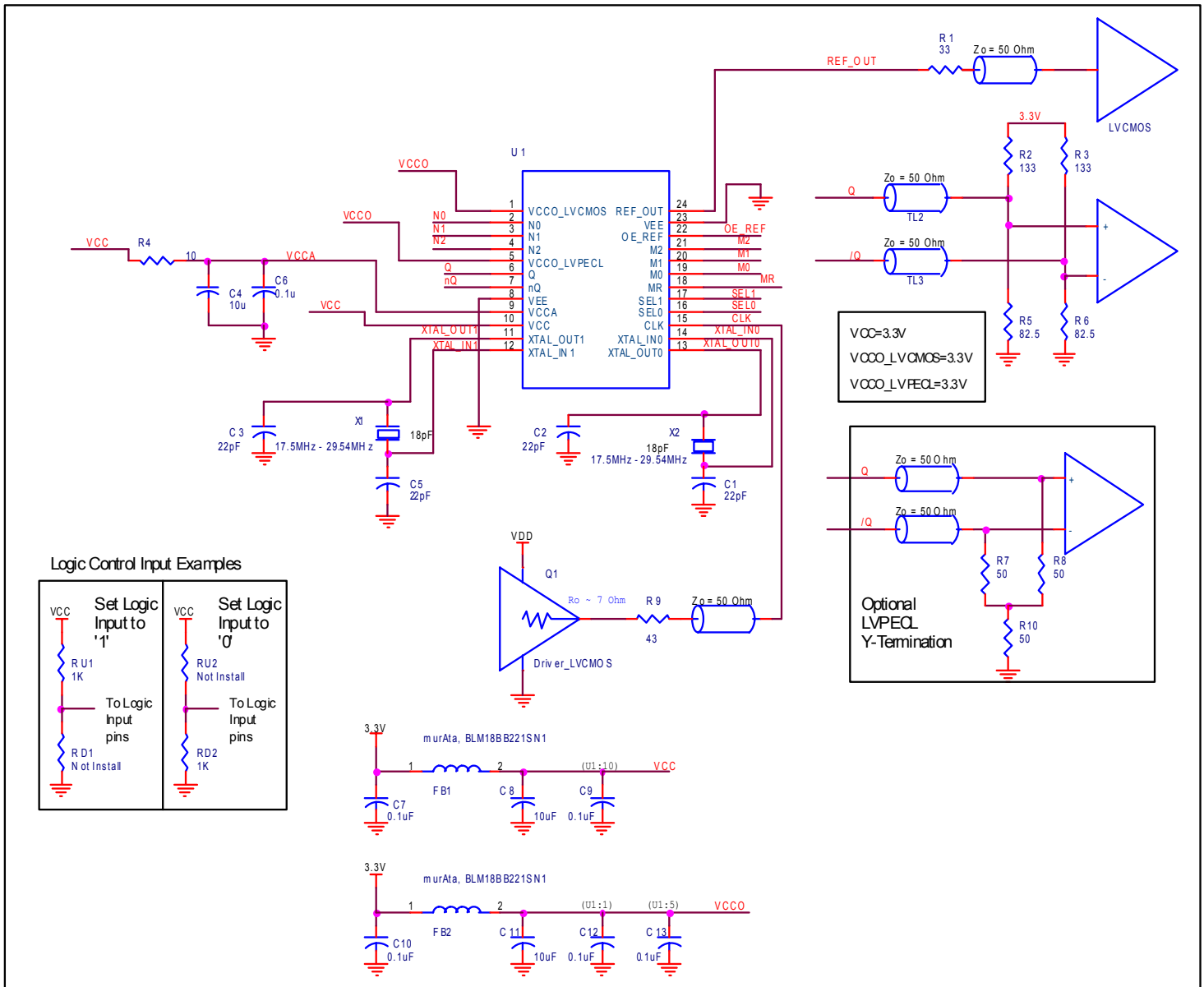


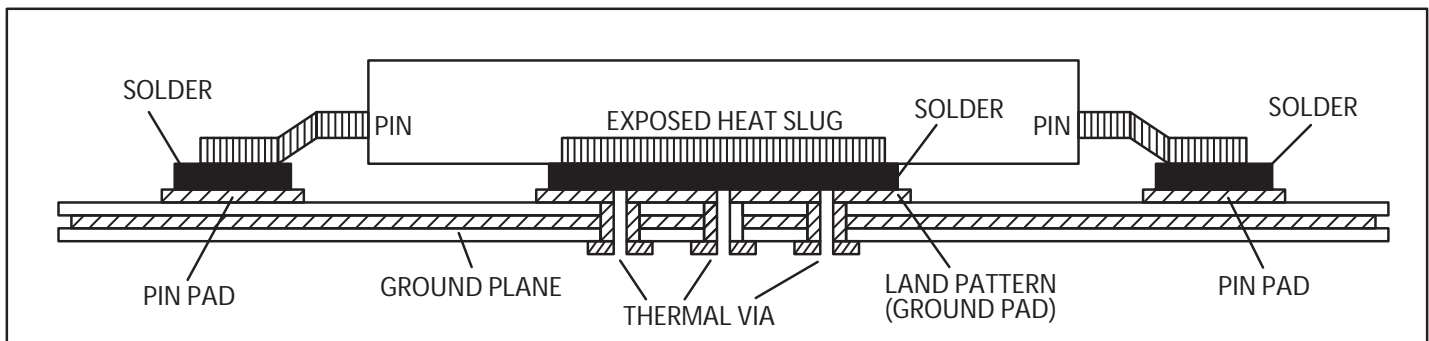
Figure 6. ICS843001I-23 Layout Example

## EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 7. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)**

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8430011-23. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8430011-23 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 140mA = 485.1mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**

### LVCMOS Output Power Dissipation

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DDO}/2$   
Output Current  $I_{OUT} = V_{DDO\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 21\Omega)] = 24.4mA$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 21\Omega * (24.4mA)^2 = 12.5mW$  per output

### Total Power Dissipation

- **Total Power**  
= Power (core) + Power (LVPECL output) + Power ( $R_{OUT}$ )  
=  $485.1mW + 30mW + 12.5mW = 527.6mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ C$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ C$  ensures that the bond wire and bond pad temperature remains below  $125^\circ C$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $32.1^\circ C/W$  per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ C$  with all outputs switching is:

$$85^\circ C + 0.528W * 32.1^\circ C/W = 102^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

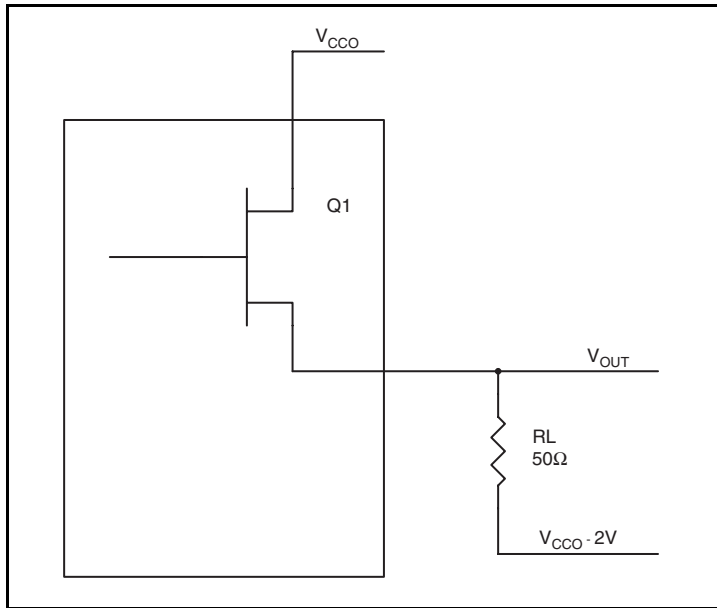
**Table 7. Thermal Resistance  $\theta_{JA}$  for 24 Lead TSSOP, E-Pad Forced Convection**

| $\theta_{JA}$ vs. Air Flow                  |                  |                  |                  |
|---|------------------|------------------|------------------|
| Meters per Second                           | 0                | 1                | 2.5              |
| Multi-Layer PCB, JEDEC Standard Test Boards | $32.1^\circ C/W$ | $25.5^\circ C/W$ | $24.0^\circ C/W$ |

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 7*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V<sub>CCO</sub> - 2V.

- For logic high, V<sub>OUT</sub> = V<sub>OH\_MAX</sub> = V<sub>CCO\_MAX</sub> - 0.9V  
(V<sub>CCO\_MAX</sub> - V<sub>OH\_MAX</sub>) = 0.9V
- For logic low, V<sub>OUT</sub> = V<sub>OL\_MAX</sub> = V<sub>CCO\_MAX</sub> - 1.7V  
(V<sub>CCO\_MAX</sub> - V<sub>OL\_MAX</sub>) = 1.7V

Pd<sub>H</sub> is power dissipation when the output drives high.

Pd<sub>L</sub> is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 24 Lead TSSOP, E-pad**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 32.1°C/W | 25.5°C/W | 24.0°C/W |

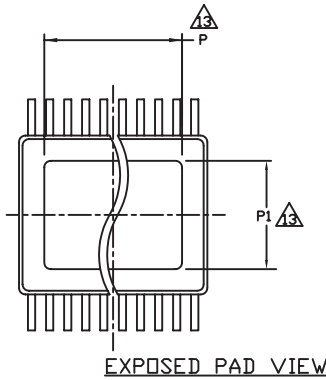
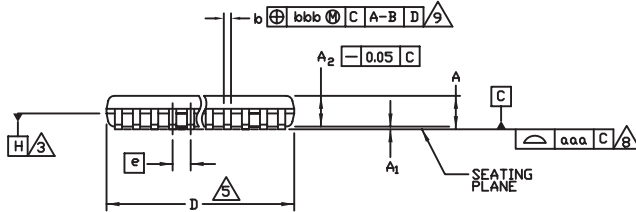
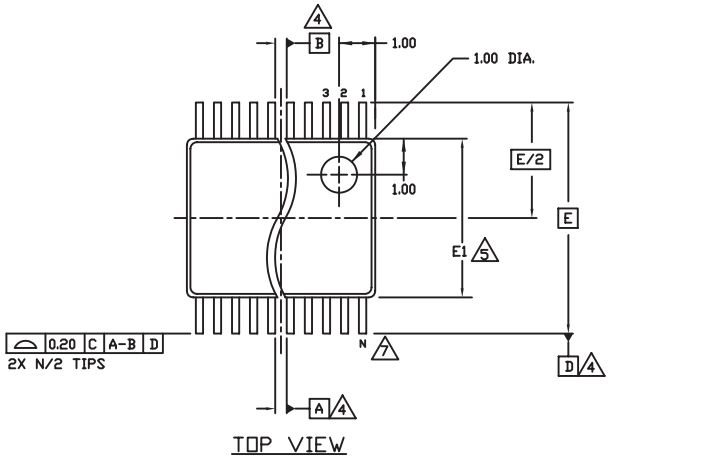
## Transistor Count

The transistor count for ICS843001I-23 is: 4165

# Package Outline and Package Dimensions

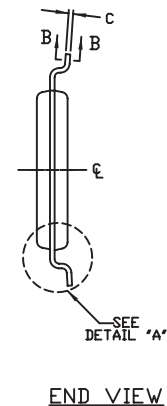
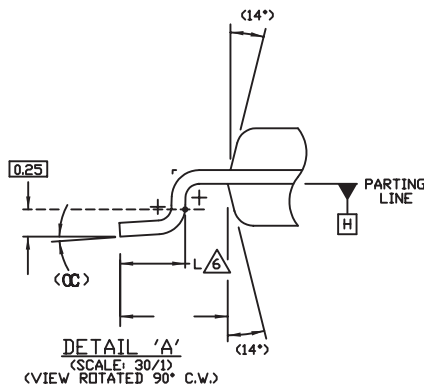
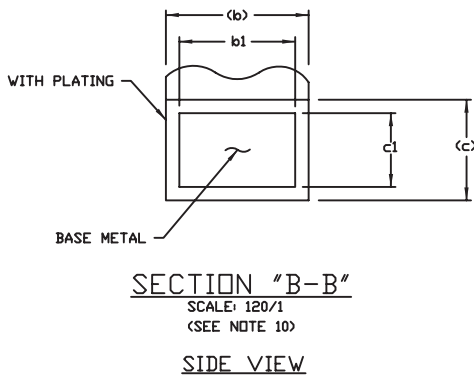
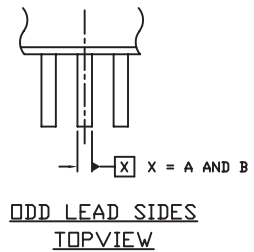
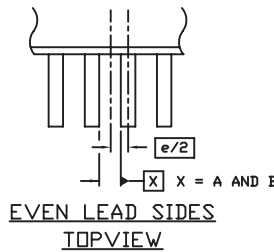
Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

Table 9. Package Dimensions



| All Dimensions in Millimeters |            |         |
|-------------------------------|------------|---------|
| Symbol                        | Minimum    | Maximum |
| N                             | 24         |         |
| A                             |            | 1.10    |
| A1                            | 0.05       | 0.15    |
| A2                            | 0.85       | 0.95    |
| b                             | 0.19       | 0.30    |
| b1                            | 0.19       | 0.25    |
| c                             | 0.09       | 0.20    |
| c1                            | 0.09       | 0.16    |
| D                             | 7.70       | 7.90    |
| E                             | 6.40 Basic |         |
| E1                            | 4.30       | 4.50    |
| e                             | 0.65 Basic |         |
| L                             | 0.50       | 0.70    |
| P                             | 5.0        | 5.5     |
| P1                            | 3.0        | 3.2     |
| $\alpha$                      | 0°         | 8°      |
| aaa                           | 0.076      |         |
| bbb                           | 0.10       |         |

Reference Document: JEDEC Publication 95, MO-153



## Ordering Information

**Table 10. Ordering Information**

| Part/Order Number | Marking       | Package                          | Shipping Packaging | Temperature   |
|-------------------|---------------|----------------------------------|--------------------|---------------|
| 843001CGI-23      | ICS843001CI23 | 24 Lead TSSOP, E-Pad             | Tube               | -40°C to 85°C |
| 843001CGI-23T     | ICS843001CI23 | 24 Lead TSSOP, E-Pad             | 2500 Tape & Reel   | -40°C to 85°C |
| 843001CGI-23LF    | ICS43001CI23L | "Lead-Free" 24 Lead TSSOP, E-Pad | Tube               | -40°C to 85°C |
| 843001CGI-23LFT   | ICS43001CI23L | "Lead-Free" 24 Lead TSSOP, E-Pad | 2500 Tape & Reel   | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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