

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR  
**2SK1284, 1284-Z**

SWITCHING  
 N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK1284 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

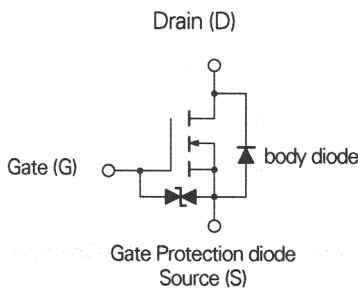
- Low On-state Resistance  
 $R_{DS(on)} \leq 0.32 \Omega$  ( $V_{GS} = 10 V, I_D = 2 A$ )  
 $R_{DS(on)} \leq 0.40 \Omega$  ( $V_{GS} = 4.0 V, I_D = 2 A$ )
- Low  $C_{iss}$ :  $C_{iss} = 500 pF$  TYP.
- Built-in G-S Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ C$ )

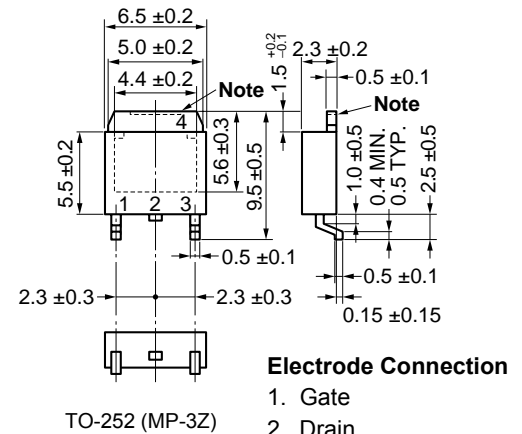
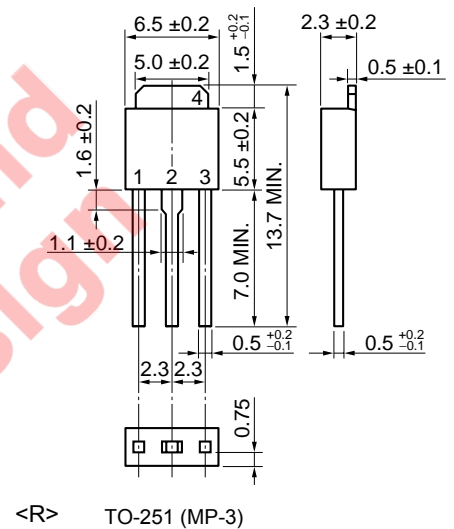
|  |                |             |            |
|--|----------------|-------------|------------|
| Drain to Source Voltage                        | $V_{DSS}$      | 100         | V          |
| Gate to Source Voltage (AC)                    | $V_{GSS(AC)}$  | $\pm 20$    | V          |
| Gate to Source Voltage (DC)                    | $V_{GSS(DC)}$  | -10, +20    | V          |
| Drain Current (DC)                             | $I_{D(DC)}$    | $\pm 3.0$   | A          |
| Drain Current (pulse) <sup>Note</sup>          | $I_{D(pulse)}$ | $\pm 12$    | A          |
| Total Power Dissipation ( $T_C = 25^\circ C$ ) | $P_{T1}$       | 20          | W          |
| Total Power Dissipation ( $T_A = 25^\circ C$ ) | $P_{T2}$       | 1.0         | W          |
| Channel Temperature                            | $T_{ch}$       | 150         | $^\circ C$ |
| Storage Temperature                            | $T_{stg}$      | -55 to +150 | $^\circ C$ |

Note  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1\%$

EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)



- Electrode Connection**
1. Gate
  2. Drain
  3. Source
  4. Drain Fin

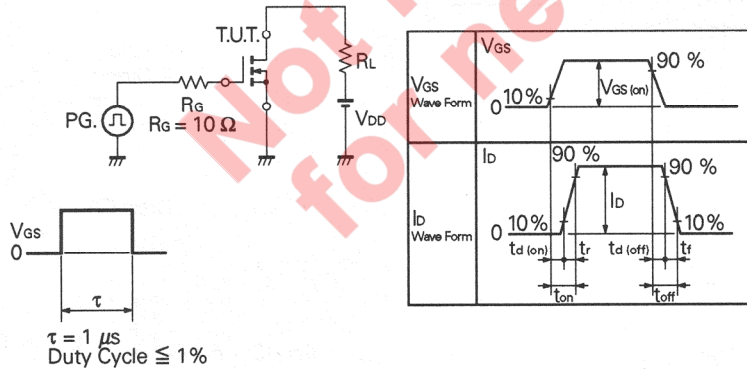
Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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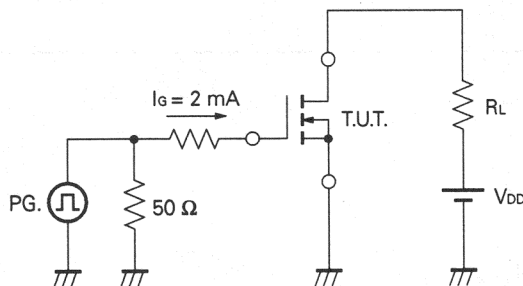
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

| CHARACTERISTIC                      | SYMBOL               | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS                               |
|-------------------------------------|----------------------|------|------|------|------|---|
| Drain to Source On-state Resistance | R <sub>DS(on)</sub>  |      | 0.26 | 0.32 | Ω    | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2 A  |
| Drain to Source On-state Resistance | R <sub>DS(on)</sub>  |      | 0.32 | 0.40 | Ω    | V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 2 A |
| Gate to Source Cutoff Voltage       | V <sub>GS(off)</sub> | 1.0  |      | 2.5  | V    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA |
| Forward Transfer Admittance         | y <sub>fs</sub>      | 2.4  |      |      | S    | V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2 A  |
| Drain Leakage Current               | I <sub>DSS</sub>     |      |      | 10   | μA   | V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0  |
| Gate to Source Leakage Current      | I <sub>GSS</sub>     |      |      | ±10  | μA   | V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0  |
| Input Capacitance                   | C <sub>iss</sub>     |      | 500  |      | pF   | V <sub>DS</sub> = 10 V                        |
| Output Capacitance                  | C <sub>oss</sub>     |      | 160  |      | pF   | V <sub>GS</sub> = 0                           |
| Reverse Transfer Capacitance        | C <sub>rss</sub>     |      | 20   |      | pF   | f = 1 MHz                                     |
| Turn-On Delay Time                  | t <sub>d(on)</sub>   |      | 40   |      | ns   | V <sub>GS(on)</sub> = 10 V                    |
| Rise Time                           | t <sub>r</sub>       |      | 55   |      | ns   | V <sub>DD</sub> = 50 V                        |
| Turn-Off Delay Time                 | t <sub>d(off)</sub>  |      | 500  |      | ns   | I <sub>D</sub> = 2 A, R <sub>G</sub> = 10 Ω   |
| Fall Time                           | t <sub>f</sub>       |      | 120  |      | ns   | R <sub>L</sub> = 25 Ω                         |
| Total Gate Charge                   | Q <sub>G</sub>       |      | 13   |      | nC   | V <sub>GS</sub> = 10 V                        |
| Gate to Source Charge               | Q <sub>GS</sub>      |      | 3    |      | nC   | I <sub>D</sub> = 3 A                          |
| Gate to Drain Charge                | Q <sub>GD</sub>      |      | 2    |      | nC   | V <sub>DD</sub> = 80 V                        |
| Diode Forward Voltage               | V <sub>SD</sub>      |      | 0.9  |      | V    | I <sub>SD</sub> = 3 A, V <sub>GS</sub> = 0    |
| Reverse Recovery Time               | t <sub>rr</sub>      |      | 140  |      | ns   | I <sub>F</sub> = 3 A, V <sub>GS</sub> = 0     |
| Reverse Recovery Charge             | Q <sub>rr</sub>      |      | 250  |      | nC   | di/dt = 50 A/μs                               |

**Test Circuit 1: Switching Time**

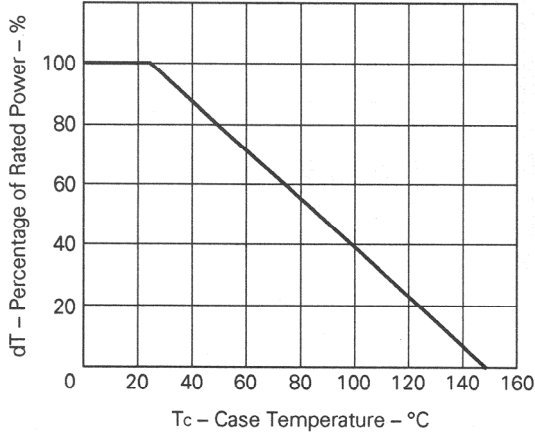


**Test Circuit 2: Gate Charge**

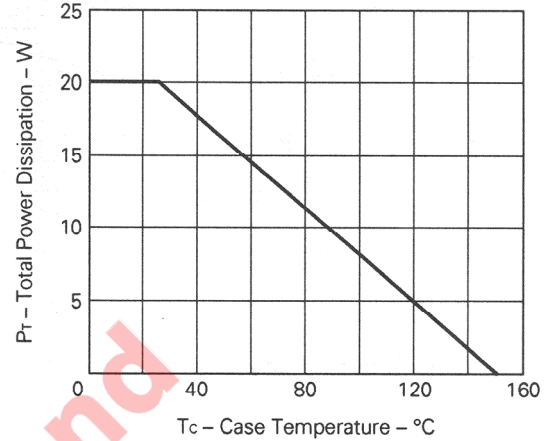


TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)

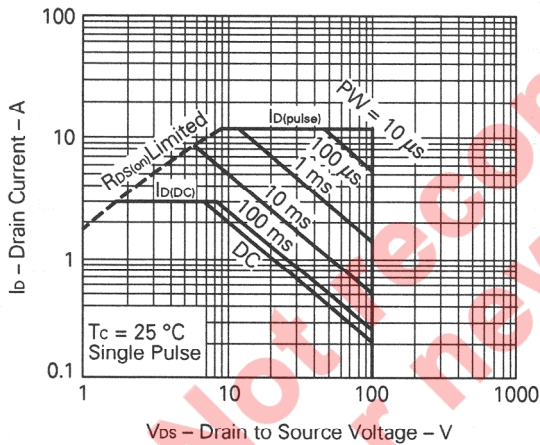
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



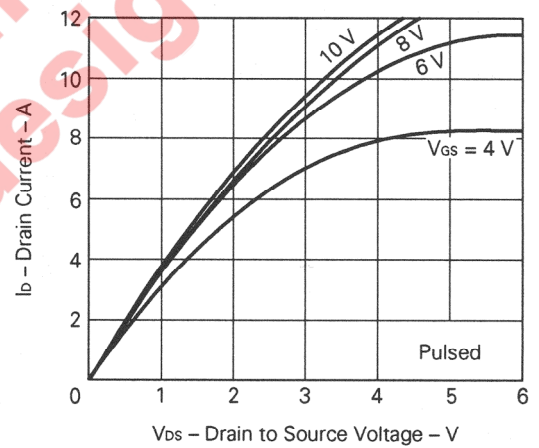
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



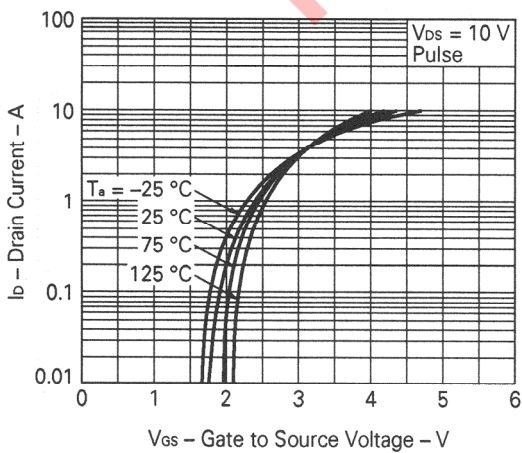
FORWARD BIAS SAFE OPERATING AREA

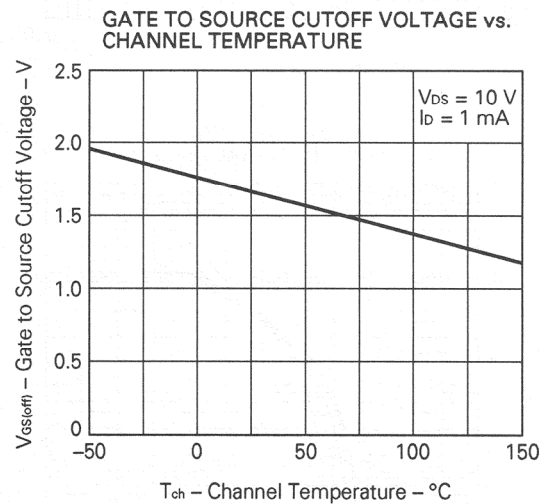
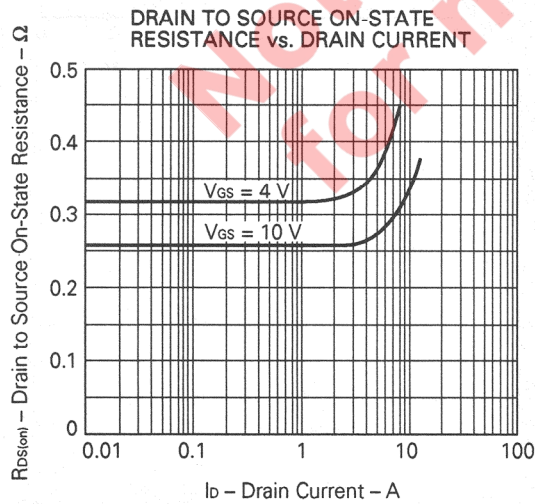
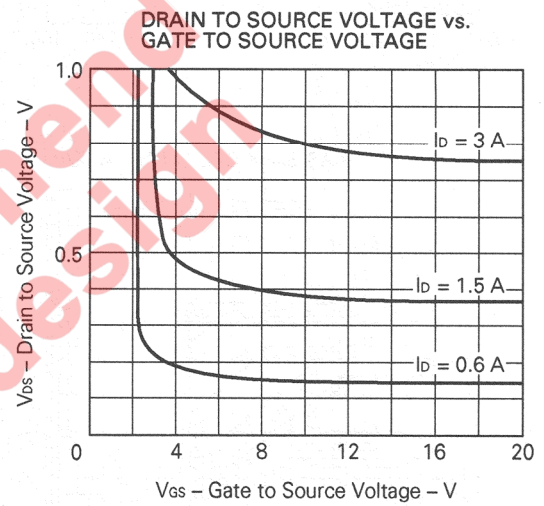
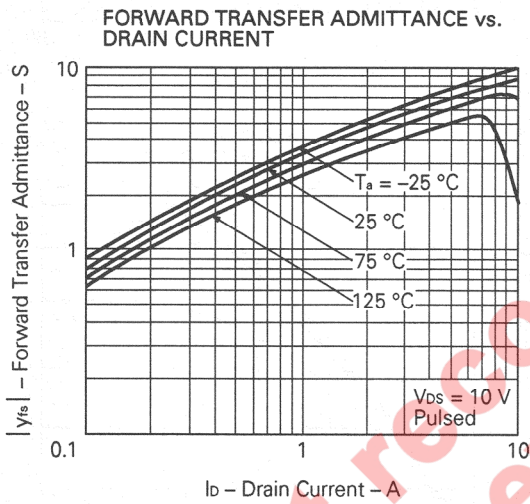
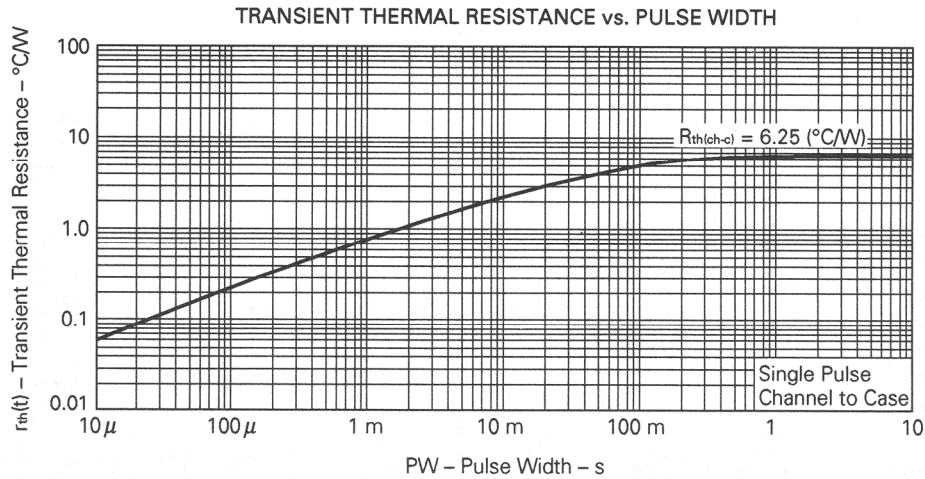


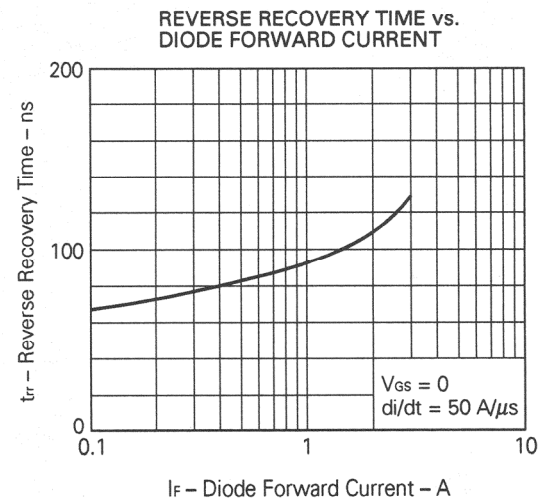
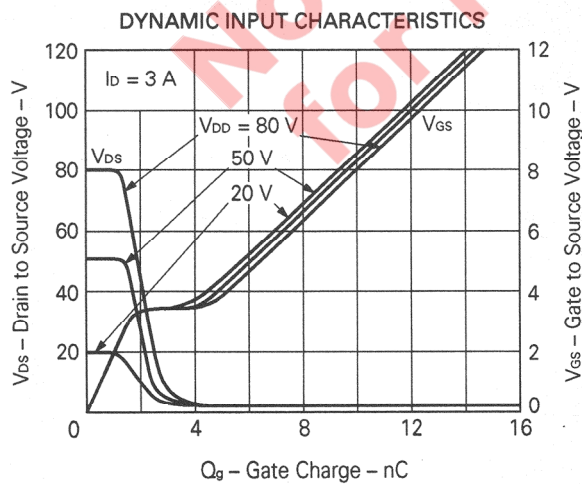
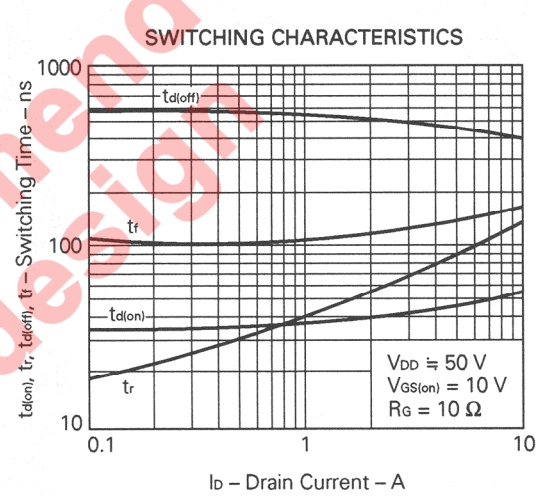
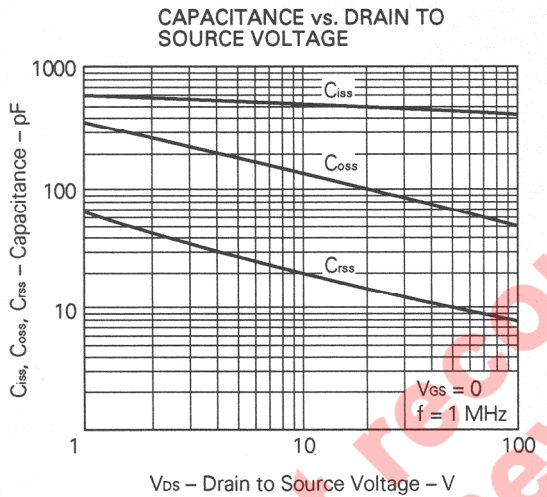
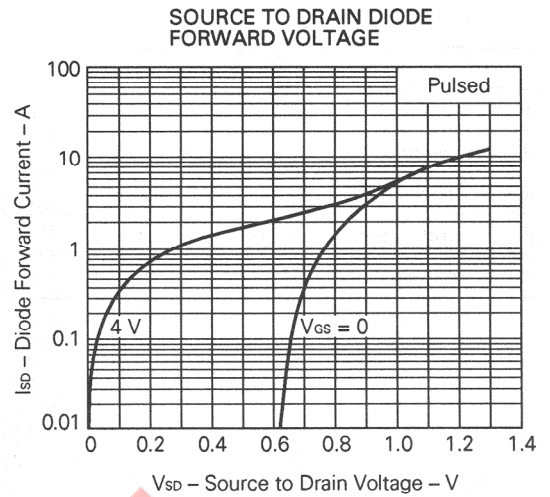
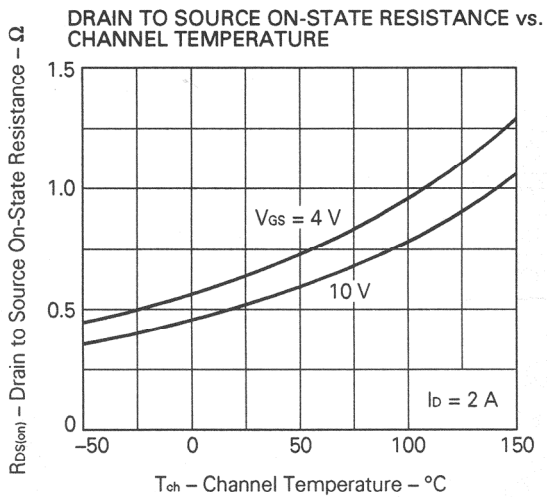
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSFER CHARACTERISTICS







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