



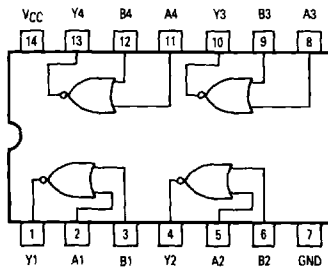
Quad 2-Input Positive NOR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/30301

Military 54LS02



LOGIC DIAGRAM



AVAILABLE AS:

- 1) JAN: JM38510/30301BXA
- 2) SMD: *
- 3) 883C: 54LS02/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

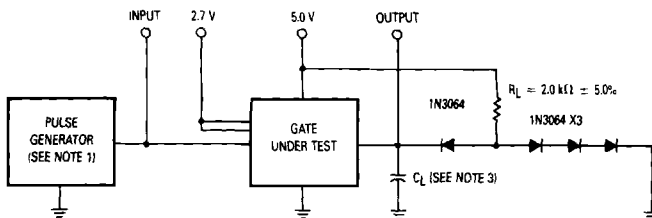
*Call Factory for latest update

PIN ASSIGNMENTS

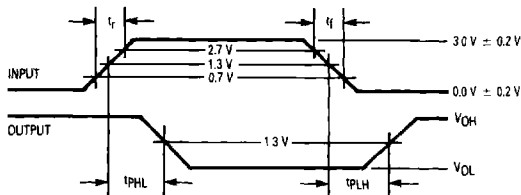
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
Y1	1	1	2	VCC
A1	2	2	3	GND
B1	3	3	4	GND
Y2	4	4	6	VCC
A2	5	5	8	GND
B2	6	6	9	GND
GND	7	7	10	GND
A3	8	8	12	GND
B3	9	9	13	GND
Y3	10	10	14	VCC
A4	11	11	16	GND
B4	12	12	18	GND
Y4	13	13	19	VCC
VCC	14	14	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

AC TEST CIRCUIT



WAVEFORMS



NOTES:

- 1 Pulse generator has the following characteristics: $t_r \approx 6.0$ ns, $t_f \approx 15$ ns, PRR ≤ 1.0 MHz, $t_D = 0.5$ μ s and $Z_{OUT} = 50$ Ω .
- 2 Diodes are 1N3064 or equivalent.
- 3 $C_L = 50$ pF $\approx 10\%$, including scope probe, wiring and stray capacitance, without package in test fixture.
- 4 $R_L = 2.0$ k $\Omega \pm 5.0\%$.
- 5 Voltage measurements are to be made with respect to network ground terminal.

TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

54LS02

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -400 μA, V _{IL} = 0.7 V, other input = 0.7 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IH} = 2.0 V, other input = 0 V.
V _{IC}	Input Clamping Voltage		-1.5					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other input is open.
I _{IH1}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.7 V, other input = 0 V.
I _{IH2}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other input = 0 V.
I _{IL}	Logical "0" Input Current	-150	-380	-150	-380	-150	-380	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs = 5.5 V.
I _{OS}	Output Short Circuit Current	-15	-100	-15	-100	-15	-100	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs), V _{OUT} = 0 V.
I _{CCH}	Power Supply Current		3.2		3.2		3.2	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCL}	Power Supply Current		5.4		5.4		5.4	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (all inputs).
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL}	Propagation Delay :Data-Output	2.0	16	2.0	26	2.0	26	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PHL}	Output High-Low	—	15	—	21	—	21	ns	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.
t _{PLH}	Propagation Delay :Data-Output	2.0	22	2.0	30	2.0	30	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 2.0 kΩ.
t _{PLH}	Output Low-High	—	15	—	25	—	25	ns	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 2.0 kΩ.

NOTE:

1. The limits specified for C_L = 15 pF are guaranteed but not tested.