To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

DATA SHEET

MOS FIELD EFFECT TRANSISTOR

2SK4070

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4070 is N-channel MOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

FEATURES

- Low on-state resistance
  $R_{DS(on)}$ = 11 Ω MAX. (V_{GS} = 10 V, I_D = 0.5 A)
- Low gate charge
  Q_G = 5 nC TYP. (V_{DD} = 450 V, V_{GS} = 10 V, I_D = 1.0 A)
- Gate voltage rating : ±30 V
- Avalanche capability ratings

<R> ### ORDERING INFORMATION

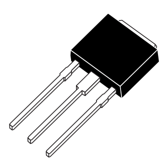
PART NUMBER	LEAD PLATING	PACKING	PACKAGE
2SK4070-S15-AY Note	Pure Sn (Tin)	Tube 70 p/tube	TO-251 (MP-3-a) typ. 0.39 g
2SK4070(1)-S27-AY Note		Tube 75 p/tube	TO-251 (MP-3-b) typ. 0.34 g
2SK4070-ZK-E1-AY Note		Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g
2SK4070-ZK-E2-AY Note			

Note Pb-free (This product does not contain Pb in external electrode.)

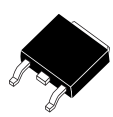
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	600	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±1.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±4.0	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	22	W
Total Power Dissipation (T_A = 25°C) Note2	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	0.8	A
Single Avalanche Energy Note3	E_{AS}	38.4	mJ

(TO-251)



(TO-252)



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on glass epoxy board of 40 mm × 40 mm × 1.6 mm

3. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω, V_{GS} = 20 → 0 V

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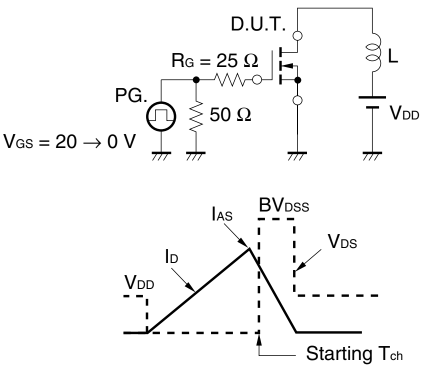
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

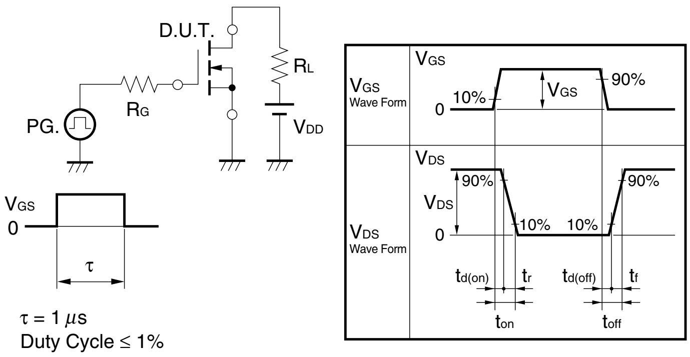
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 600 V, V_{GS} = 0 V			100	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	2.5	2.9	3.5	V
Forward Transfer Admittance Note	$\lvert y_{fs} \rvert$	V_{DS} = 10 V, I_D = 0.5 A	0.2	0.4		S
Drain to Source On-state Resistance Note	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 0.5 A		9.2	11	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V,		110		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		50		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		11		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 0.5 A,		7.5		ns
Rise Time	t_r	V_{GS} = 10 V,		6		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		11		ns
Fall Time	t_f			18		ns
Total Gate Charge	Q_G	V_{DD} = 450 V,		5		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V,		1		nC
Gate to Drain Charge	Q_{GD}	I_D = 1.0 A		2.8		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 1.0 A, V_{GS} = 0 V		0.86	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 1.0 A, V_{GS} = 0 V,		135		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		285		nC

Note Pulsed

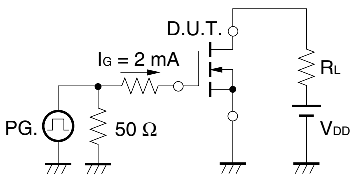
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

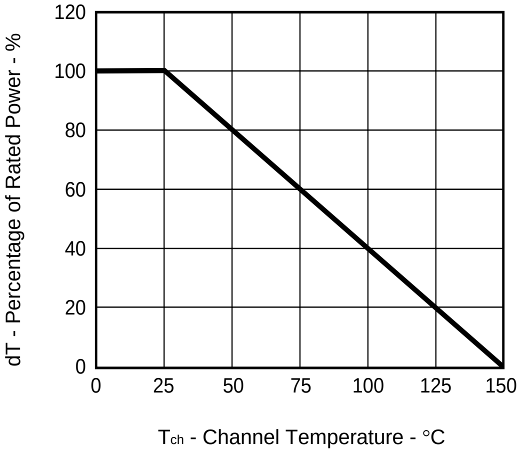


TEST CIRCUIT 3 GATE CHARGE

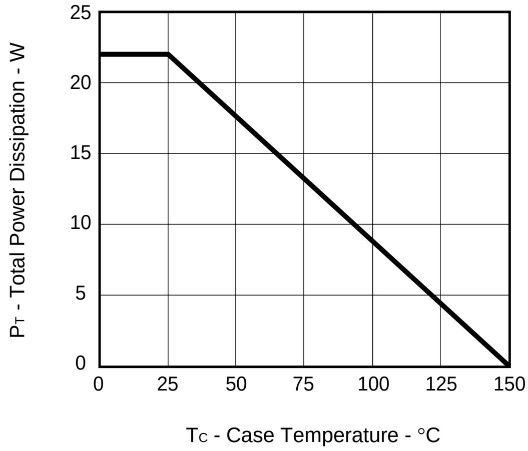


TYPICAL CHARACTERISTICS (T_A = 25°C)

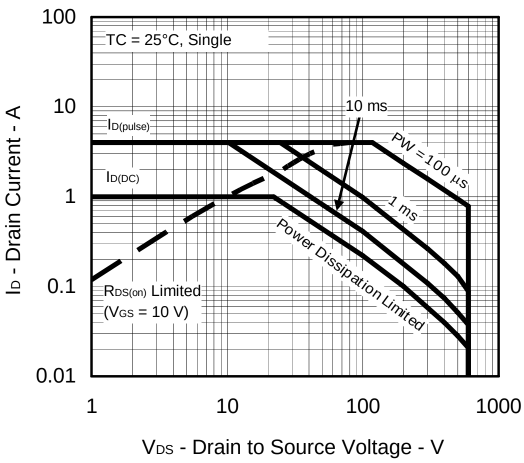
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



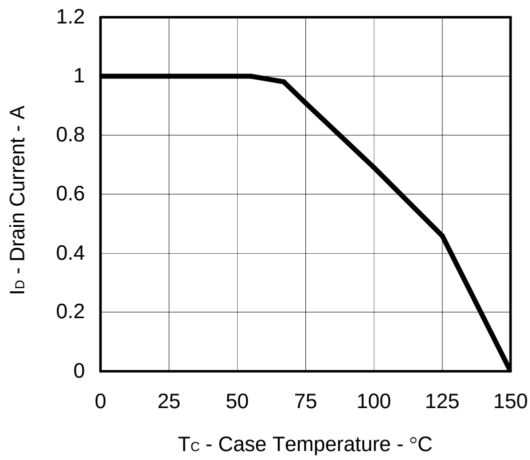
<R> TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



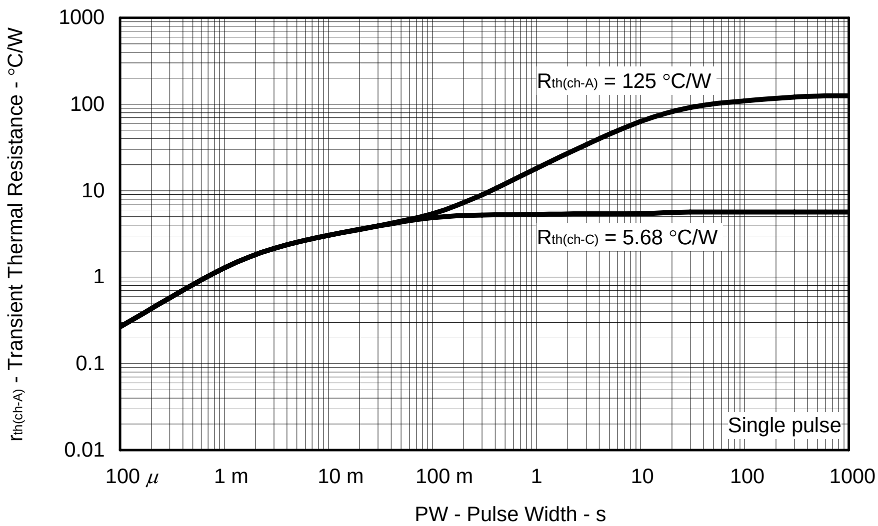
<R> FORWARD BIAS SAFE OPERATING AREA



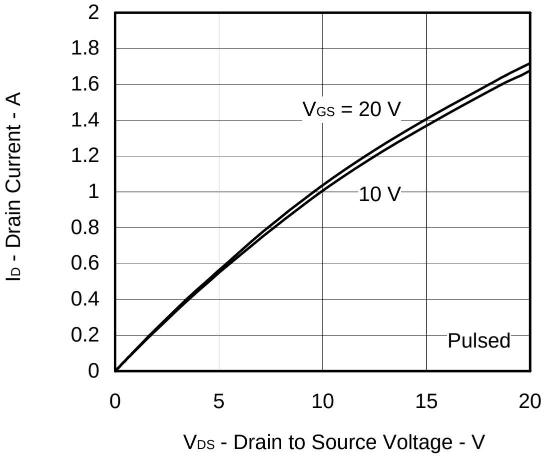
DRAIN CURRENT vs. CASE TEMPERATURE



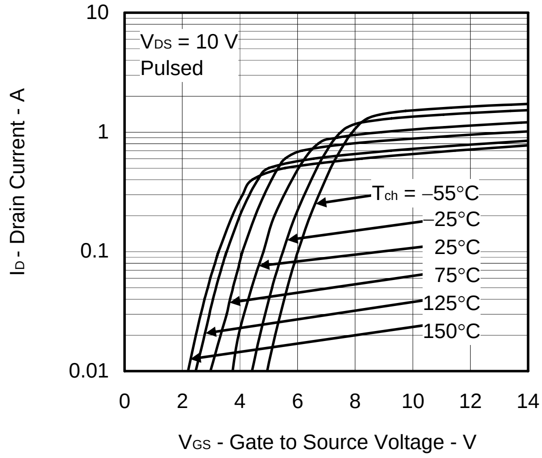
<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



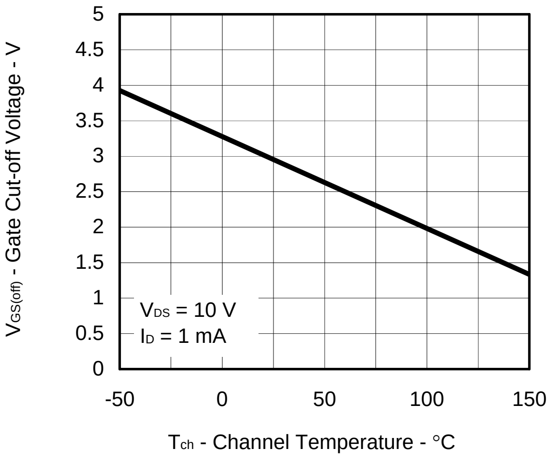
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



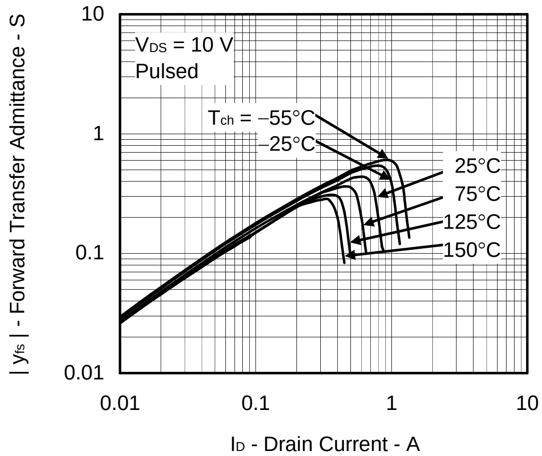
FORWARD TRANSFER CHARACTERISTICS



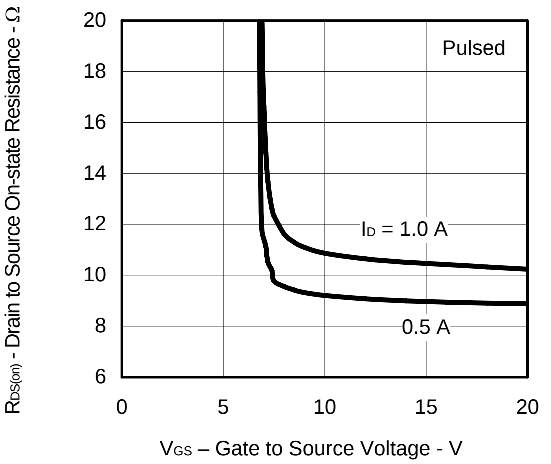
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



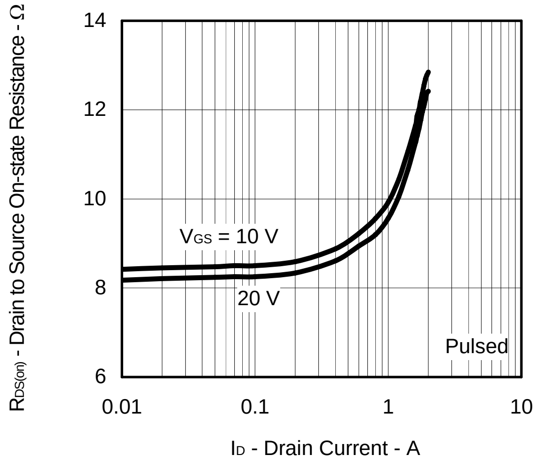
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



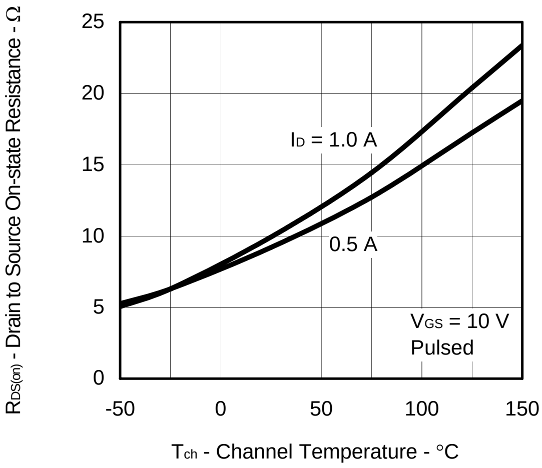
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



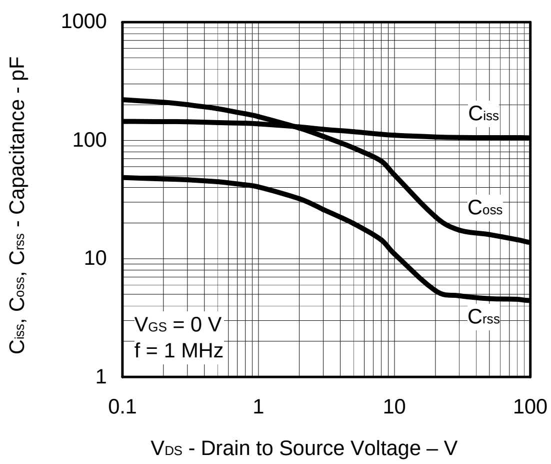
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



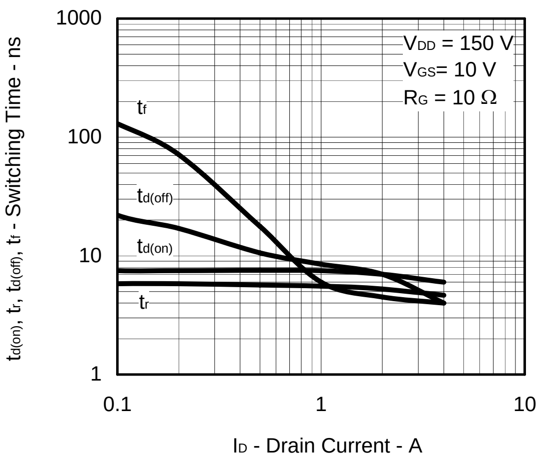
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



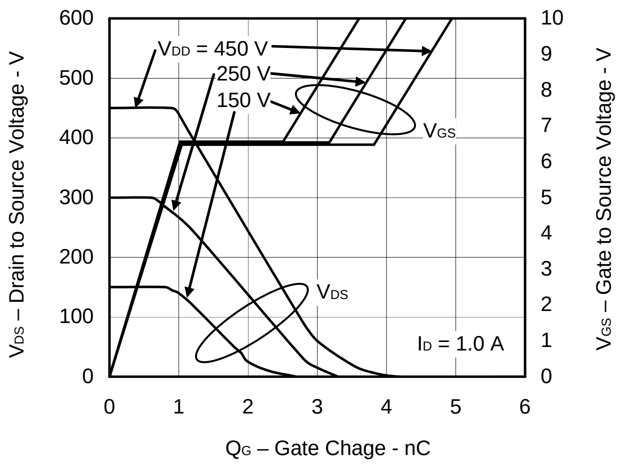
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



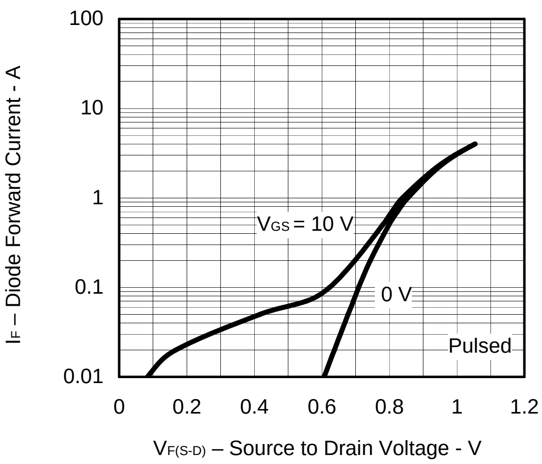
SWITCHING CHARACTERISTICS



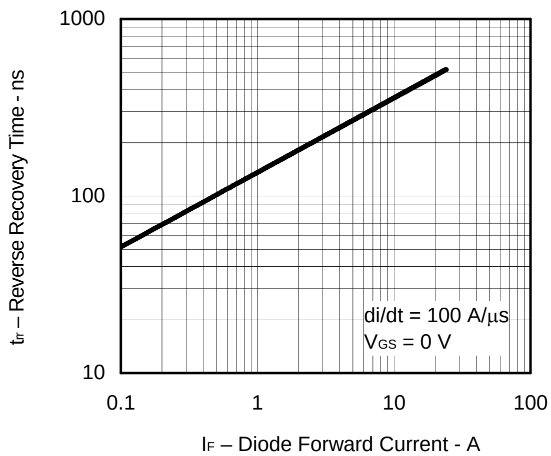
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



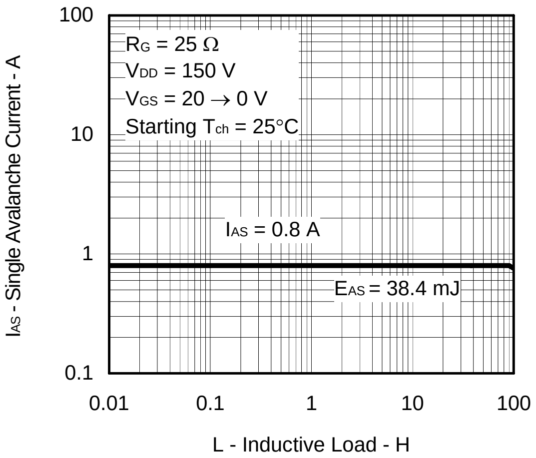
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



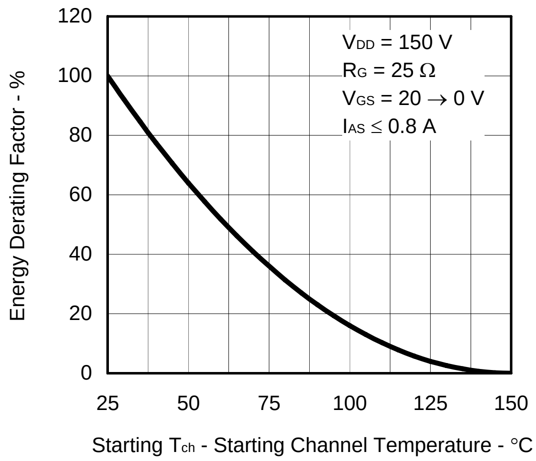
REVWESE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD

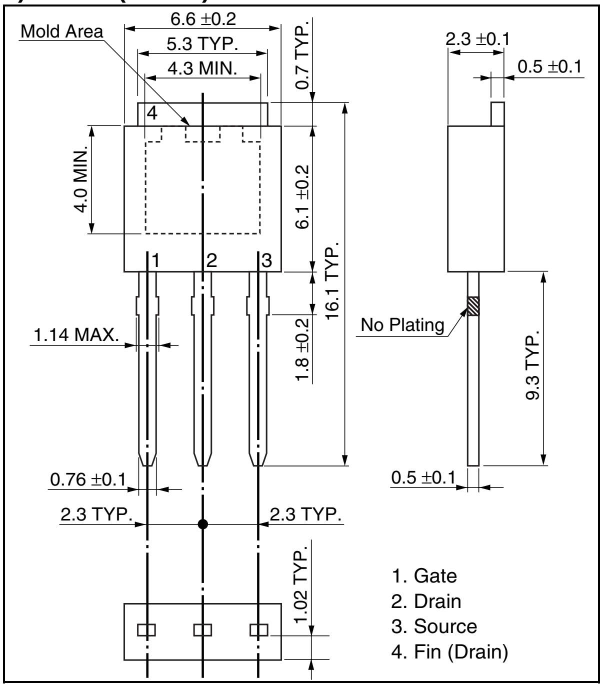


SINGLE AVALANCHE ENERGY DERATING FACTOR

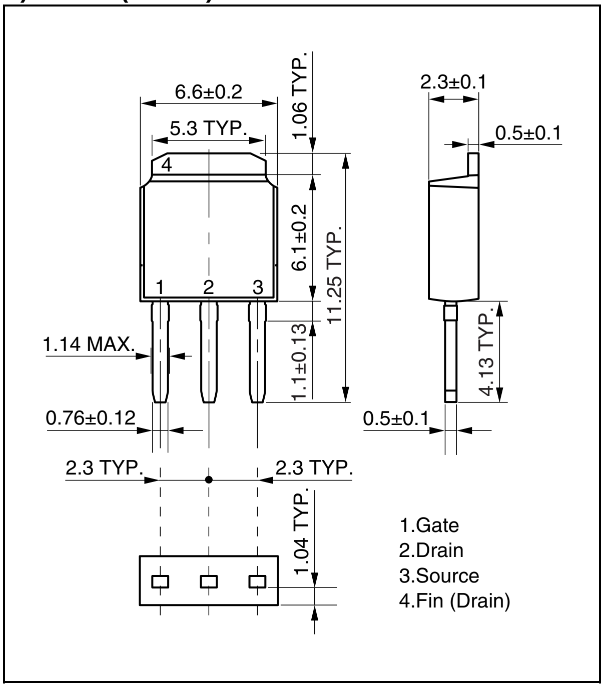


<R> **PACKAGE DRAWINGS (Unit: mm)**

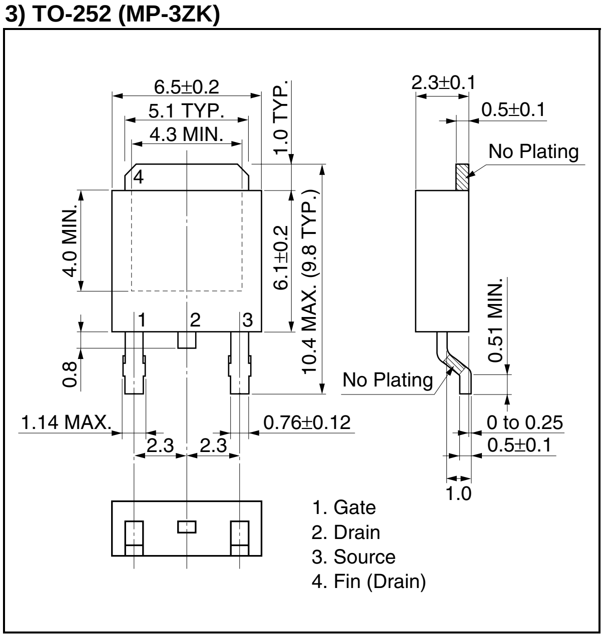
1) TO-251 (MP-3-a)



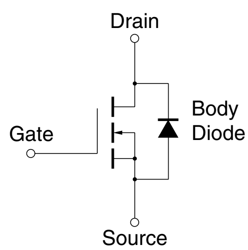
2) TO-251 (MP-3-b)



3) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.